Introduction to LVDS

Chapter 1

1.0.0 INTRODUCTION TO LVDS

LVDS stands for Low Voltage Differential Signaling. It is a way to communicate data using a very low voltage swing (about 350mV) over two differential PCB traces or a balanced cable.

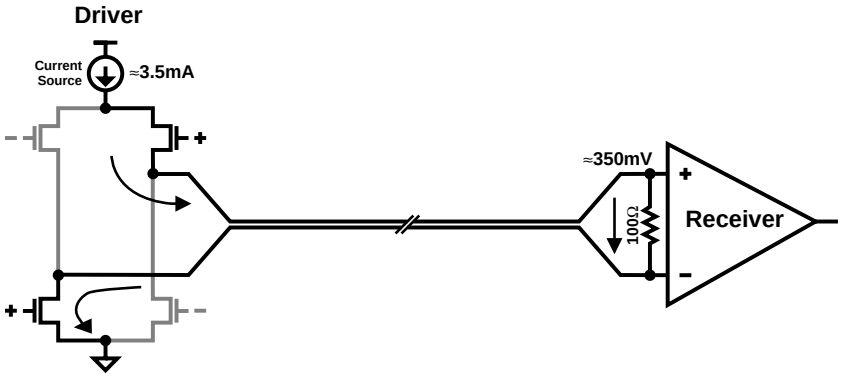
1.1.0 THE TREND TO LVDS

Consumers are demanding more realistic, visual information in the office and in the home. This is driving the need to move video, 3-D graphics, and photorealistic image data from camera to PCs and printers through LAN, phone, and satellite systems to home set top boxes and digital VCRs. Solutions exist today to move this high speed digital data both very short and very long distances: on a printed circuit board (PCB) and across fiber or satellite networks. Moving this data from board to board or box to box, however, requires an extremely high performance solution that consumes a minimum of power, generates little noise (must meet increasingly stringent FCC/CISPR EMI requirements), is relatively immune to noise, and is inexpensive. Unfortunately existing solutions are a compromise of these four basic ingredients: **performance, power, noise, and cost.**

1.2.0 GETTING SPEED WITH LOW NOISE AND LOW POWER

LVDS is a low swing, differential signaling technology which allows single channel data transmission at hundreds of Megabits per second (Mbps). Its low swing and current mode driver outputs create low noise and provide a very low power consumption across frequency.

1.2.1 How LVDS Works



Simplified diagram of LVDS driver and receiver connected via 100Ω controlled differential impedance media.

National's LVDS outputs consist of a current source (nominal 3.5mA) which drives one of the differential pair lines. The receiver has high DC impedance (it does not source or sink DC current), so the majority of driver current flows across the 100Ω termination resistor generating about 350mV across the receiver inputs. When the driver switches, it changes the direction of current flow across the resistor, thereby creating a valid "one" or "zero" logic state.

1.2.2 Why Low Swing Differential?

The differential data transmission method used in LVDS is less susceptible to common-mode noise than single-ended schemes. Differential transmission uses two wires with opposite current/voltage swings instead of the one wire used in single-ended methods to convey data information. The advantage of the differential approach is that noise is coupled onto the two wires as common mode (the noise appears on both lines equally) and is thus rejected by the receivers which looks at only the *difference* between the two signals. The differential signals also tend to radiate less noise than single-ended signals due to the canceling of magnetic fields. And, the current mode driver is not prone to ringing and switching spikes, further reducing noise.

Because differential technologies such as LVDS reduce concerns about noise, they can use lower signal voltage swings. This advantage is crucial, because it is impossible to raise data rates and lower power consumption without using low voltage swings. The low swing nature of the driver means data can be switched very quickly. Since the driver is also current mode, very low — almost flat — power consumption across frequency is achieved since the power consumed by the load (3.5mA x 350mV ≈ 1.2mW) stays almost constant.

1.2.3 The LVDS Standards

Two key industry standards define LVDS: one from the ANSI/TIA/EIA (American National Standards Institute/Telecommunications Industry Association/Electronic Industries Association) and another from the IEEE (Institute for Electrical and Electronics Engineering).

The generic (multi-application) LVDS standard, **ANSI/TIA/EIA-644**, began in the TIA Data Transmission Interface committee TR30.2. The ANSI/TIA/EIA standard defines driver output and receiver input characteristics, thus it is an electrical-only standard. It does not include functional specifications, protocols or even complete cable characteristics since these are application dependent. ANSI/TIA/EIA-644 is intended to be reference by other standards that specify the complete interface (connectors, protocol, etc.). This allows it to be easily adopted into many applications.

ANSI/TIA/EIA-644 (LVDS) Standard

Note: Actual datasheet specifications may be significantly better.

Parameter	Description	Min	Max	Units
V_{OD}	Differential Output Voltage	247	454	mV
V_{OS}	Offset Voltage	1.125	1.375	V
ΔV_{OD}	|Change in V_{OD}|		50	|mV|
ΔV_{OS}	|Change in V_{OS}|		50	|mV|
I_{SC}	|Short Circuit Current|		24	|mA|
t_r/t_f	Output Rise/Fall Times (≥200Mbps)	0.26	1.5	ns
	Output Rise/Fall Times (<200Mbps)		30% of t_{ui}†	
I_{IN}	|Input Current|		20	|µA|
V_{TH}	|Threshold Voltage|		100	|mV|
V_{IN}	Input Voltage Range	0	2.4	V

† t_{ui} is unit interval (i.e bit width).

The ANSI/TIA/EIA standard does specify a recommended maximum data rate of 655Mbps and a theoretical maximum of 1.923Gbps based on a lossless medium. The standard also covers minimum media specifications, fail-safe operation of the receiver under fault conditions, and other configurations issues such as multi-receiver operation. The ANSI/TIA/EIA-644 standard was approved in November 1995. National Semiconductor held the editor position for this standard.

The other LVDS standard is from an IEEE project. This standard came out of an effort to develop a standard for purposes such as linking processors in a multiprocessing system or grouping workstations into a cluster. This Scalable Coherent Interface (SCI) program originally specified a differential ECL interface that provided the high data rates required but did not address power concerns or integration.

The low-power SCI-LVDS standard was later defined as a subset of SCI and is specified in the **IEEE 1596.3** standard. SCI-LVDS specifies also specifies signaling levels (electrical specifications) similar to the ANSI/TIA/EIA-644 standard for the high-speed/low-power SCI physical layer interface. The standard also defines the encoding for packet switching used in SCI data transfers. The IEEE 1596.3 standard was approved in March 1996. National Semiconductor chaired this standardization committee.

In the interest of promoting a wider standard, no specific process technology, medium, or power supply voltages are defined by either standard. This means that LVDS can be implemented in CMOS, GaAs or other applicable technologies, migrate from 5V to 3.3V to sub-3V supplies, and transmit over PCB or cable thereby serving a broad range of applications.

1.2.4 A Quick Comparison

Parameter	RS-422	PECL	LVDS
Differential Driver Output Voltage	±2-5 V	±600-1,000 mV	±250-450 mV
Receiver Input Threshold	±200 mV	±200-300 mV	±100 mV
Data Rate	<30 Mbps	>400 Mbps	>400 Mbps

Parameter (Based on DS90C031/2)	RS-422	PECL	LVDS
Supply Current Quad Driver (no load, static)	60mA	32-65mA (Max.)	3.0mA
Prop. Delay of Driver	11ns (Max.)	4.5ns (Max.)	3.0ns (Max.)
Prop. Delay of Receiver	30ns (Max.)	7.0ns (Max.)	5.0ns (Max.)
Supply Current Quad Receiver (no load, static)	23mA (Max.)	40mA (Max.)	10mA (Max.)
Skew (Driver or Receiver)	N/A	500ps	400ps

The chart above compares LVDS signaling levels with those of PECL and shows that LVDS has half the voltage swing of PECL. LVDS swings are 1/10 of traditional TTL/CMOS and RS-422 levels. Another voltage characteristic of LVDS is that the drivers and receivers do not depend on a specific power supply, such as 5V. Therefore, LVDS has an easy migration path to lower supply voltages such as 3.3V or even 2.5V, while still maintaining the same signaling levels and performance. In contrast, technologies such as ECL or PECL have a greater dependence on the supply voltage, which make it difficult to migrate systems utilizing these technologies to lower supply voltages.

1.2.5 Easy Termination

Whether the LVDS transmission medium consists of a cable or controlled impedance traces on a printed circuit board, the transmission medium must be terminated to its characteristic differential impedance to complete the current loop and terminate high speed signals. If the medium is not properly terminated, signals reflect from the end of the cable or trace and interfere with succeeding signals. Proper termination also reduces unwanted electromagnetic emissions.

To prevent reflections, LVDS requires a terminating resistor of 100Ω ± 20Ω that is matched to the actual cable or PCB traces. This resistor completes the current loop and properly terminates the signal. This resistor is placed across the differential signal lines as close as possible to the receiver input . With this termination, an LVDS driver (DS90C031) can drive a twisted pair wire (e.g. SCSI cable) over 10m at speeds in excess of 155.5Mbps (77.7MHz). The real limitation on speed is two fold: 1) how fast TTL data can be delivered to the driver, 2) bandwidth performance of the selected media (cable). In the case of LVDS drivers like the DS90C031, its speed is limited by how fast the TTL data can be delivered to the driver. (National's Channel Link devices capitalize on the speed mismatch between TTL and LVDS by serializing the TTL data into a narrower LVDS data stream — more about this later.)

The simplicity of the LVDS termination scheme makes it easy to implement in most applications. ECL and PECL can require more complex termination than the one-resistor solution for LVDS. PECL drivers commonly require 220Ω pull down resistors from each driver output, along with 100Ωs across the receiver input.

1.2.6 Saving Power

LVDS technology saves power in several important ways. The power dissipated by the load (the 100Ω termination resistor) is a mere 1.2mW. In comparison, an RS-422 driver typically delivers 3V across a 100Ω termination, for 90mW power consumption — 75 times more than LVDS. Similarly, LVDS devices require roughly one-tenth the power supply current of PECL/ECL devices.

Aside from the power dissipated in the load and static I_{CC} current, LVDS also lowers system power through its CMOS current-mode driver design. This design greatly reduces the frequency component of I_{CC}. The I_{CC} vs. Frequency plot for LVDS is virtually flat between 10MHz and 100MHz for the quad devices (<50mA total for driver+receiver at 100MHz). Compare this to TTL/CMOS transceivers whose dynamic power consumption increases exponentially with frequency.

1.2.7 Fail-Safe Feature

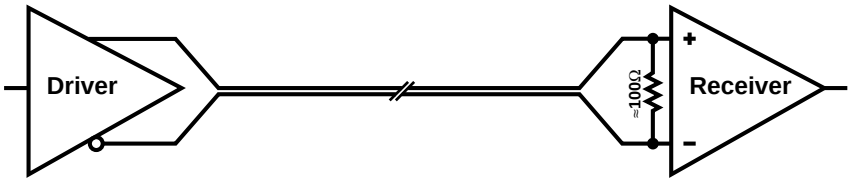
To help ensure reliability, LVDS receivers have a fail-safe feature that guarantees the output to be in a known logic state (HIGH) under certain fault conditions. These conditions include open, shorted, or terminated receiver inputs.

If the driver loses power, is disabled or is removed from the line, while the receiver stays powered on with inputs terminated, the receiver output remains in a known state with the fail-safe feature.

If LVDS receivers did not have the fail-safe feature and one of the fault conditions occurred, any external noise above the receiver thresholds could trigger the output and cause an error. A receiver without fail-safe could even go into oscillation under certain fault conditions. The fail-safe features ensures that the receiver output will be a HIGH — rather than an unknown state — under fault conditions.

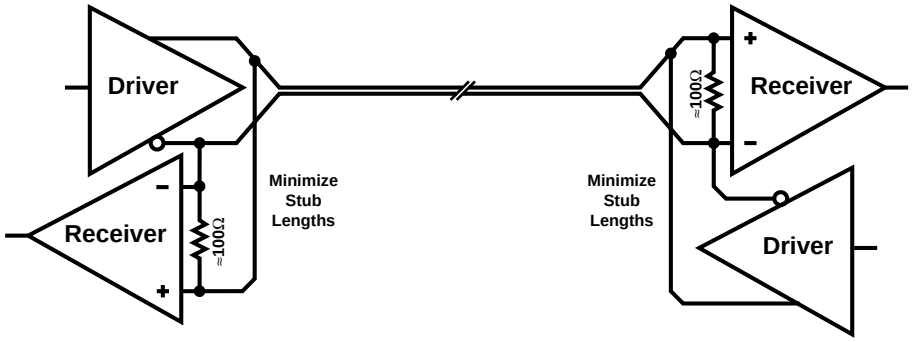
With the fault conditions accommodated internal to the receiver, designers do not need to include the external biasing resistors required by other technologies. This LVDS advantage saves valuable board space, cost, and design headaches.

1.2.8 LVDS Configurations

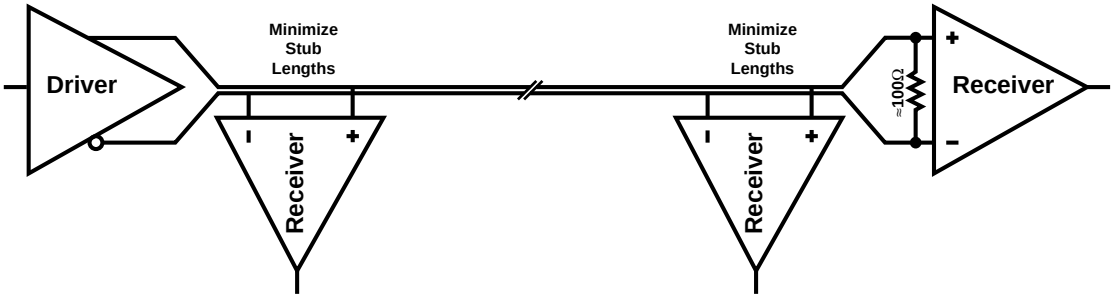


Point-to-point configuration.

Although LVDS drivers and receivers are typically used in a point-to-point arrangement (above), other topologies are possible. The configuration shown next allows bi-directional communication over a single twisted pair. Data can flow in only one direction at a time. The requirement for two terminating resistors reduces the signal (and thus the differential noise margin), so this configuration should be considered only where noise is low and transmission distance is short (≤10m).



Bi-directional half-duplex configuration.



Multidrop configuration.

A multidrop configuration can also be used if transmission distance is short and stub lengths are less than 12mm (<7mm is recommended). Dedicated point-to-point links are still the preferred solution. LVDS has many advantages that make it likely to become the next data transmission standard for data rates at and above 100Mbps for distances around 10m or less. In this role, LVDS will far exceed the 20Kbps to 30Mbps rates of the RS-232, RS-422, and RS-485 standards.

1.3.0 SAVE MONEY TOO

LVDS can save money in several important ways:

1) National's LVDS solutions are inexpensive CMOS implementations.

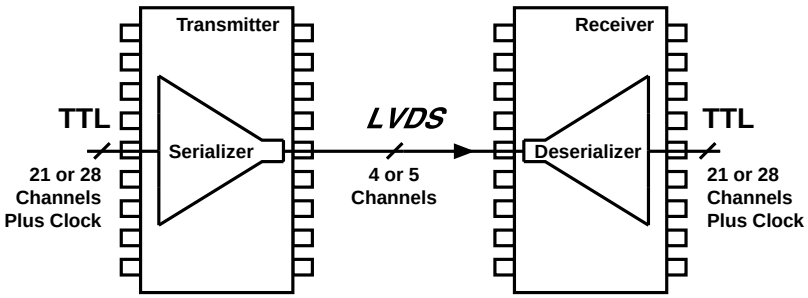
2) High performance can be achieved using low cost, off-the-shelf CAT3 cable and connectors.

3) LVDS consumes very little power, so power supplies, fans, etc. can be reduced or eliminated.

4) LVDS is a low noise producing, noise tolerant technology power supply and EMI noise headaches are greatly minimized.

5) LVDS transceivers are relatively inexpensive and can also be integrated around digital cores.

6) Since LVDS can move data so much faster than TTL, multiple TTL signals can be serialized or muxed into a single LVDS channel, reducing board, connector, and cable costs. National's family of Channel Link devices do just that. A channel link transmitter takes 21 or 28 bits of TTL data and converts it to 4 or 5 LVDS channels. These 4 or 5 channels of LVDS can then be routed across controlled impedance PCB traces or cable to the receiver which converts the data back to TTL.



National's Channel Link chipsets convert a TTL bus into a compact LVDS data stream and then back to TTL.

The conversion of a wide TTL bus to a few LVDS channels using Channel Link can substantially lower the power required to move the data, reduce noise and EMI concerns, and dramatically cut the size and number of PCB layers, connector pins, and cable conductors. In fact in most cases, the PCB, cable, and connector cost savings greatly overshadow any additional silicon costs. Smaller PCBs, cables, and connectors also result in a much more ergonomic (user-friendly) system.

1.4.0 LVDS APPLICATIONS

The high speed and low power/noise/cost benefits of LVDS broaden the scope of LVDS applications far beyond those for traditional technologies. Here are some examples:

PC/Computing	Telecom/Datacom	Consumer/Commercial
Flat panel displays	Switches	Home/commercial video links
Monitor link	Add/drop multiplexers	Set top boxes
SCI processor interconnect	Hubs	In-flight entertainment
Printer engine links	Routers	Game displays/controls
Digital Copiers		
System clustering	(Box-to-box & rack-to-rack)	
Multimedia peripheral links		

1.5.0 NATIONAL'S WIDE RANGE OF LVDS SOLUTIONS

National Semiconductor offers LVDS technology in several forms. For example, National's 5V DS90C031/DS90C032 and 3V DS90LV031/DS90LV032 quad line driver/receiver devices implement LVDS technology in discrete packages for general-purpose use. This family of basic line drivers and receivers also contains singles, duals and transceivers.

For the specialized task of connecting laptop and notebook computers to their high-resolution LCD screens, National offers the Flat Panel Display Link (FPD-Link) LVDS interface devices. These parts make it practical for portable computers to take advantage of the same high screen resolutions used in CRT-based desktop PCs.

Another more generalized use of LVDS is in the National Channel Link family which can take 21 or 28-bits of TTL data and convert it to 3 or 4 channels of LVDS plus clock. These devices provide fast data pipes (up to 1.84Gbps throughput) and are well suited for high-speed network hubs or routers applications or anywhere a low cost high speed link is needed. Their serializing nature provides an overall savings to system cost as cable and connector physical size and cost are greatly reduced.

1.6.0 CONCLUSION

National's LVDS technology solutions eliminate the trade-offs in speed, power, noise, and cost for high performance data transmission applications. In doing so, LVDS not only achieves great benefits in existing applications, but opens the door to many new ones.