Signal Integrity and Validation of National's Bus LVDS (BLVDS) Technology in Heavily Loaded Backplanes

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26 May, 1998

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1 Introduction

The feasibility of designing a 100+ MHz/200+ Mbps differential multi-point backplane has been demonstrated with the use of the new National Semiconductor Corporation Bus Low Voltage Differential Signaling (Bus LVDS) family. This paper presents the results of the BLVDS design and performance analysis and provides system backplane interconnect designers manufacturable design guidelines. The guidelines are given in terms of suggested stub lengths, PCB impedances, termination resistor values and other design parameters. This data provides the design choices leading to straightforward implementations of 100+ MHz multi-point backplanes. The attainment of this level of performance will permit an immediate reduction in the complexity of high-speed, high-bandwidth system interconnects.

The advantages of multi-point backplane buses have been recognized for many years as offering a low cost bi-directional crossbar. But, the performance data rate has suffered because of the high driver current demands in single-ended designs. National has achieved a fundamental breakthrough with the BLVDS family by offering CMOS differential driver/receiver solutions with low current drive requirements and high data rate performance for multi-point backplane design applications.

NESA completed a series of measurements and analyses of National's prototype 20-slot, 0.8" pitch test BLVDS backplane, demonstrating the high performance potential of the BLVDS concept. The test backplane offered a number of signal paths, permitting the analysis of heavily loaded full-length 20-slot designs as well as 11-slot half-length loaded designs and a lightly loaded architecture. The modeled backplane was constructed of standard FR-4 material and implemented microstrip (surface trace) geometries. Standard VME-style 3-row 96-pin DIN connectors, with the center B-row grounded, were used; twenty differential (edge-coupled, 85 – 95 Ω) pairs were distributed to adjacent pin pairs across the A and C rows. The results and discussions from these studies are summarized in the appendix.

This paper discusses in-depth system SPICE simulation analyses which are used to optimize the design and performance of a heavily-loaded BLVDS multi-point backplane to achieve maximum noise margin and data rate performance. Over a number of years, NESA has developed proprietary methods of modeling single-ended and differential TDR and TDT measurements in SPICE that NESA calls "passive signal integrity analysis" methodologies. Using these methods, NESA has demonstrated that by balancing the etch impedance and termination effects, it is possible to optimize BLVDS backplane designs to maximize the noise margins at every slot.

With the development of an optimum passive backplane design, a number of “active simulations” using the National BLVDS driver/receiver models were run in order to validate the “optimum design” and to determine the BLVDS performance boundaries. The attainment of 200 Mbps simulated data transfers on a fully populated backplane has been demonstrated. The advantages in the utilization of low power, low propagation delay differential transceiver parts for high-performance backplane designs are formidable.

2 Description and SPICE Simulation of the Prototype NSC BLVDS Backplane Configuration

NESA began investigations into optimizing the BLVDS backplane design by first studying an existing National design. Figure 1 shows the prototype BLVDS backplane configuration. Following lab measurement work, backplane interconnect SPICE models were built which reflected the physical test case. Included in the SPICE files were active device models, standard DIN connector models, signal transmission line models (using lossy Hspice w-element models), termination and other passive components. For these active simulations, SPICE models for the National BLVDS devices were used for the driver and receiver. All SPICE simulations were completed using Avanti Corporation’s Star-Hspice® simulator.

The CMOS differential design of these parts offers low voltage swing, lower termination power and reduced EMI emissions due to the far lower common-mode current components that differential technology offers. The BLVDS devices are 3.3 V transceiver parts capable of sinking 8.5 mA per differential pair. The parts are designed for a 270 mV swing with a +/- 100 mV receiver threshold region. The output is designed to provide a balanced impedance with light bus loading (5 pF typical).

The backplane impedance was originally designed using two closely spaced 50 Ω single-ended (SE) lines, with target differential impedances of 85 Ω and 95 Ω. Taking the coupling between the traces in a differential pair into account, the trace differential impedance was measured and analyzed to be in

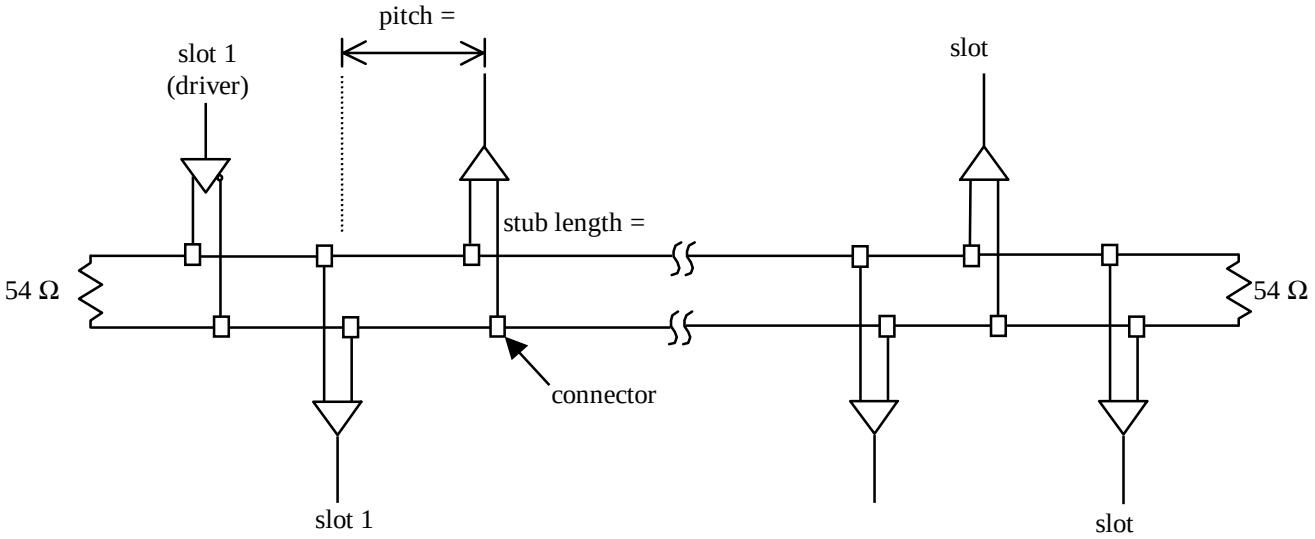

Figure 1. - The National BLVDS backplane; Z_0 = 50 Ohms (SE), termination resistor = 54 Ohms at each end.

the high-80's Ω to mid-90's Ω. End-point termination was achieved through the use of 54 Ω differential resistive terminations on each end of the bus.

In this set of active simulations, data was clocked over the backplane at 66, 100, 156 and 200 MHz clock rates. The measured data transmission rates were 66, 100 and 156 Mbps. The simulated waveform outputs were then compared and correlated to the measurements made by National's engineers using prototype silicon. The 200 Mbps simulation demonstrated the use of SPICE in predicting performance at higher data rates based on a validated backplane model. Typical simulated 100 Mbps waveforms at each receiver are shown in Figure 2.

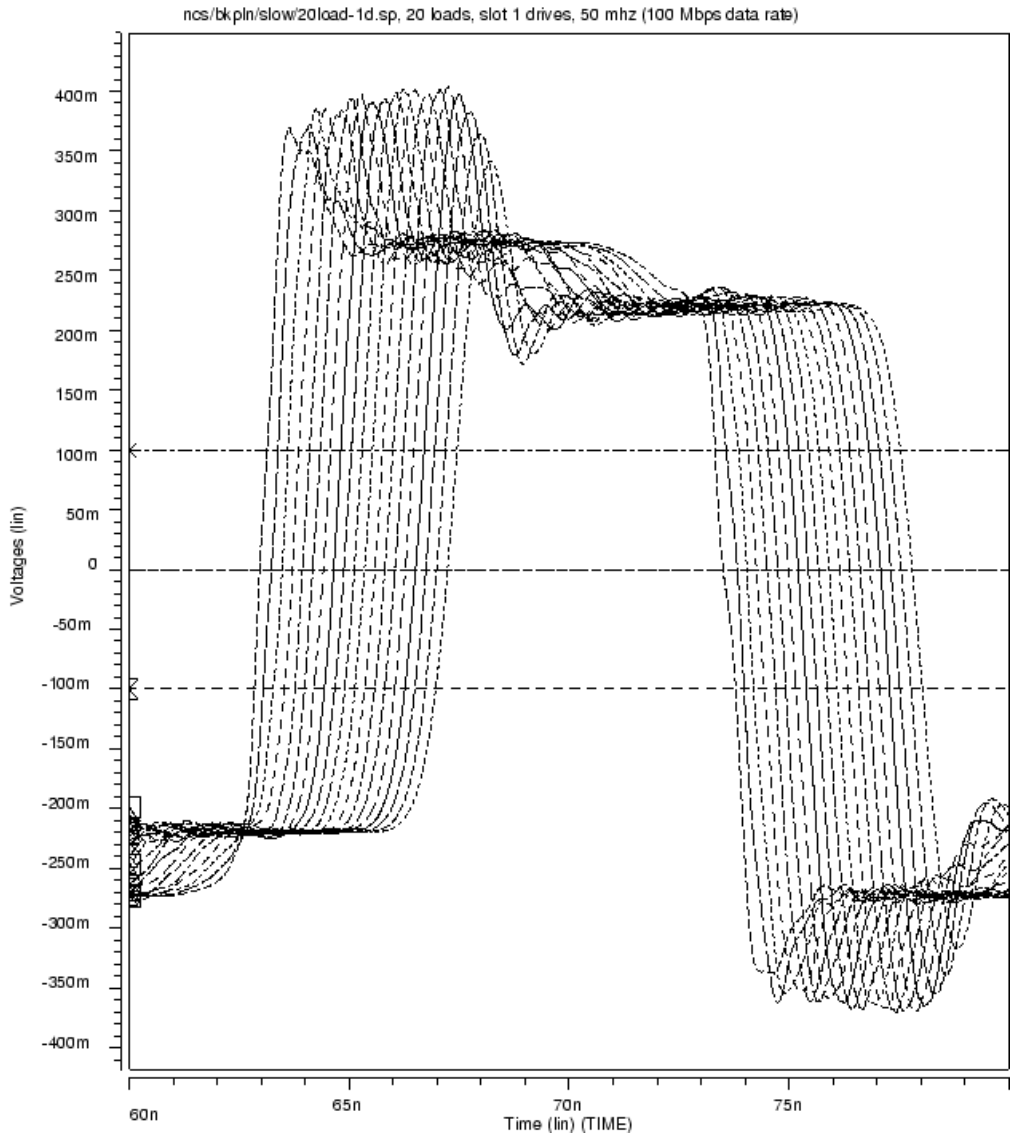

Figure 2 – 20-slot BLVDS backplane simulation results (receiver input waveforms).

In this figure, the simulation results for the National 20-slot BLVDS backplane are shown at the receiver pin. The receiver thresholds of +/- 100 mV are shown on the plot as dotted lines. The input

waveforms have very clean edges through the threshold region showing no evidence of "porching" or other reflections which could lead to meta-stable switching performance.

Upon closer examination of the voltage at the receivers, the noise margin is seen to be approximately 80 mV, which in some instances may not be sufficient. Loss of noise margin is usually associated with low effective impedance; that is, the impedance the driver "sees" with the plug-in cards inserted is lower than optimum. There is also a static loss of noise margin due to the low termination impedance of 27 Ω when both 54 Ω termination resistors are factored into the signal response. The overshoot and undershoot are slightly bigger than those seen in the measurements for this case and are thought to be due to the faster rise/fall times in the SPICE models (0.5 – 1.0 ns) vs. the rise/fall times (1.0 – 1.5ns) exhibited by the prototype parts. In general, the backplane simulations show that the National BLVDS family is well suited to drive a 20-slot differential backplane while meeting reasonable receiver noise margin specifications. It was felt however, that the noise margin performance could be optimized with little or no cost impact on the backplane design.

The remaining portions of this paper focus on how to improve the BLVDS multi-point bus noise margin performance by optimizing the backplane design parameters through passive SPICE simulations and related analyses. This is followed by a presentation and discussion of the "active" simulation results which were used to validate the optimized BLVDS multi-point backplane configuration.

3 Optimizing a BLVDS Backplane through "Passive Signal Integrity" Simulations

In general, multi-point backplane performance is strongly affected by a number of factors including: module stub lengths, the effective bus impedance, the backplane driver technology (edge rates, device/package load), and the selected termination values. The plug-in card stub length, the raw trace differential impedance, the connector loads, and the device loads all affect the effective backplane impedance. The stubs, connectors, and device loads all contribute to the per unit capacitive loading of the bus, which in turn lowers the impedance; this "loaded" impedance is termed the effective impedance of the bus. The effect of capacitive loading on a differential trace can be approximated by the formula for the effective differential impedance:

$$Z_{diff}^{effective} = Z_{diff} * \sqrt{\frac{C_o}{C_o + N / \ell * C_L}} \qquad (1)$$

where: C_o is the unit capacitance of the trace, the trace is "ℓ" (length) long, and N is the total number of capacitive loads on the trace length, each of capacitance C_L. Thus, $N / \ell * C_L$ is the per unit incremental loading capacitance.

With a spacing of 0.8", the connector loading is equivalent to 2.5 to 3.75 pF/in and the unit capacitance of the trace is in the 2 - 3 pF/in range. This extra loading capacitance will reduce the impedance to approximately 0.7 Z_{diff}. Thus, the effective transmission line impedance is seen to be

much lower for the 20-slot heavily loaded traces as compared to, for example, the lightly loaded 4 slot traces (refer to the appendix). The voltage variations due to reflections from the plug-in card stubs and the end point terminations are also affected by the signal rise time, which in turn depends on the BLVDS devices.

NESA has developed over a number of years an accurate virtual differential TDR simulation technique. With this simulation tool, the effective impedance of a fully loaded (i.e., all slots populated) BLVDS backplane can be determined, independent of the driver/receiver semiconductor technology. Using these means, the BLVDS device performance can be optimized while also determining how PCB design limitations can affect the bus design.

A 20-slot BLVDS backplane SPICE model including the backplane half of the connectors was constructed. SPICE models were then constructed for the cards as well to permit the virtual TDR measurements in order to account for the plug-in card loading including the plug-in card half of the connector. Therefore, when a card was plugged into the backplane, the full connector model was included. In a fully loaded system simulation, all 20 card slots were populated as in Figure 1. The BLVDS device in the selected "driver" plug-in card was turned off ("tri-stated"). All of the receivers on the remaining logic cards were present to account for the input receiver parasitic capacitance. Since there are no active devices in these types of TDR-based investigations, they are usually termed "passive". In these passive TDR simulations, the termination resistors were removed for probing and the differential TDR probing point was positioned at one end of backplane.

3.1 Effect of Module Stub Length

In NESA's backplane design experience, the stub lengths on the logic cards are very important to the signal integrity of a multi-point backplane bus. The maximum allowable length of the stubs depends on the specific semiconductor package footprint and whether two-sided surface mount technology for active devices can be utilized. It is well known that if the stub length between the connector and I/O pin is too long, it can substantially reduce the effective backplane impedance, thereby raising the driver current. Long stubs also cause significant local reflections due to the capacitive impedance mismatch.

In this study, the stub lengths on the plug-in cards were set to 0.5", 1.0", 1.5" and 2.0" respectively for the TDR simulations, with the differential raw PCB transmission line impedance set to $Z_{diff.} = 100\ \Omega$ to begin the optimization study. Figure 3 shows the results of changing the stub length from 0.5" to a maximum length of 2". The effect on the loaded impedance is quite striking as is the increased unit propagation delay.

The rise time of the TDR generator incident step also affects the measurement resolution. The smaller the TDR rise time, the higher the measurement resolution and the more local reflections are seen. Since typical BLVDS signal rise times are in the 0.5 – 1.0 ns range, simulations of the TDR response were made with the rise times set to these values. Figure 3 shows the TDR simulation results for a 0.5ns TDR rise time.

With 0.5” stub lengths, the average effective differential impedance is about 67 Ω and the impedance discontinuity min/max is roughly 60 Ω and 73 Ω. With 2” stubs, the average effective impedance drops significantly to 50 Ω and the impedance discontinuity min/max varies between 33 Ω to 65 Ω. The reflections caused by the logic card capacitive loading are roughly proportional to the length of stubs. However, there is an inverse relationship between stub length and the effective backplane differential impedance.

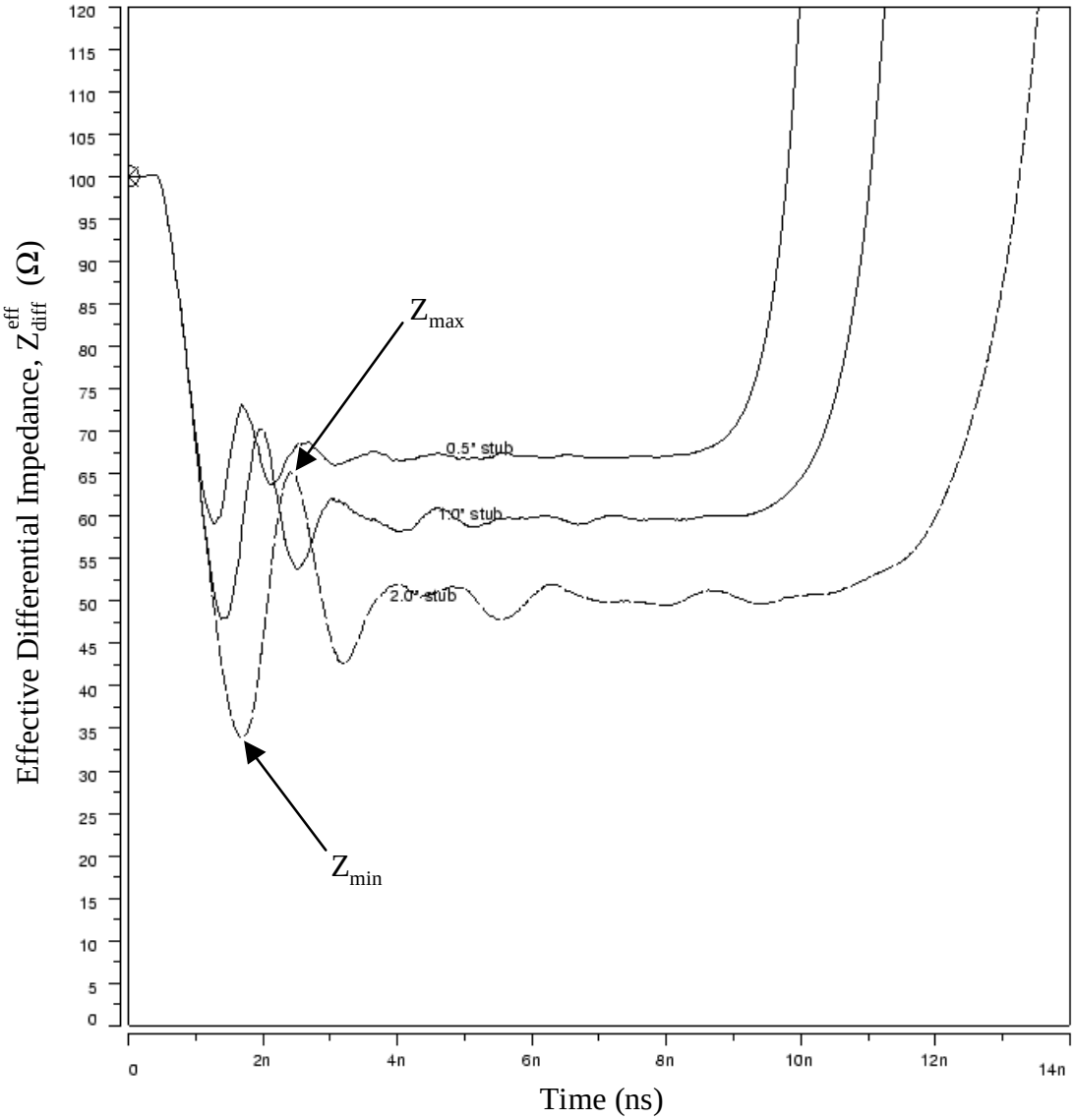

Figure 3. - TDR simulation for a fully loaded 20-slot BLVDS backplane, TDR rise time = 0.5 ns, PCB differential etch impedance = 100Ω

3.2 Effect of Raw (Bare Board) Impedance

In order to increase the effective loaded impedance and reduce the impedance variations, the raw (i.e., bare board) differential impedance should be as high as can be reliably manufactured and the plug-in card stubs must be kept as short as possible.

If the average effective backplane differential impedance Z_{eff} is plotted with its maximum values Z_{max} and its minimum values Z_{min}, interesting conclusions can be reached regarding "optimum designs". The results for $Z_{diff.}$ = 100 Ω raw transmission line impedance and 0.5 ns TDR rise time are shown in Figure 4. Even with as little as 0.5" of stub length, the effective differential impedance is reduced to 67 Ω which is more than 30% lower than 100 Ω raw etch backplane differential impedance. As the stub length becomes longer, the effective differential impedance gets lower, and the variation between Z_{max} and Z_{min} gets bigger! These two factors taken together will reduce the backplane bit rate performance.

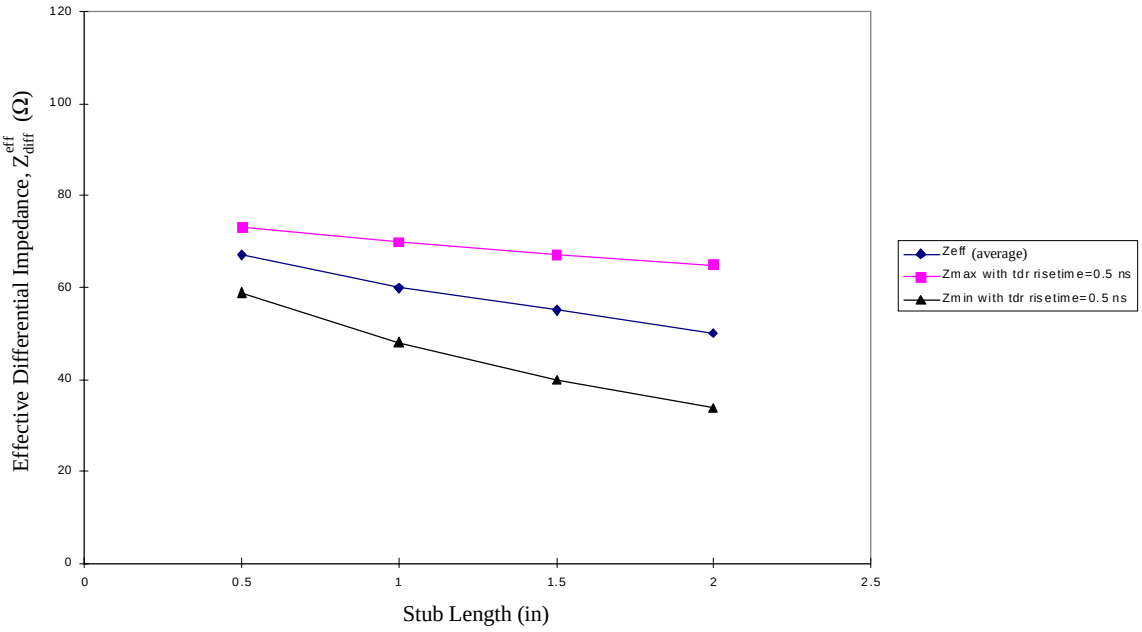

Figure 4. – Differential Impedance (min, max and effective) vs. Stub Length For PCB raw etch Z_{diff} = 100 Ω and TDR rise time = 0.5ns.

In order to raise the effective ("loaded") differential impedance (refer to equation 1), the raw etch differential impedance was raised to the maximum practically possible with a stripline design, namely $Z_{diff.}$ = 130 Ω (although higher differential impedances are possible using microstrip, some designs must use stripline – stripline use also allows for more flexibility in stackup designs). The backplane model was updated with this new PCB impedance value and the TDR of the backplane was re-simulated. Figure 5 shows a similar set of data as shown in Figure 4, with the higher bare board Z_{diff}.

As expected, the effective differential impedance is higher. With a stub length of 0.5", the effective differential impedance is about 84 Ω. Even with 1" of stub length, the effective differential impedance remains relatively high (76 Ω). These changes will reduce the device current by ~25% and increase

the logic swing. It was shown earlier that when the plug-in card stub length is increased to 2", the effective differential impedance is about 50 Ω with a standard raw differential impedance of 100 Ω. Even with a raw impedance of $Z_{diff.}$ = 130 Ω, the effective differential impedance is still low at approximately 64 Ω. And the reflections from the plug-in cards, which are proportional to the impedance variation, remain very large. So, 2" of stub on the logic cards is clearly not acceptable. It should be reiterated that the stub lengths on the cards be limited to around 1" or as short as possible. It is important to note that the change in PCB raw impedance does not significantly affect the Z_{min} and Z_{max} variations. A reduction in rise time (i.e. slowing the edge rate) has a very noticeable effect on these parameters.

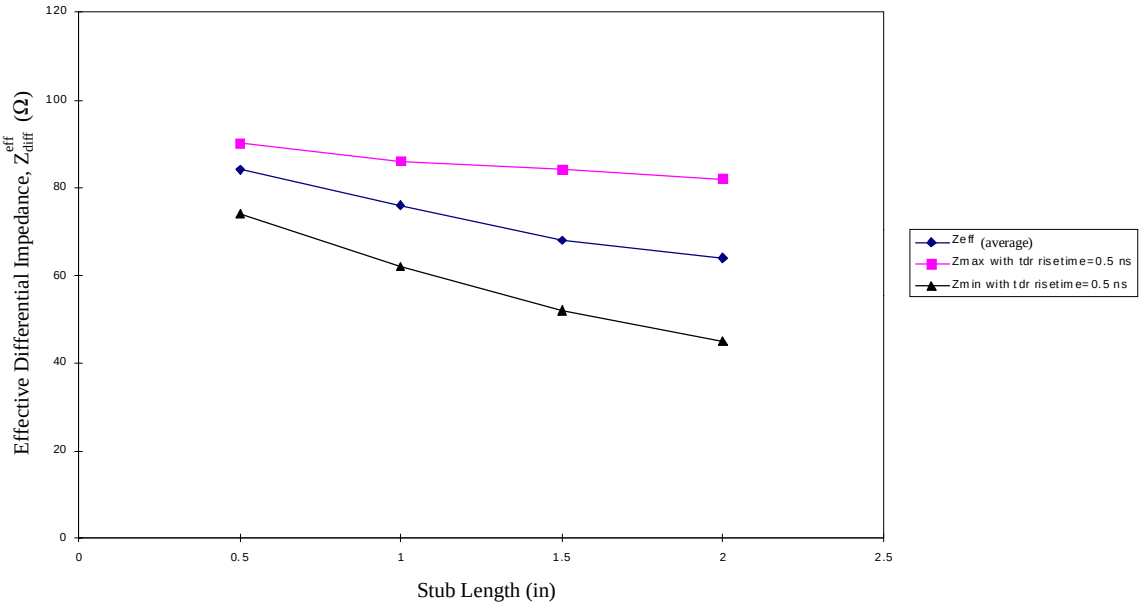

Figure 5. – Effective Diff. Impedance (min, max and average) vs. Stub Length For PCB raw etch Z_{diff} = 130 Ω and TDR rise time = 0.5ns.

3.3 Effect of Rise Time

The effects of rise time on overall signal integrity have also been investigated. The TDR rise time was slowed from 0.5 ns to 1.0 ns to provide for comparison data. The slowing of the incident rise time has an averaging effect on the TDR profile; the minimum and maximum impedance peaks are much reduced with the slower risetime, while the average effective impedance remains the same. This is clearly shown in the data of Table 1. Additionally, if the rise time can be slowed down or controlled to 1 ns or slower, the reflections from the connectors and plug-in cards will be much smaller and more of the logic cycle will be usable. Table 1 presents data for the average loaded (effective), minimum, and maximum impedance under various conditions. This data summarizes how the backplane bus impedance, and, therefore, the signal integrity, can be affected in response to changes in stub length, raw impedance, and signal rise time.

Effective Diff. Impedance (Ω)	0.5" stub			1.0" stub			1.5" stub			2.0" stub		
(Z_{diff} & TDR rise time varied)	Z_{eff}	Z_{max}	Z_{min}	Z_{eff}	Z_{max}	Z_{min}	Z_{eff}	Z_{max}	Z_{min}	Z_{eff}	Z_{max}	Z_{min}
$Z_{diff.}$=100 Ω with 0.5 ns rise time	67	73	59	60	70	48	55	67	40	50	65	34
$Z_{diff.}$=100 Ω with 1.0 ns rise time	67	68	67	60	60	57	55	56	50	50	55	43
$Z_{diff.}$=130 Ω with 0.5 ns rise time	84	90	74	76	86	62	68	84	52	63	82	45
$Z_{diff.}$=130 Ω with 1.0 ns rise time	83.5	83	84	75	76	72	68	72	64	64	68	56

Table 1. Effective backplane differential impedance for a fully loaded 20-slot BLVDS backplane vs. stub length (Zdiff and Trise varied).

Using TDT measurement techniques, the measured incident risetime and the measured transmitted waveform risetime can be used to determine approximate interconnect bandwidth. The effective risetime bandwidth of a digital interconnect can be expressed in what we at NESA call the RMS Risetime Loss, which is defined as:

$$\tau^{RMS}{}_{r_{loss}} = \sqrt{\tau^2{}_{r_{out}} - \tau^2{}_{r_{in}}} \qquad (2)$$

This "square root of the difference of the squares" number gives an indication of the fastest risetime that can be sent down the backplane. As in the case of the effective impedance discussed earlier, the transmitted waveform's risetime (and, therefore, the propagation delay) is affected by the per unit capacitive loading of the bus; the affect of this loading is to slow the edge which in turn decreases the apparent bandwidth. A good approximation of the typically sited 3 dB bandwidth number can be determined by dividing 0.35 by the τ^{RMS} number. See the appendix for some sample TDT results.

3.4 Effect of Termination Value

Following the passive simulations, a number of active simulations were completed to investigate the role of the termination resistor values in the noise margin response. Active simulations (with operating driver and receiver models) were run with terminations of 54, 65, 80, 100 and 130 Ω at each end of the bus. The noise margin as a function of these termination resistor values is plotted in Figure 6 for 1" and 2" stub lengths. The simulations show that the noise margin is always better for shorter logic card stubs. It also shows that the 80 Ω termination resistor is the best value for a fully loaded backplane with $Z_{diff.}$ = 130 Ω. This optimized termination value agrees with that found with the NESA TDR predictor.

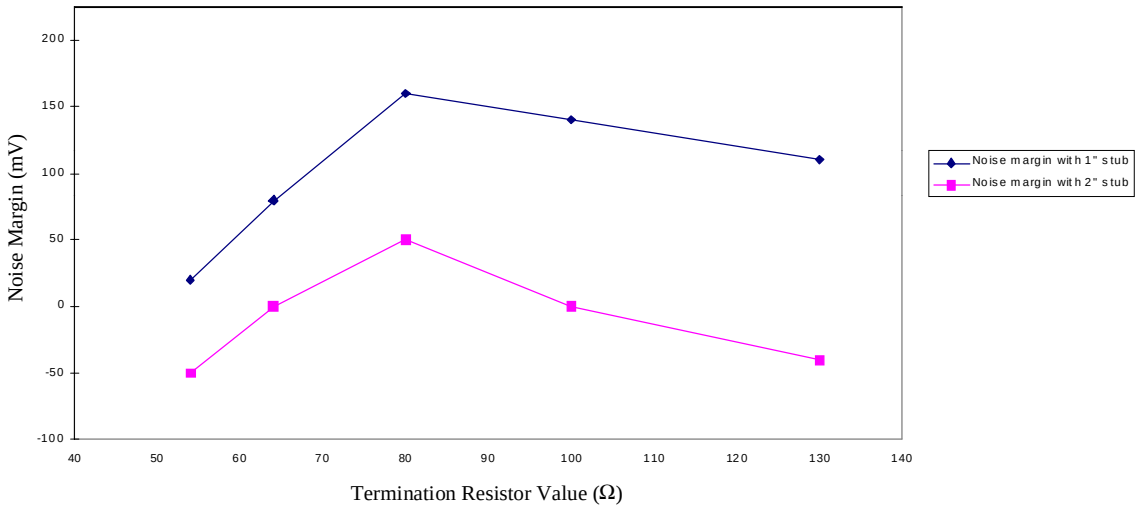

Figure 6. - Noise Margin vs Termination Resistance Value for Two Stub Lengths at 100 Mbps Data Rate (active simulation).

The optimized configuration provides an overall cleaner design for the multi-point BLVDS bus.

4 Optimized Multi-point BLVDS Backplane Interconnect Configuration

With the results of the analyses presented in this paper, an optimum backplane interconnect configuration can be recommended for a fully loaded 20-slot BLVDS backplane. An optimized configuration should have following parameter values:

1. Stub lengths should be limited 1” (or as small as possible) on the logic cards;
2. The recommended differential transmission line impedance, $Z_{diff.}$ is 130 Ω - either microstrip (edge-coupled) or stripline (edge- or broadside-coupled) can be implemented (see below for specific geometry examples);
3. A slower edge rate is preferred (trade-off with timing and data cycle considerations);
4. The termination resistor value should be closer to 80 Ω than the original 54 Ω on each end.

These parameters differ from the original backplane design parameters in the following manner: the PCB differential impedance has been raised to the highest practical value that can be achieved in stripline and the termination resistor values have been selected to match the loaded impedance of the backplane for a limited stub length of 1”. These are very easy changes to implement; controlling the rise time of the driver is less so, but this may be possible with discrete passive components if it is found to be critical.

The connector can be any of a number of standard backplane connectors with 0.1 in, 2.5 mm, or 2 mm pitch. For the speeds discuss in this paper, NESA generally recommends at least a 2:1 signal-to-ground ratio.

Specific geometry examples to reach goal impedance of 130 Ω differential:

Figure 7 describes a simple internal stripline geometry for an edge-coupled differential pair. For a reasonably spaced edge-coupled pair, the following dimensions will give approximately 130 Ω differential (73.5 Ω SE): W = 6 mils, S = 13 mils, and H = 16 mils. Standard FR-4 is assumed throughout with $\varepsilon_r \sim 4.5$. To reduce the dielectric thickness, the lines can be moved apart; for W = 6 mils, S = 18 mils, and H = 13 mils, the SE impedance is closer to 68.5 Ω to meet the 130 Ω differential. For reference, to reach approximately 100 Ω differential with 6 mil lines, S = H = 8 mils (SE impedance = 55 Ω).

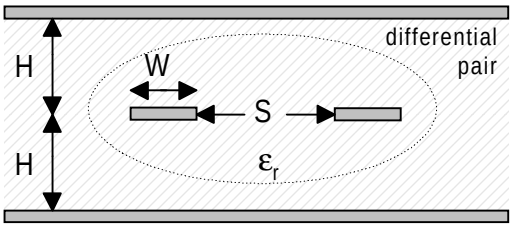

Figure 7 – Simple stripline differential pair geometry.

For a microstrip design using 6 mil line widths, S = H = 7 mils will give a SE impedance around 75 Ω and a differential impedance close to the desired 130 Ω (assumes $\varepsilon_r = 4.5$ and 1 mil of solder mask over the top).

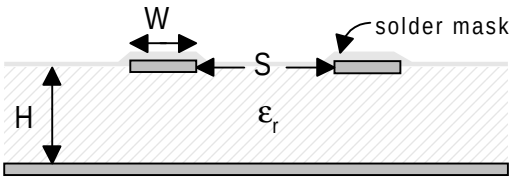

Figure 8 – Simple microstrip differential pair geometry.

4.1 Active Simulation Validation

In order to evaluate (and validate) the optimized set of parameters, new fully loaded active simulations were completed. As in the earlier simulations, the BLVDS driver was located in slot 1. The simulated receiver input waveforms are shown in Figure 9 and can be compared to their counterpart results shown in Figure 2.

Under the "optimized parameter" conditions, the backplane is well terminated and the reflections are reasonably small with respect to the overall signal swing. There is now little signal loss due to the terminations and the edges through the threshold region remain very clean. The overshoot and undershoot of the waveforms remain fairly large due to the fast rising and falling edges of the BLVDS signals through the connector pins. However, the available noise margins are greatly increased.

Compared to the minimum 80 mV margin of the current backplane design (see Figure 2), the noise margin of the optimized configuration is more than 150 mV. The static margin loss is not present due to the higher effective termination resistance of 40 Ω (two 80 Ω resistors in parallel), which in turn plays a role in maximizing the signal swing.

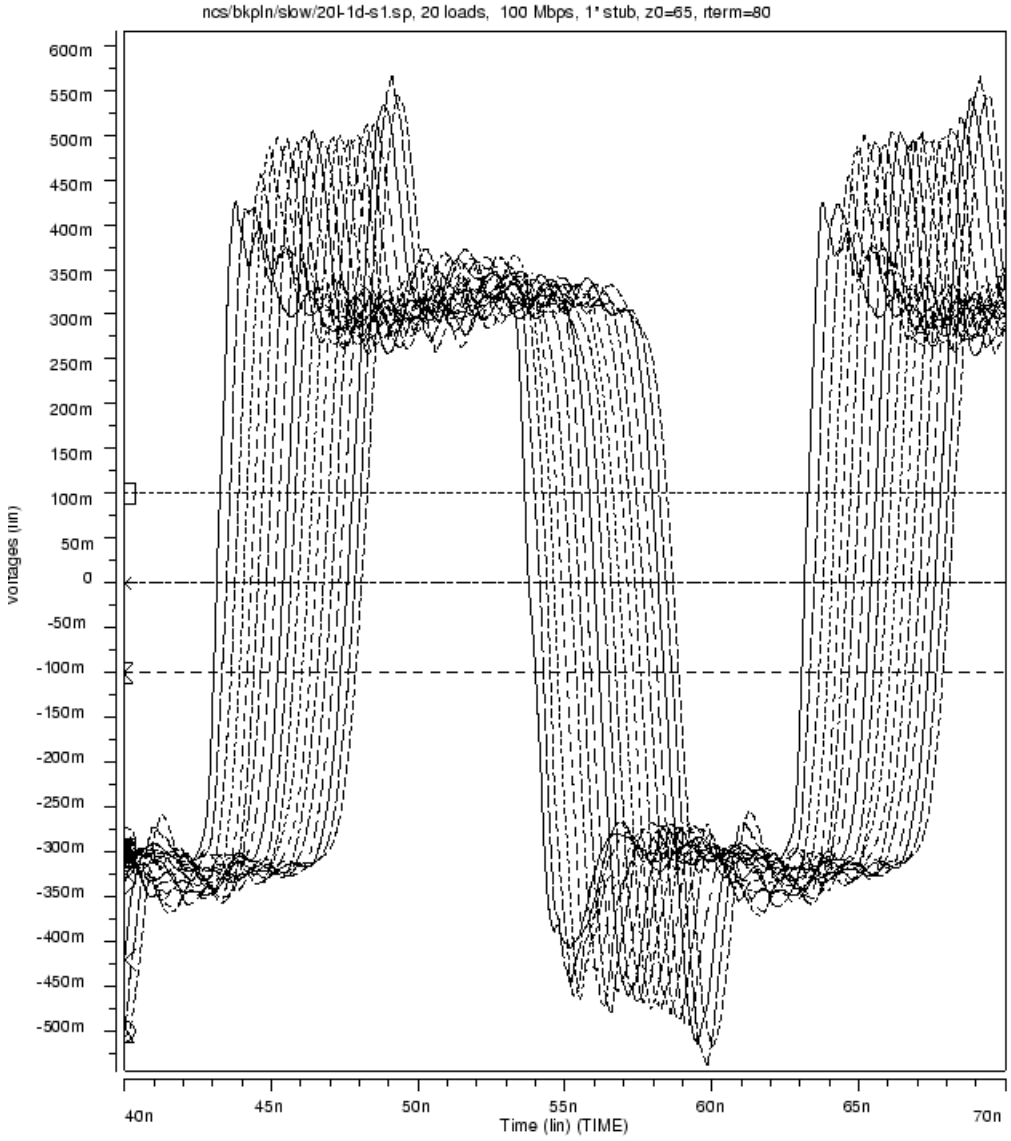

Figure 9. – BLVDS receiver input waveforms under "optimized parameter" conditions.

4.2 Backplane Performance versus Data Rate

Incorporating the optimized backplane parameters, the following simulation cases were run in order to measure the performance of the BLVDS interconnect:

1) A fully loaded 20-slot backplane, with slot 1 driving, and a data rate of 100 Mbps
2) A fully loaded 20-slot backplane, with slot 1 driving, and a data rate of 156 Mbps
3) A fully loaded 20-slot backplane, with slot 1 driving, and a data rate of 200 Mbps
4) A fully loaded 20-slot backplane, with slot 10 driving, and a data rate of 100 Mbps
5) A half loaded 20-slot backplane, with slot 10 driving, and a data rate of 100 Mbps

The half-loaded configuration had slots 1-10 loaded with slots 11-20 open. Noise margin results for the above-described cases are shown in Table 2 below. For all of the cases, the receiver input waveforms are very clean with substantial noise margins.

Optimized Backplane Configuration and Bit Rate	Drive Slot Location	Noise Margin (mV)
20-Slot, Fully Loaded – 100 Mbps	1	150
20-Slot, Fully Loaded – 156 Mbps	1	140
20-Slot, Fully Loaded – 200 Mbps	1	130
20-Slot, Fully Loaded – 100 Mbps	10	150
20-Slot, Half Loaded – 100 Mbps	10	170

Table 2 – Noise margin vs. data rate for several "optimized" BLVDS backplane simulations.

5 Summary and Conclusions

The National Bus LVDS proto-type backplane was measured and characterized with Time Domain Reflectometry (TDR) and Time Domain Transmission (TDT) techniques (see appendix). Based on the results of these measurements, an accurate SPICE model for a 20-slot, multi-point BLVDS backplane has been built and simulated. NESA-developed passive TDR SPICE simulations were used to determine optimum backplane and termination configuration. For high performance backplane operation at bit rates in excess of 100 MHz / 200 Mbps, the stub length on the plug-in cards should not exceed 1" if possible. The optimal value of the raw etch PCB differential impedance is Zdiff = 130Ω and the termination resistors should be 80Ω on each end in order to minimize reflections and maximize noise margin.

The validated SPICE simulations show that with the DS92LV010 BLVDS transceiver and the optimized design parameters presented in this paper, the Bus LVDS devices can operate in 20-slot multi-point backplane bus environments. The transmission data rate could be as high as 200 Mbps under those conditions. The attainment of this level of performance will permit an immediate reduction in the complexity of high-bandwidth system interconnects.

The advantages of a multi-point backplane buses have been recognized for many years as offering a low cost bi-directional crossbar. But, the performance data rate has suffered because of the high current single-ended drivers in technologies such as CMOS, TTL, GTL, BTL, etc.

National has achieved a fundamental breakthrough with the BLVDS family by offering CMOS differential driver/receiver solutions with low current drive requirements and high data rate performance for multi-point backplane design applications. In addition the device performance, BLVDS greatly reduces system complexity as it enhances and or supports the following: Bus LVDS simplifies and reduces complex termination design required by single-ended drivers to just 2 passive resistors. It also does not require special termination voltages and is powered from a common rail (3.3V or 5V). Adequate differential noise margins are provided, while the common mode range is greatly increased on the issue of noise rejection / tolerance. Noise generation is greatly reduce

through the use of current mode drivers, a small signal swing, differential data transmission, and advanced circuit design techniques. With low power dissipation, and a core CMOS process, integration of digital functions is now possible for optimized interface devices.

With the level of device performance achieved, and with the system advantages in power, flexible configurations, noise tolerance and even live insertion, high performance backplane design for bandwidth hungry applications is revolutionized.

About NESA, Inc.

High Performance Engineering and Design

Founded in 1973, North East Systems Associates, In., (NESA) provides a wide range of engineering services for customers requiring high performance designs. The Company specializes in getting clients to market quickly with competitive products. This is achieved through extensive design experience, strategic technology relationships and tight project management. Their client's success is NESA's primary goal.

NESA's clients include networking, telecommunications, computer, component and interconnect companies. Many of NESA's clients are start-ups or entrepreneurial divisions within larger corporations. They learn about NESA from engineering peers, attending technical conference where NESA staff is presenting, published technical papers and articles and from the Company's homepage at http://www.nesa.com.

"Right by design" is NESA's design methodology. This means one-pass designs that meet regulatory requirements the first time. NESA's design services include complete signal integrity analysis and system design, busses, backplanes, enclosures, power distribution, thermal analysis and regulatory compliance. Layout and routing, assembly and fabrication services can also be coordinated by the Company's engineering and business teams. In response to client requests, NESA offers a series of design seminars that focus on performance technology and proven methods of successfully implementing it into products. NESA's team has the proven ability to quickly turn design challenges into cost effective solutions for their clients.

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Appendix

A. Sample TDR/TDT Measurement Plots for the National BLVDS Backplane

B. Selected SPICE Simulation Results for BLVDS Backplane Designs

C. Clock Frequency vs. Duty Cycle

D. National Bus LVDS Plug-in Cards and Backplane Physical Description

A. Sample TDR/TDT Measurement Plots for the National BLVDS Backplane

Below are two TDR plots made on the National BLVDS backplane. Figure A1 shows the single-ended (SE) and differential impedance profile of the 20-slot bus with no cards inserted (backplane halves of connectors only). Figure A2 shows the same data for the 4-slot bus with two connectors on each end of the backplane. The more heavily loaded 20-slot bus shows a differential impedance of around 77 – 78 Ω while the lighter loaded 4-slot bus shows a differential impedance 20 Ω higher.

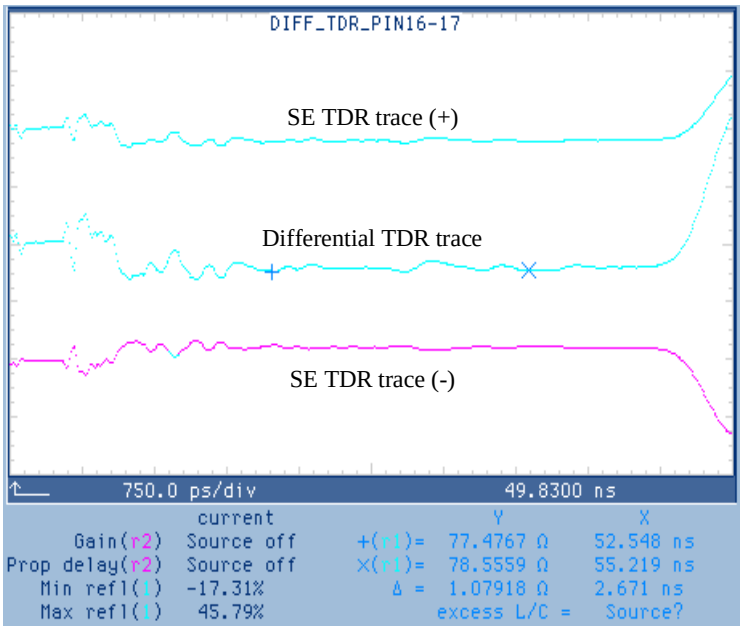


Figure A1 - Differential TDR measurement, 20-slot backplane.

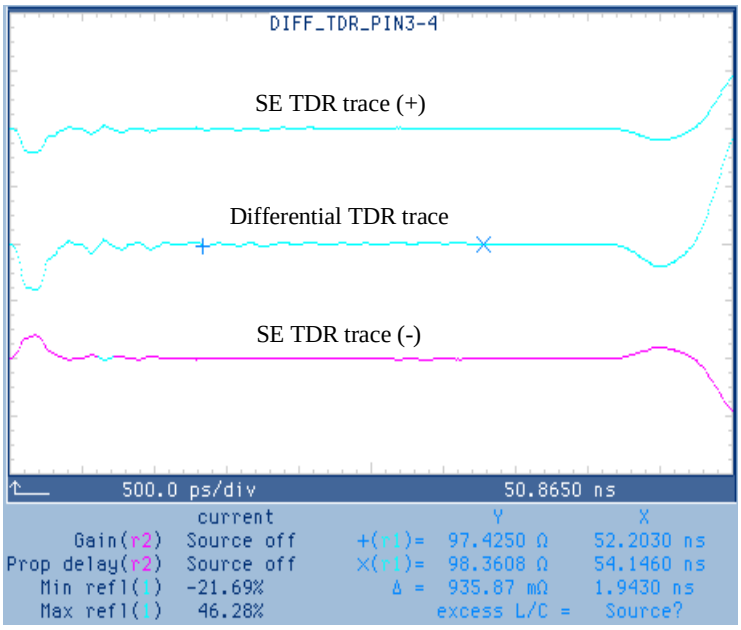


Figure A2 - Differential TDR measurement, 4-slot backplane.

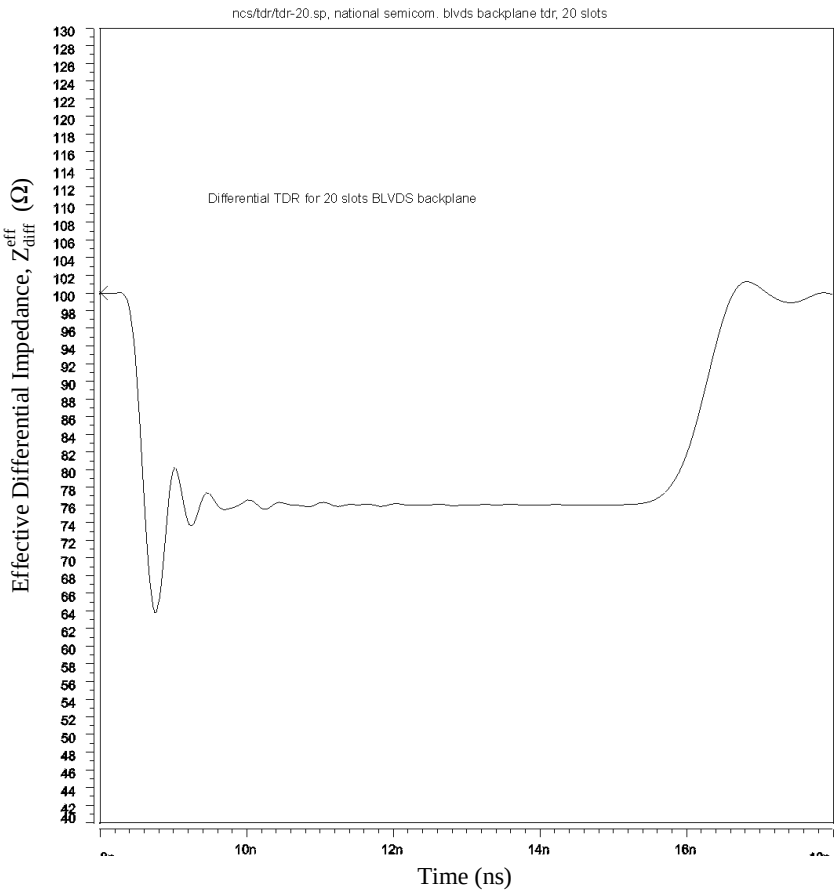
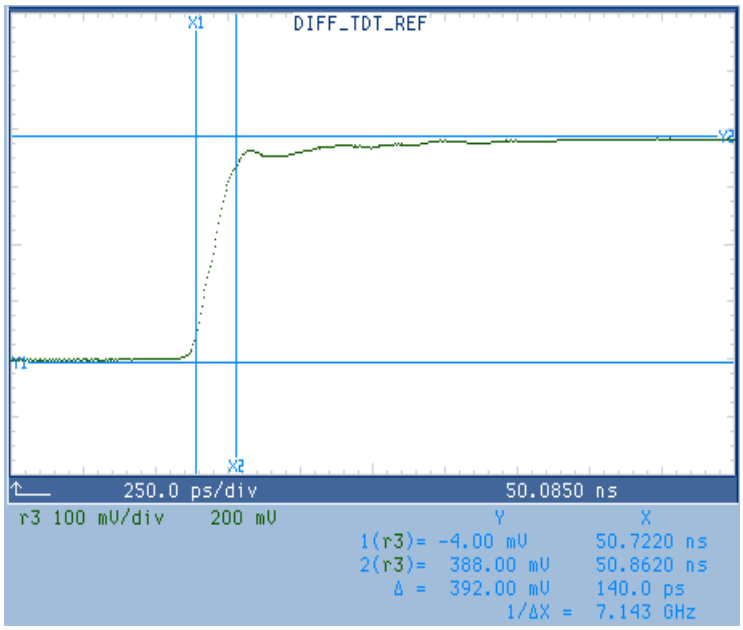


Figure A3 shows a simulated TDR profile for the 20-slot bus; this can be directly compared to Figure A-1 above. The simulation and measurement results agree that the impedance is roughly 78 Ω. Figure A3 shows a simulated TDR profile for the 20-slot bus; this can be directly compared to Figure A-1 above. The simulation and measurement results agree that the impedance is roughly 78 Ω.

Figure A3 – Simulated TDR for the 20-slot backplane.



The figures below show sample TDT results for the reference (incident), 20-slot, and 4-slot bus transmitted edges. The most important characteristics are the risetime and amplitude.

Figure A4 shows the reference edge which was applied to the sample backplane signal lines; the risetime is measured to be 140 ps and the amplitude is measured to be approximately 392 mV (the maximum value is 400 mV out of the TDR generators).

Figure A4 – TDT reference (incident) waveform.

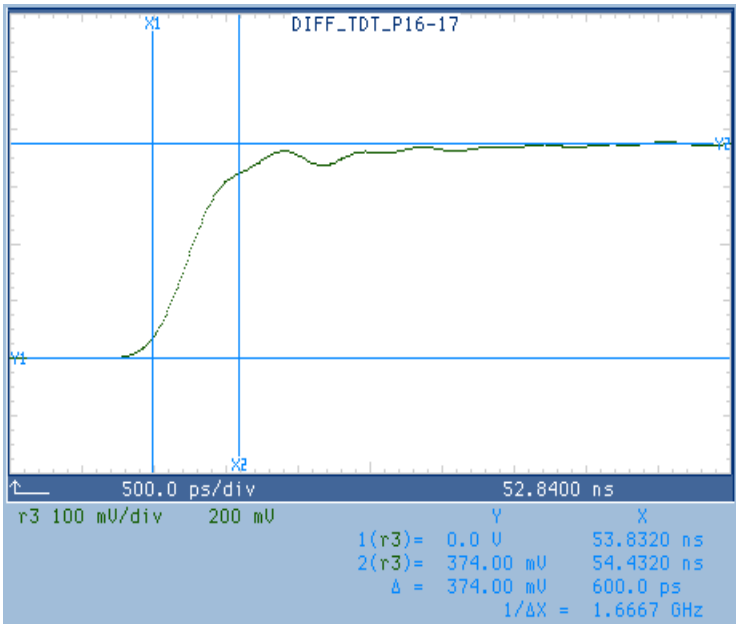


Figure A5 – TDT transmitted waveform (20-slot bus).

Figure A5 shows a TDT waveform which has been transmitted down a 20-slot bus signal of the BLVDS backplane.

Figure A5 shows that an edge which has been transmitted down the backplane. The bus line hits all twenty slots, each with the backplane half of the connector.

Note that the edge is seen to slow down significantly to a 600 ps risetime. Using the formula presented earlier for "RMS Risetime Bandwidth" (equation 2), an edge with a risetime close to 600 ps is roughly at the bandwidth of this backplane.

The amplitude is also seen to decrease to around 374 mV – or a gain of 95 % when compared to the reference waveform.

Figure A6 shows similar data for the 4-slot bus case.

Figure A6 shows the resulting transmitted waveform for a 4-slot bus, with two connectors on either end of the backplane. Note that we still see a similar slowing of the edge's risetime since the signal traverses the length of the backplane.

However, the amplitude eventually reaches 100 % of the reference amplitude so the signal losses seen in the 20-slot case are not evident here.

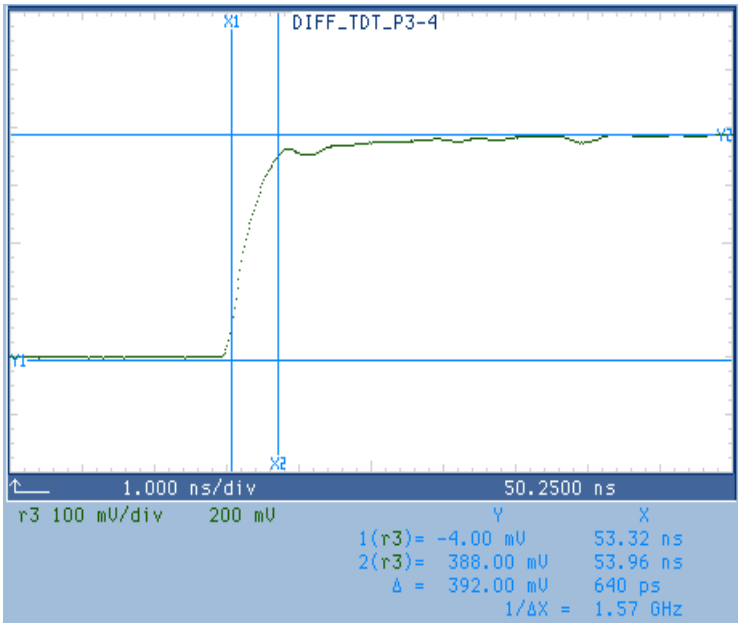


Figure A6 – TDT transmitted waveform (4-slot bus).

B. Selected SPICE Simulation Results for BLVDS Backplane Designs

The following are a number output plots from the SPICE analysis of the existing National Bus LVDS test backplane with plug-in cards. Avanti Corp.s Star-Hspice® simulator was used throughout.

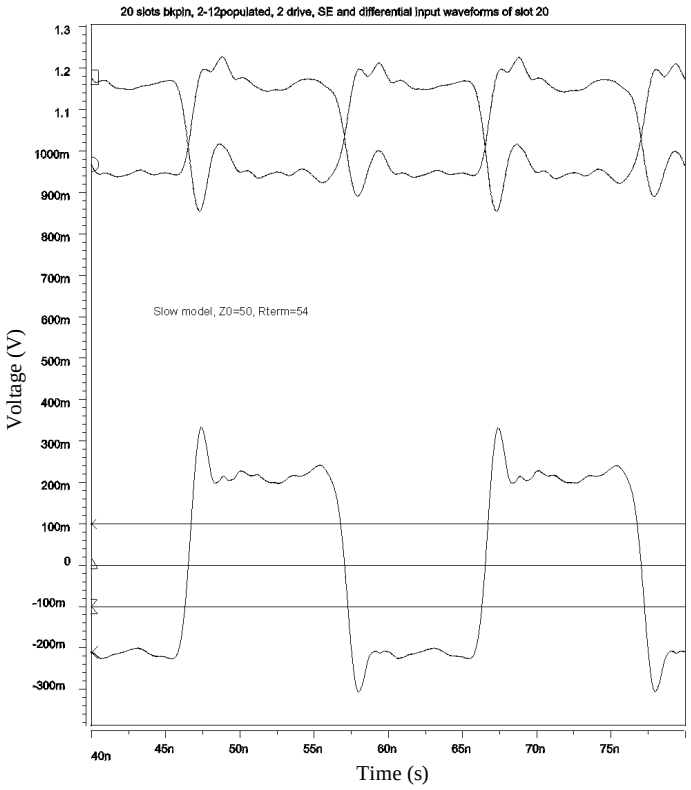


Figure B-1 (right) shows the simulation result for the 20-slot backplane with cards in slots 2-12. The card in slot 2 is the driver. Both the single-ended and differential receiver input waveforms are shown for the receiver in slot 20.

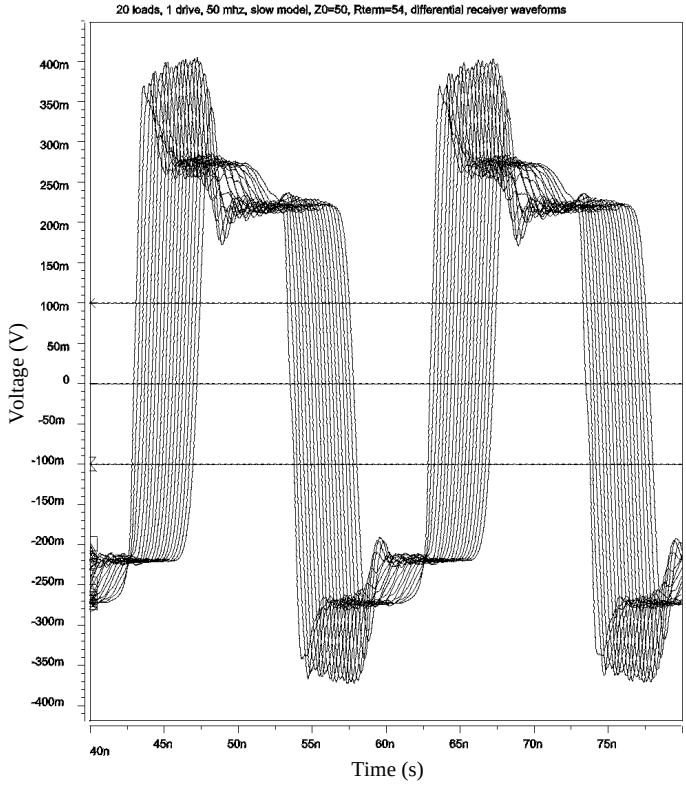


Figure B2 (left) shows the differential receiver input waveforms for slots 2-20 for a fully loaded 20-slot backplane with slot 1 as the driving card.

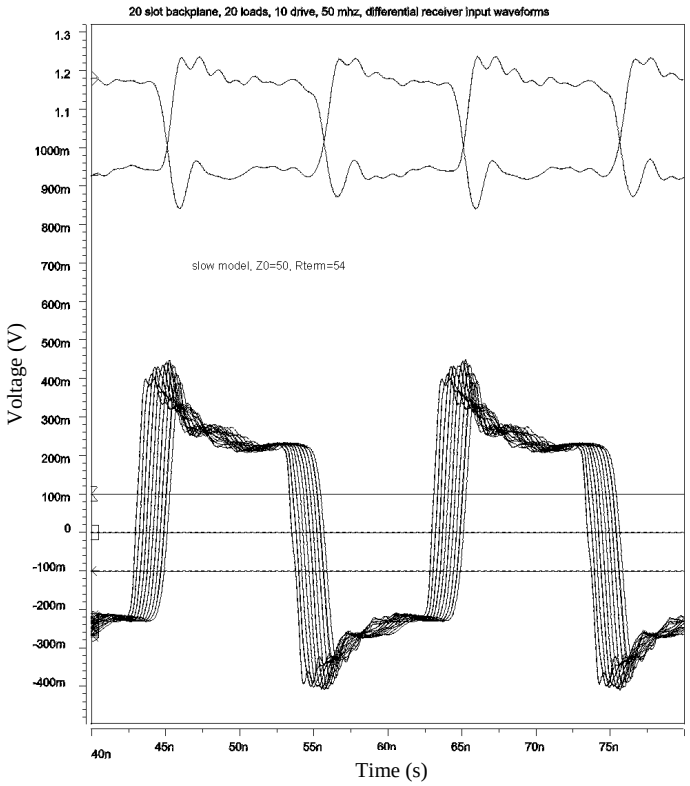


Figure B3 (right) also shows results for a fully-loaded 20-slot backplane. Here, single-ended (slot 20 receiver) and differential results (slots 1-9, 11-20) are shown for the case where the driving card is located in slot 10.

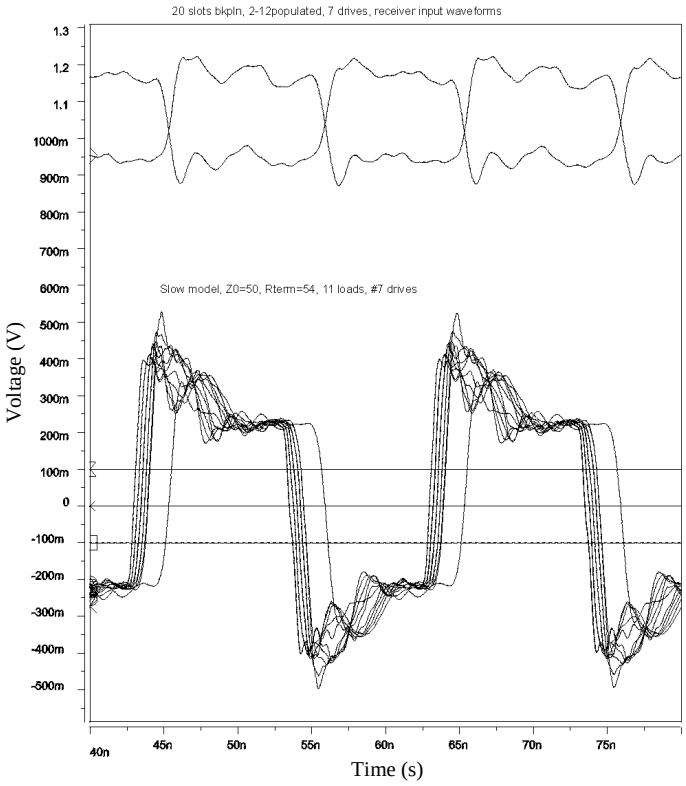
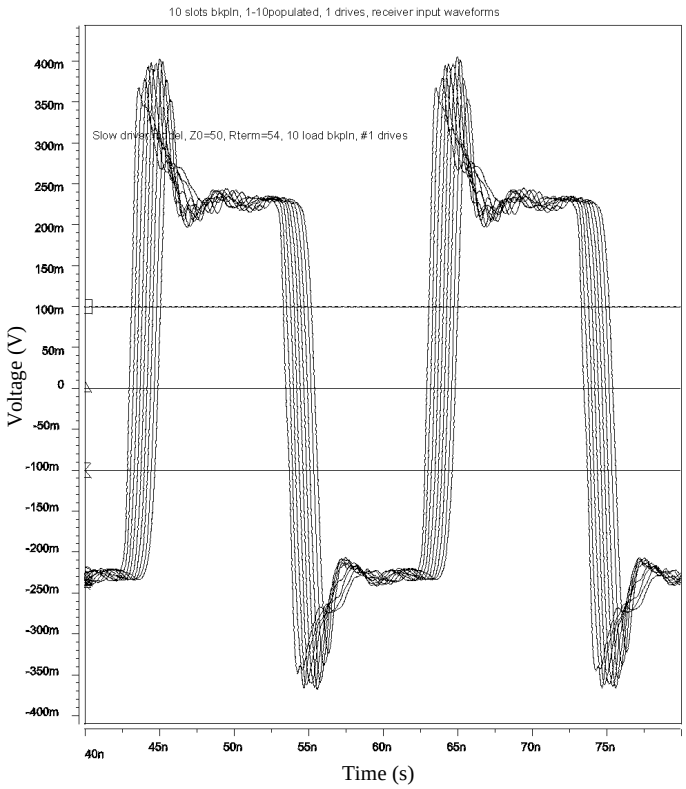


Figure B4 (left) shows similar results for a partial load (slots 2-12 populated) when the card in slot 7 drives the bus. The single-ended waveforms at the top of the plot are at the receiver of the card in slot 20. The differential results are at slots 2-6 and slots 8-12.

Figure B5 (right) shows the differential receiver input waveforms at slots 2-10 for a 10-slot BLVDS backplane with the card in slot 1 driving the bus.



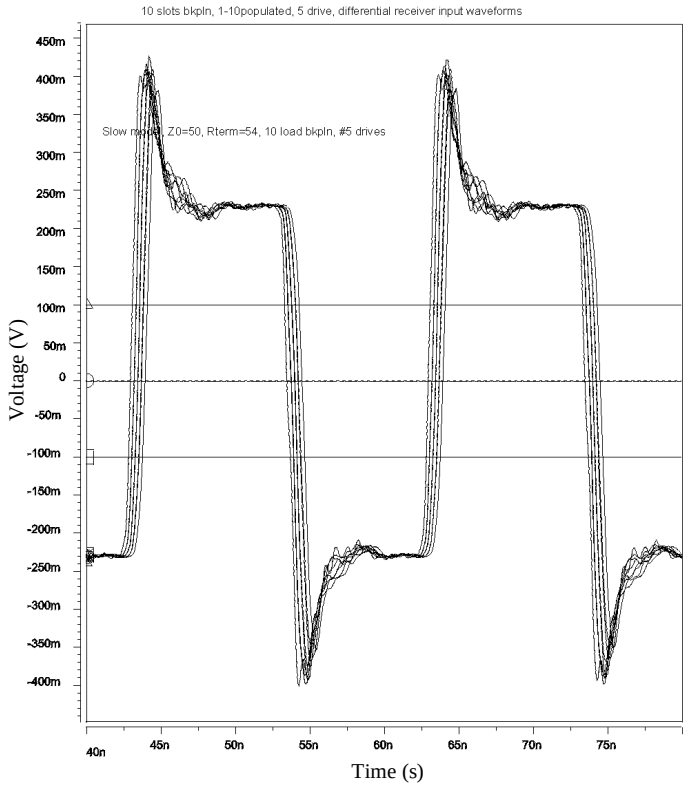
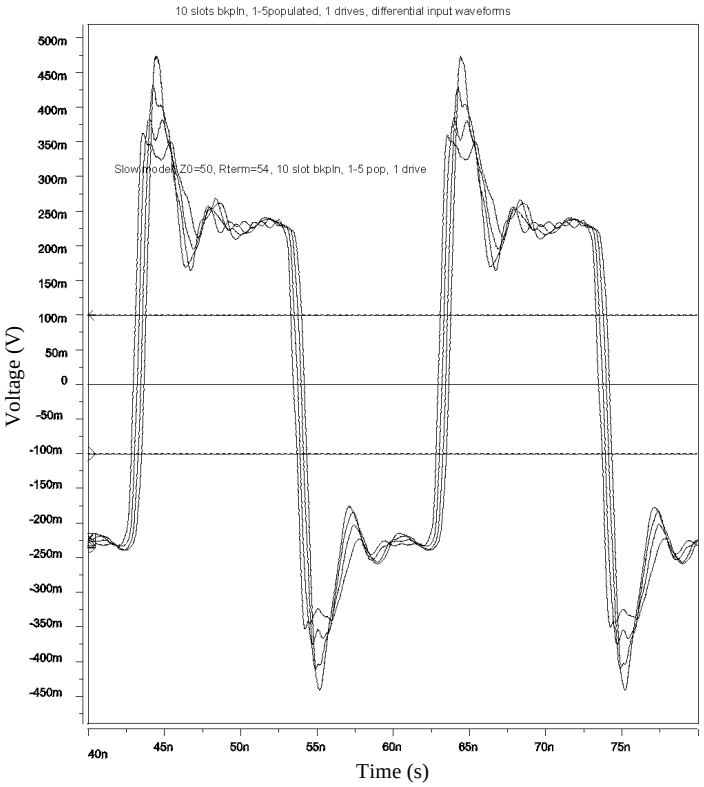


Figure B6 (left) shows similar data for the 10-slot backplane configuration but, with the card in slot 5 driving the bus. The differential waveforms shown are at the inputs to the receivers at slots 1-4 and 6-10.

Figure B7 (right) shows simulation results for a half-loaded, 10-slot BLVDS backplane with slots 1-5 populated. The card in slot 1 drives the bus. Differential receiver input waveforms are shown for slots 2-5.



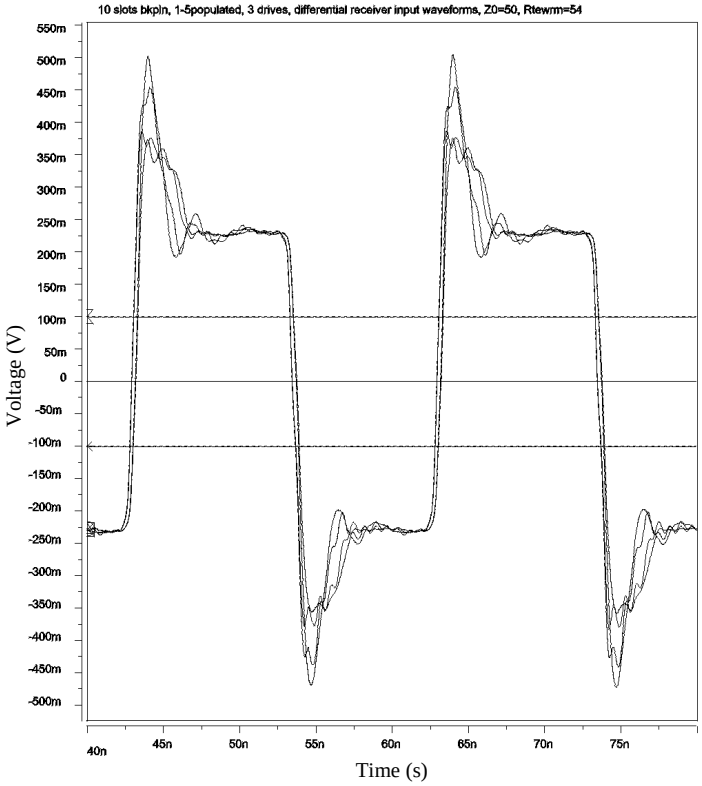


Figure B8 (left) shows the results for the same half-loaded, 10-slot backplane but, with the card in slot 3 driving. Differential receiver input waveforms are shown for the cards in slots 1, 2, 4, and 5.

C. Clock Frequency vs. Duty Cycle

NESA has found, during extensive simulation studies, that a given signal's duty cycle will shift with clock frequency, shifting more with greater frequency. The reason for this is not completely understood at this time but, this phenomenon seems to be contained to the simulations. Figure C1 shows a typical BLVDS signal running at 66 Mbps; the duty cycle is 54 % (the low bit is roughly 46 % of the "33 MHz" high/low data cycle).

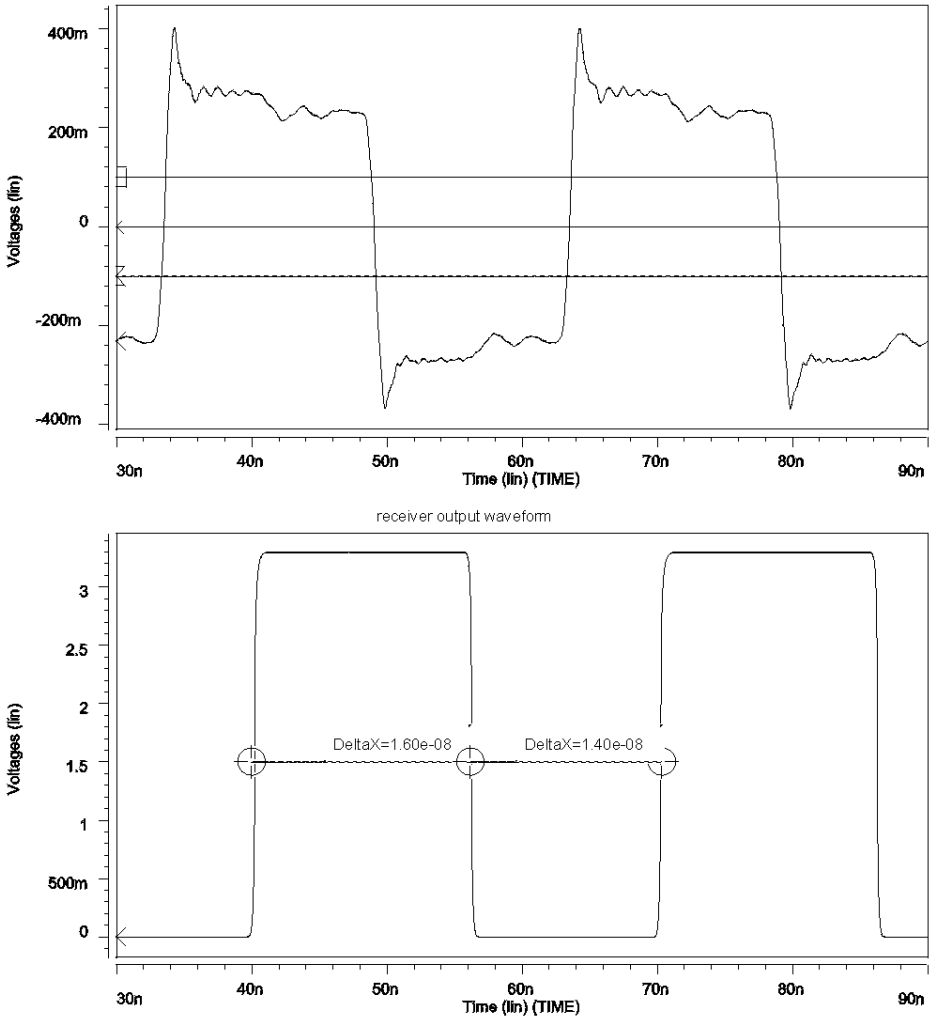


Figure C1 – Receiver input (above) and output; high/low bit sequence running at 66 Mbps.

Figure C2 below shows the rather pronounced shift for a 200 Mbps case. The low data bit is now roughly 40 % of the "100 MHz" high/low data cycle. This type of shift may, or may not, be significant depending on available timing margins and required sampling time for the low bit; it would certainly need to be taken into account in the system analysis. It should be reiterated that NESA has only seen this shift in simulation data to date. All active measurement results have been fairly well balanced. Figure C3 shows graphically the "duty cycle" shift versus clock frequency.

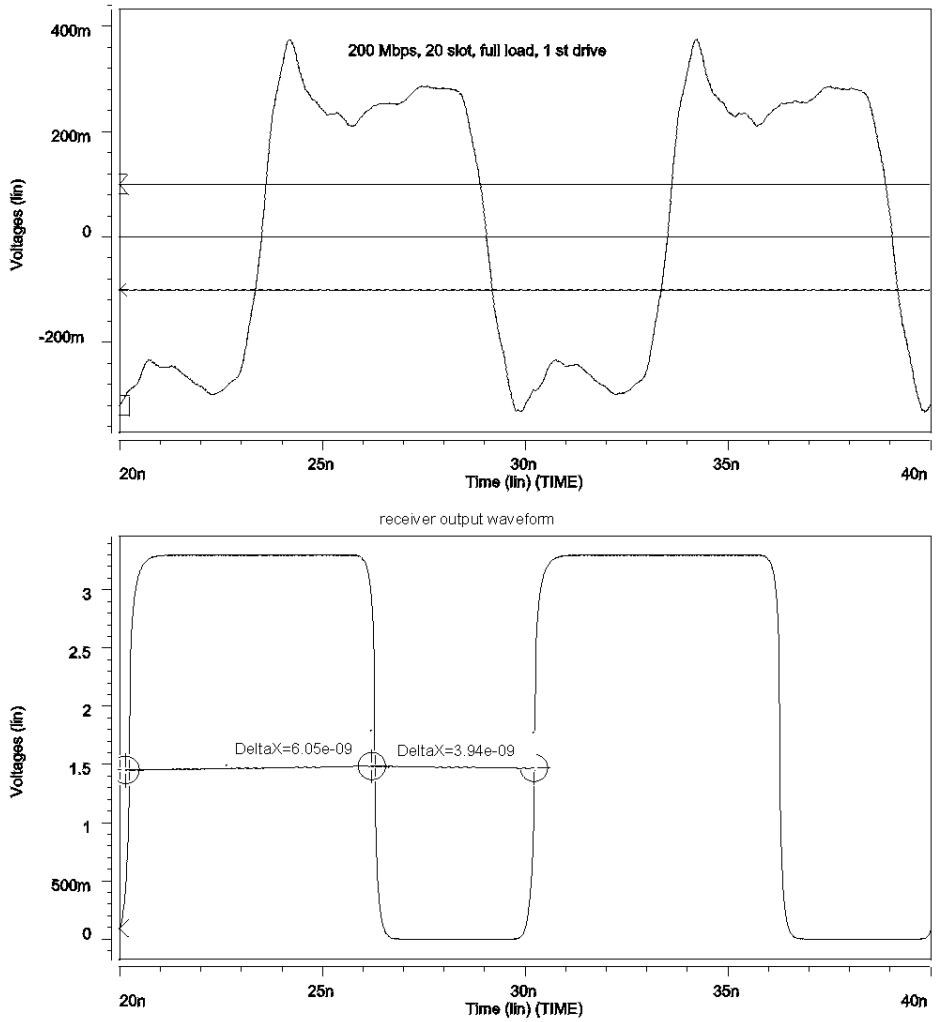


Figure C2 – Receiver input (above) and output; high/low bit sequence running at 200 Mbps.

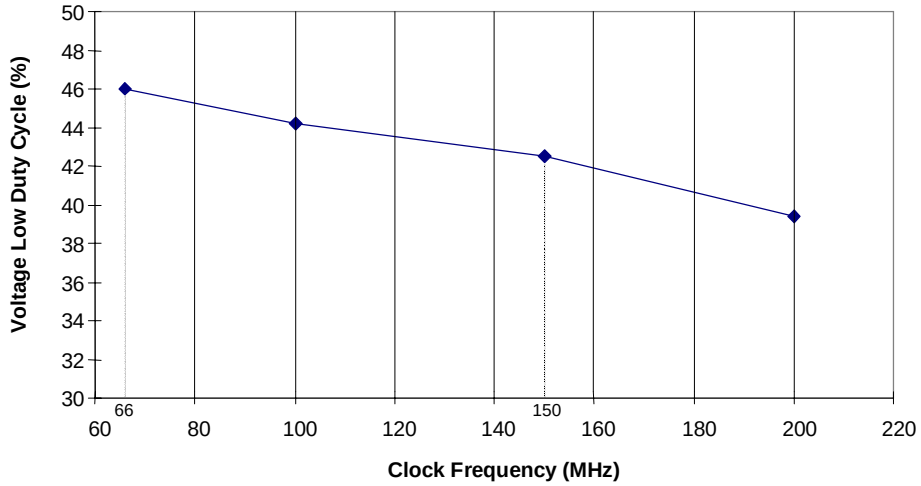


Figure C3 – Low data bit duty cycle vs. clock frequency.

D. National Bus LVDS Plug-in Cards and Backplane Physical Description

Plug-in Card Physical Description:

Construction: four-layer design with microstrip signal geometries (sig/gnd/vcc/sig)
Material: FR-4
Thickness: 0.062”
Impedance: 50 Ω single-ended traces; 80 – 90 Ω differential

BLVDS Backplane Physical Description:

Construction: four-layer with microstrip signal geometries (sig/gnd/vcc/sig)
Material: FR-4
Thickness: 0.125”
Impedance: 50 Ω single-ended traces; 80 – 90 Ω differential

For C-row signal traces:
Trace thickness, t = 0.0014” (1 oz. copper)
Trace width, W = 0.015”
Trace separation (within pair), S = 0.014”
Dielectric thickness, H = 0.008”
Assumed dielectric constant (used in National predictions), $\varepsilon_r = 3.9$
Predicted unloaded impedance: single-ended = 50 Ω
differential = 87 Ω

For A-row signal traces:
Trace thickness, t = 0.0014” (1 oz. copper)
Trace width, W = 0.015”
Trace separation (within pair), S = 0.008”
Dielectric thickness, H = 0.008”
Assumed dielectric constant (used in National predictions), $\varepsilon_r = 3.9$
Predicted unloaded impedance: single-ended = 50 Ω
differential = 82 Ω

Connectors: 3-row, 96-pin DIN connectors (AMP p/n 535043-4)

(See backplane drawing in Figure D1 next page.)

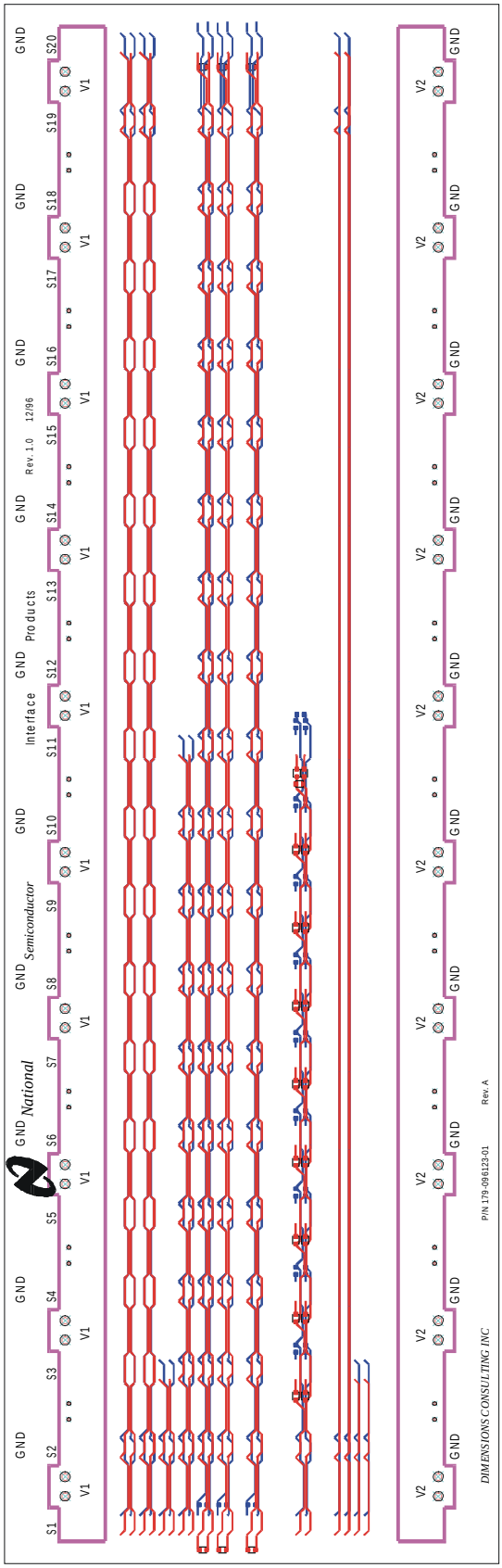


Figure D1 – Layer plot of the National Bus LVDS (BLVDS) test backplane.