National Semiconductor

Application Note OA-14

Improving Amplifier Noise Figure for High 3rd Intercept Amplifiers

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Abstract

Wide spurious-free dynamic range certainly the goal for any IF amplifier. This is particularly true for OTH radar as well as other systems using high resolution digitizers. Recently introduced current feedback amplifiers offer exceptional 3rd order intermodulation intercepts at very low quiescent power levels, but have been plagued by relatively poor noise figures. Teaming these op amps with a simple transformer input coupling yields noise figures less than 7dB with 3rd order intercepts greater than 40dBm (for frequencies < 10MHz).

Although not commonly considered for IF amplifiers, wideband, DC coupled operational amplifiers can offer considerable performance advantages at the lower IF (or HF) over standard AC coupled amplifiers. Particularly suitable from a distortion standpoint are a family of recently introduced monolithic current feedback operational amplifiers. Similar to the more common voltage feedback op amps, these parts offer very high non-inverting input impedance, very low output impedance, and a very high open loop gain that is controlled through the use of external resistors to set a well controlled closed loop gain. These amplifiers are unique in that the inverting node presents a low impedance through which the amplifier senses a feedback current as opposed to the more common feedback voltage. (Reference 1)

The current feedback topology, as implemented in National's CLC400 and CLC401 amplifiers, is also exceptionally symmetric. This yields intrinsically low distortion mechanisms internal to the amplifier which are then divided by the loop gain to yield the closed loop distortion. As described in Reference 1, the loop gain for a current feedback amplifier is principally set by the feedback resistor value. The loop gain will, of course, show a frequency dependence yielding a continued improvement in distortion down to the dominant open loop pole frequency (at approximately 350kHz for these parts). Conversely, the distortion will worsen moving to higher frequencies as the open loop gain rolls off. Measuring the 3rd order intermodulation intercept at 10MHz yields between 40 and 45dBm for these two parts. Although theory indicates a continued improvement below this frequency, accurate measurements are difficult to perform for intercepts above 45dBm for output power levels within the capability of these two devices.

Taking advantage of this exceptional intercept performance has, however, been impaired by noise figures ranging from 11 to 20dB depending on the device and the gain setting used. Reflecting all op amp noise sources to the non-inverting input typically yields an equivalent input spot noise voltage (at frequencies above the 1 /f noise corner) that range from 2.4nV/√Hz to well over 5nV/√Hz (for the CLC401 operated at low gains.) Aside from the intrinsic noise voltage at the non-inverting input, the effect of the inverting noise current also contributes strongly to this result. (See the appendix and Application Note OA-12 for a discussion of calculating the equivalent input noise voltage.)

As suggested in the literature (Reference 2), transformer coupling can sometimes be used to reduce an amplifier's noise figure. This is possible when the equivalent input noise voltage is much greater than the noise voltage generated by the input noise current through the source impedance. Reference 2 suggests an optimum source impedance for noise figure given by the ratio of noise voltage to noise current. If this ideal impedance is much greater than the typical 50Ω source impedance seen in IF strips (as it is for the two amplifiers considered here), a significant improvement in the noise figure can be achieved using transformer coupling. Conceptually, the transformer will provide a noiseless voltage gain at the expense of increasing the source impedance for the input noise current.

Using this technique with the current feedback op amps will sacrifice the DC coupling, with the transformer setting the low frequency limit of operation. Depending on the amplifier to set the high frequency limit will yield poor distortion performance near the amplifier's -3dB frequency. The amplifier's -3dB point is largely determined by the frequency at which the loop gain has dropped to unity. With negligible loop gain, the internal distortion mechanisms are no longer corrected yielding poor distortion performance. Hence, it is preferable to have the transformer also limit the high frequency performance. Both amplifiers considered here offer -3dB bandwidths exceeding 100MHz. A transformer offering good performance up through 50MHz maximum and down to as low a frequency as is desired would probably be a suitable choice.

Topology Description

Figure 1 shows the topology to be considered.

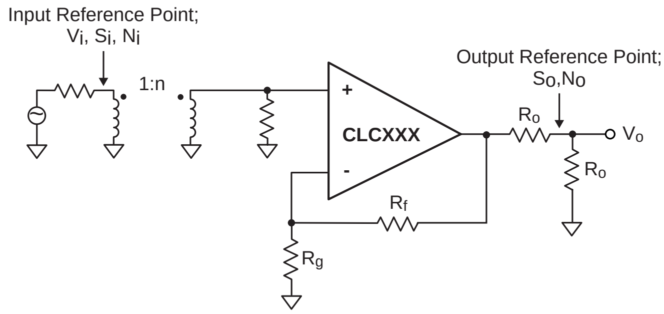

Figure 1

The transformer will provide a noiseless voltage gain from the voltage applied to its input to the non-inverting input of the amplifier. This is done at the expense of increasing the AC source impedance looking back out of the amplifier's non-inverting input. Increasing the turns ratio of the transformer (i.e. picking up voltage gain) will decrease the noise figure until the noise term due to the non-inverting input noise current times the source impedance equals the equivalent non-inverting input noise voltage.

Constraints and Assumptions

1. Input impedance matching to the source impedance (R_S) at the transformer input is desired. Therefore, $R_1 = n^2R_S$
   With this assumption, going to the output side of the transformer, the source impedance for the non-inverting input noise current will equal $R_1/2$ or, in terms of R_S will be $n^2R_S/2$.
   R_1 will also introduce a noise voltage term into the analysis.

2. Since the op amp offers a low output impedance, a separate matching resistor must be added to drive into a matched load as would be typical in an IF application (normally, R_o = 50 ohms). If we assume the resistor noise of the output matching network is negligible compared to the noise at the output, no change in the S/N ratio will be seen in going from the output pin of the amplifier to the load point. Therefore, the noise figure and gain will be calculated to the load point neglecting any noise added by the output matching resistor, R_o.

3. The various noise contributors for the amplifier are considered to be uncorrelated. This allows equivalent total noise powers to be developed as the sum of the separate noise powers. The noise voltage and currents are taken to be the spot noise values yielding a spot noise figure value. For transformer low frequency rolloff comers < 100kHz, some increase in spot noises at the low frequencies will be observed due to the 1/f noise comers for the amplifiers. (Refer to the individual op amp data sheets or Application Note OA-12 for detailed noise data).

Noise Figure Computation

To develop an expression of the noise figure for the circuit of Figure 1, the most elementary definition shown as Equation 1 will be used

$$NF = 10\log\frac{S_i / N_i}{S_o / N_o} \qquad \textbf{Eq. 1}$$

This definition states that the noise figure is 10 times the log of the ratio of the signal/noise ratio at the input to the signal/noise ratio at the output. These ratios are for the signal and noise powers available at the input and output. The noise power available at the input is taken to be that delivered by R_S to a conjugate matched load where the noise of that load is separated out as being added by the system. Since some noise will always be added, the signal/noise ratio at the output will be degraded from that at the input yielding a noise figure always > 0.

To evaluate the noise figure expression, the circuit of Figure 1 is redrawn in a more idealized form in Figure 2.

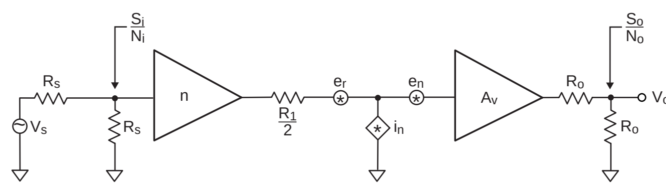

Figure 2

In this circuit, the transformer has been replaced by its equivalent elements; an input terminating impedance (R_S), a noiseless voltage gain given by the turns ratio (n), and an equivalent output impedance taken as the parallel combination of R_1 and R_S reflected through the transformer. ($R_1/2$). Note that R_1 has been reflected to the input side as a noiseless terminating resistor, R_S. R_1's noise contribution is retained as e_r on the output side of the transformer since this needs to be considered as part of the noise added by the system.

The amplifier has been replaced by an infinite input impedance gain block (A_V) with its two equivalent noise sources brought out as e_n, and i_n. Note that en includes the noise contributions of the inverting input noise current and the feedback and gain setting resistor noises. (This analysis is described in the appendix.)

Although the gain and noise terms of Figure 2 have thus far been expressed as voltage gains with noise voltage and current terms, the noise figure development deals only with power gains and noise powers. Therefore, the gains and noises shown on Figure 2 will be modified to get the power gain from input to output and the noise powers delivered at the input and output.

Looking at the separate parts of the argument in Equation 1, we can separate them as:

$\frac{S_i}{S_o} \rightarrow$ inverse of the power gain through the path

$$= \frac{V_i^2 / R_s}{\left(\frac{nA_vV_i}{2}\right)^2 / R_o} = \frac{4}{(nA_v)^2} \frac{R_o}{R_s}$$

$\frac{N_o}{N_i} \rightarrow$ output noise power over input noise power

The output noise power can be developed by taking each contributing noise voltage term through to the output then developing the power of that voltage across R_o and adding all the terms. The separate noise voltage terms at the output are:

Source noise voltage $\rightarrow \sqrt{4KTR_s}\,\frac{1}{2}\,nA_v\,\frac{1}{2}$

Terminating resistor noise $(e_r) \rightarrow \sqrt{4KTR_1}\,\frac{1}{2}\,A_v\,\frac{1}{2}$

where $K \rightarrow$ Boltzman's constant
$= 1.38E-23$ Joules / °Kelvin
$T \rightarrow$ °Kelvin $= 290°$ in this analysis
then $4kT = 16E\text{-}21J$

Amplifier current noise $\rightarrow i_n \frac{R_1}{2} A_v \frac{1}{2}$

Amplifier voltage noise $\rightarrow e_n\, A_v\, \frac{1}{2}$

Note that both noise voltages intrinsic to R_s and R_1 are attenuated by 1/2 due to the impedance matching present on both sides of the transformer (i.e. R_1 reflects to the source side as R_s to ground, and R_s reflects to the secondary side as the driving impedance for the non-inverting input terminating impedance, R_1).

Substituting with $R_1 = n^2R_s$, and adding each noise voltage term squared divided by the output terminating impedance, R_o, will yield the total output noise power.

$$N_o = \left[KTR_s\left(\frac{nA_v}{2}\right)^2 + KTn^2R_s\left(\frac{A_v}{2}\right)^2 + i_n^2\left(\frac{n^2R_s}{2}\right)\left(\frac{A_v}{2}\right)^2 + e_n^2\left(\frac{A_v}{2}\right)^2\right] / R_o$$

The input noise power may be derived as the power delivered to the source matching resistor from the source resistor noise voltage. This is:

$$N_i \rightarrow \left[\frac{1}{2}\sqrt{4KTR_s}\right]^2 / R_s = KT$$

Pulling an $\left(\frac{nAv}{2}\right)^2 R_s$ out of the N_o expression, the ratio of input to output noise power may be rewritten as:

$$\frac{N_o}{N_i} = \frac{(nA_v)^2R_s}{4R_o}\,\frac{KT + KT + i_n^2n^2\frac{R_s}{4} + \frac{e_n^2}{n^2R_s}}{KT}$$

Combining the expressions for noise power ratios and the inverse of the power gain through the channel, developed above, yields:

$$\frac{S_i}{S_o}\frac{N_o}{N_i} = \frac{4R_o}{(n\,R_v)^2R_s}\,\frac{(n\,R_v)^2R_s}{4R_o}\left(2 + \frac{i_n^2n^2\frac{R_s}{4} + \frac{e_n^2}{n^2R_s}}{KT}\right) =$$

$$\frac{S_i}{S_o}\frac{N_o}{N_i} = \left(2 + \frac{i_n^2n^2\frac{R_s}{4} + \frac{e_n^2}{n^2R_s}}{KT}\right)$$

Multiplying the fraction through, top and bottom, by R_s and going back to the log form for noise figure yields:

$$NF = 10\log\left(2 + \frac{\left(i_n n\frac{R_s}{2}\right) + \left(\frac{e_n}{n}\right)^2}{KTR_s}\right) \qquad \textbf{Eq. 2}$$

Looking at the component parts of this expression, the "2" in the log argument arises from our terminating with a discrete (noisy) matching resistor, R_1. This increases the minimum achievable noise figure from 0dB to 10 • log (2) = 3dB.

The $\frac{\left(i_n n\frac{R_s}{2}\right) + \left(\frac{e_n}{n}\right)^2}{R_s}$ parts of the fraction represents the 2 noise voltages (the total equivalent input noise voltage and the voltage generated by the noise current through the source impedance) at the input of the amplifier reflected to the transformer input and added as powers across R_s. The kT term in the denominator is simply the noise power available from the source at the input to the network. From this, as the turns ratio increases, the contribution of the noise current increases while that due to the noise voltage decreases As reported in Reference 1, the minimum value will occur when these two terms are equal.

Solving for the optimum turns ratio to minimize the noise figure:

$$n_{opt} = \sqrt{\frac{e_n}{i_n\frac{R_s}{2}}}$$

Substituting this in Equation 2 yields a minimum noise figure:

$$NF_{min} = 10 \log\left(2 + \frac{e_n i_n}{KT}\right)$$

Recognizing that transformer turns ratios are actually only available in integer steps, the optimum turns ratio is somewhat academic. However, for a given n, it can be recognized that anything that will reduce i_n or e_n will improve the noise figure.

Little can be done to reduce the noise current at the amplifier's non-inverting input. The equivalent input noise voltage can, however, be reduced as the amplifier is operated at higher gains. The results in the appendix show that equivalent input noise terms due to the inverting noise current and resistor noises are reduced as the gain increases. However, once these noise terms have been reduced below the intrinsic non-inverting input noise voltage, further improvements through increased gain are minimal.

Design Procedure and Test Results

To illustrate the design procedure and the resulting performance using this input transformer coupling, two possible designs using the CLC400 and CLC401 will be developed. The designs will proceed with the assumption that the maximum gain consistent with broad bandwidth and good 3rd order intermod intercept is desired. Enough information is presented to allow a design to proceed from a targeted gain as well.

The CLC400 is a broadband DC coupled monolithic amplifier intended for relatively low gain operation. Typical specifications show a 200MHz bandwidth (-3dB) at a gain of +2. Both parts pull a nominal no load current of 15mA when operated from their recommended ±5 volt power supplies. For the current feedback topology, a low gain part corresponds to a part that has been optimized for a lower value of feedback resistor as opposed to a high gain part such as the CLC401. Hence, the nominal N at a gain of + 2 for the CLC400 is shown on the data sheet as 250 ohms, while the CLC401 is optimized to use a 1.5k feedback at a gain of +20. Most of the requisite information for the design can be found in National Application Notes OA-12 (Noise Analysis) and OA-13 (Current Feedback Loop Gain Analysis).

Non-inverting input intrinsic noise voltage	$e_{ni} = 2.5nV/\sqrt{Hz}$
Inverting input noise current	$i_i = 14pA/\sqrt{Hz}$
Non-inverting input noise current	$i_{ni} = 3.2pA/\sqrt{Hz}$
Inverting input impedance	$Z_i \simeq 50\Omega$
Nominal feedback transimpedance for maximally flat frequency response	$Z_t = 350\Omega$

Using these numbers, and equation F in the appendix, a maximum amplifier gain for reduced equivalent input noise voltage may be derived as (this assumes an ** of 1/9) G = 4.3

Rounding this off to a gain of +4 yields a feedback resistor value of:

$R_f = Z_t - GZ_1 = 150\Omega$ **(Eq. D In Appendix)**

Note that taking the gain too high will eventually yield very low R_f values from this equation. For very low values of R_f, a significant degradation in both bandwidth and 3rd order intercept will be observed due to the added output stage loading presented by the feedback network. Generally, $R_f + R_g = 200\Omega$ should be taken as a lower limit to R_f.

Computing the equivalent input noise voltage for G = 4 using Eq. E of the appendix yields:

$$e_n = \sqrt{(2.5nV)^2 + [(14pA)(37.5\Omega)]^2 + 16E-21(37.5\Omega)} = 2.67\frac{nV}{\sqrt{Hz}}$$

As hoped, this total equivalent input noise voltage is nearly equal to the intrinsic noise voltage listed above. From these results, and assuming a 50Ω source impedance, an optimum transformer turns ratio would be:

$$n_{opt} = \sqrt{\frac{e_n}{i_n \frac{R_s}{2}}} = \sqrt{\frac{6.67nV}{3.2pA(25\Omega)}} = 5.78$$

This yields a best case noise figure equal to

$$NF_{min} = 10 \log\left(2 + \frac{2.67nV}{4E-21}\right) = 6.2dB$$

It is, however, difficult to maintain broadband performance through the transformer with a turns ratio this high. For test, a 1:4 turns ratio transformer from Mini-Circuits was selected as a reasonable compromise between best noise figure and broadband performance (part #T16-6T)

The resulting test circuit for the CLC400 is shown in Figure 3.

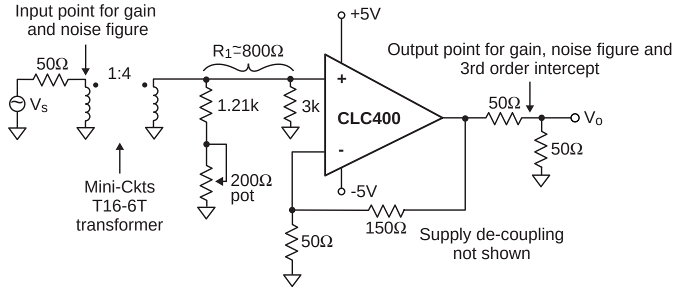

Figure 3

$$NF = 10\log\left(2 + \frac{\left(4(3.2pA)25\Omega\right)^2 + \left(\frac{2.67nV}{4}\right)^2}{(4E-21)\,(50\Omega)}\right) = 6.2dB$$

Using this test circuit, the anticipated performance can be calculated to be:

Overall gain Av = 4 • 4 • 1/2 = + 8 (18dB)

Noise Figure (from Eq.2)
In test, the first step was to tune the input impedance matching to provide a good 50Ω match over the frequency range of interest, after which the transfer function (S_{21}) was measured. These results are shown in Figure 4

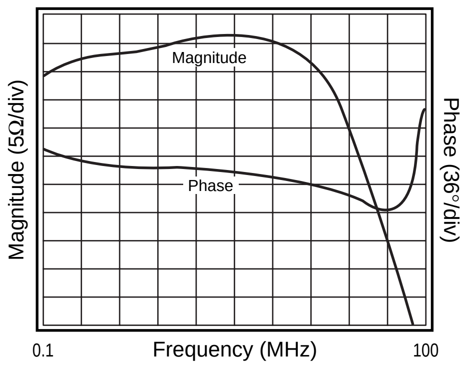

Figure 4a: Input Impedance

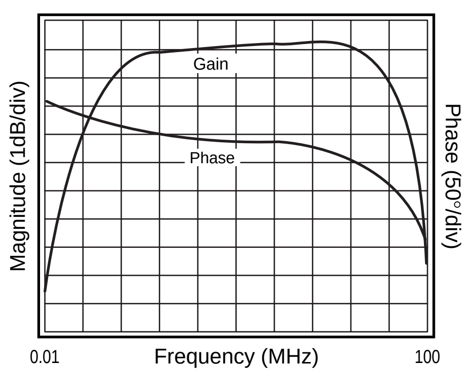

Figure 4b: Transfer Function

These results show excellent input impedance matching over a broad frequency range with a very flat passband gain from about 60kHz to 30MHz.

The noise figure for this circuit was measured using an HP8970A with an HP346B noise source. Figure 5 tabulates those results along with the 3rd order intercept.

Frequency	Noise Figure	3rd Order Intercept
10MHz	6.8dB	44dB
20MHz	6.8dB	38dB
30MHz	7.1dB	33dB
40MHz	7.1dB	30dB

Figure 5

The measured noise figure shows excellent agreement with the predicted value, while the 3rd order intercept parallels the CLC400 data sheet plots. Note that the data sheets typically show intercept defined for a power level at the output pin as opposed to the 6dB lower value if defined at the matched load. Adding 6dB to the results shown above gets us back to the data sheet plots. This indicates that the intercept has not been degraded by the transformer input coupling.

Note that the noise figure for just the CLC400, configured as shown in Figure 3 without the transformer, may be derived by simply letting n = 1 in the noise figure equation (Equation 2). Doing this yields a noise figure of 15.8dB for the CLC400 by itself (assuming only a 50Ω non-inverting input impedance matching resistor). Hence, the transformer not only provides us with more gain but with greatly improved noise figure.

In summary, this circuit shows a 50Ω in/50Ωout, 18dB gain block with very flat frequency response from 60kHz to 30MHz offering an approximate 7dB noise figure with a 3rd order intercept greater than 33dBm over that frequency range, while dissipating only 150mW quiescent power!

Design and Test Results for the CLC401
The CLC401 is a monolithic, DC coupled, wideband current feedback amplifier optimized for higher closed loop gains. Typical specifications show a 150MHz -3dB bandwidth at a gain of +20 using a 1.5k feedback resistor while drawing only 15mA no load current from the specified ±5 volt supplies. Getting the requisite design information from Application Notes OA-12 and OA-13,

Non-inverting input intrinsic noise voltage	e_{ni} = 2.4nV/√Hz
Inverting input noise current	i_i = 1 7pA/√Hz
Non-inverting input noise current	i_{ni} = 2.SpA/√Hz
Inverting input impedance	$Z_i \simeq 50\Omega$
Nominal feedback transimpedance for maximally flat frequency response	Z_i = 2.5kΩ

Using these numbers, and Eq. F of the Appendix, yields a maximum amplifier gain for minimal equivalent input noise voltage of (assuming ? of 1/9) G = 32.5

Building up the circuit at this gain and using the same transformer as for the CLC400 test circuit resulted in a 3dB response peaking at the higher frequency limits.

This seemed to arise from a gain dependent non-inverting input impedance resonating with the transformer. Reducing the amplifier gain ameliorated this effect, Since the amplifier gain was being determined somewhat arbitrarily to reduce the noise figure, backing away from this gain to improve frequency response seemed reasonable. For test, an amplifier gain of G = +25 was selected. Using Eq. E of the appendix shows an equivalent input noise voltage with again of +25 given by:

$$e_n = \sqrt{(2.4\text{nV})^2 + [(17\text{pA})(37.5\Omega)]^2 + 16\text{E}-21(50\Omega)} = 2.70\,\frac{\text{nV}}{\sqrt{\text{Hz}}}$$

With this result, an optimum turns ratio for the transformer and a theoretical best noise figure may be calculated to be:

$$n_{opt} = \sqrt{\frac{2.70\text{nV}}{(2.8\text{pA})(25\Omega)}} = 6.2$$

and

$$NF_{min} = 10\log\left(2 + \frac{2.70\text{nV}\,(2.8\text{pA})}{4\text{E}-21}\right) = 5.9\text{dB}$$

Again, the high transformer turns ratio required for optimum noise figure would result in an unnecessarily limited bandwidth. Backing off to a 1:4 turns ratio transformer yielded the test circuit shown in Figure 6.

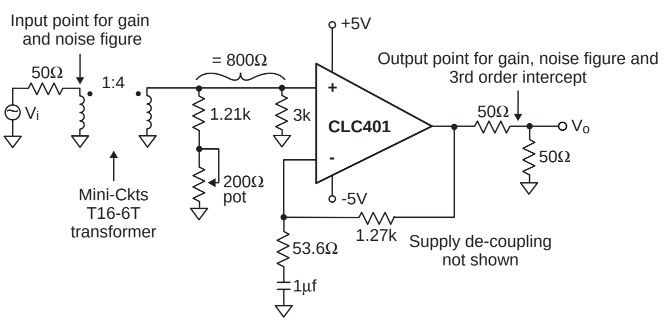

Figure 6

Note that for this test, the amplifier's gain setting resistor has been AC coupled with a 1mf capacitor. This is intended to reduce the DC gain for the amplifier's input offset voltage to 1, holding the output DC as close to 0 as possible. The capacitor value was chosen to yield a transfer function pole well below the transformer low frequency cutoff. The feedback resistor value is set using Equation D of the Appendix. The anticipated midband gain and noise figure performance can be calculated to be:

Overall Gain Av = 4 • 25 • 1/2 = + 50 (34dB)

Noise Figure (from Eq. 2)

$$NF = 10\log\left(2 + \frac{(4(2.8\text{pA})25\Omega)^2 + \left(\frac{2.70\text{nV}}{4}\right)^2}{4\text{E}-21(50\Omega)}\right) = 6.7\text{dB}$$

As with the CLC400, the test sequence was to the input matching impedance network to yield a good 50Ω match over as wide a frequency range as possible. After this, the input to output transfer function was measured (S21). Figure 7 show these results:

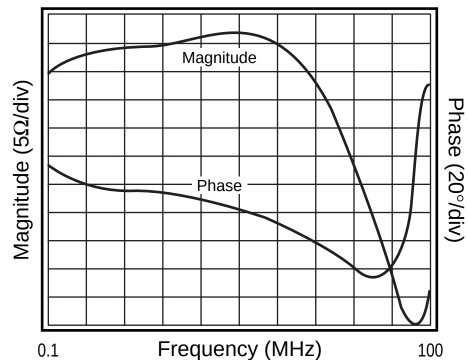

Figure 7a: Input Impedance

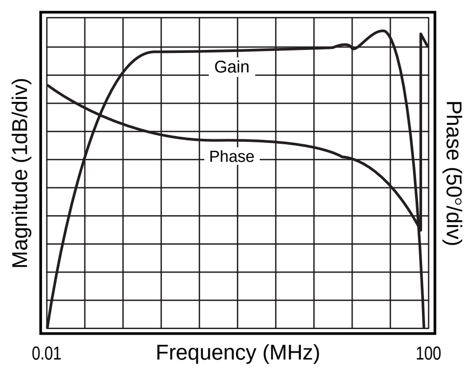

Figure 7b: Transfer Function

This circuit doesn't do quite as well in holding up the input impedance to higher frequencies but it does provide a reasonably flat frequency response from 70kHz to 50MHz (passband with < ± 0.5dB ripple).

A measure of the noise performance was obtained using an HP3585 spectrum analyzer along with a CLC100 low noise wideband amplifier as a preamp to the analyzer input. Although accurate noise figure measurements are difficult to achieve in this fashion, this approach indicated noise figures between 7 and 8dB. Figure 8 tabulates the measured 3rd order intercept results and this estimated noise figure.

Frequency	Estimated NF	3rd Order Intercept
10MHz	7-8dB	38dB
20MHz	7-8dB	33dB
30MHz	7-8dB	29dB
40MHz	7-8dB	25dB
50MHz	7-8dB	23dB

Figure 8

Calculating the noise figure of just the CLC401 without the transformer coupling (by letting n = 1 in the noise figure equation) yields 15.9dB for just the amplifier by itself with a 50Ω non-inverting termination resistor. So, again, the transformer has added signal gain while greatly improving the noise figure.

The results of Figures 7 and 8 show a 50Ω in/50Ω out, 34dB gain block with reasonably flat frequency response from 70kHz to 50MHz offering an approximate 7dB noise figure with 3rd order intercepts greater than 25dBm for operation below 40MHz dissipating only 150mW! The intercept performance improves rapidly at lower frequencies with continued improvement observed below 10MHz.

Comparisons and Conclusions

Clearly, the transformer coupling offers the potential for some real improvement in noise figures for the amplifiers considered here. Having given up the DC coupling in the process, however ‘ we are now looking to compare these parts to the more classical AC coupled IF amplifiers.

Those parts generally use a Class A output stage as opposed to the Class AB structure used in most of National’s amplifier products. This, along with the high loop gain at lower frequencies, allows exceptional distortion performance to be achieved at a fraction of the quiescent power dissipation vs. the more classical Class A output. This advantage narrows as we move to frequencies over 100MHz with the op amp’s loop gain dropping below unity at these higher frequencies.

Generally, for the lower frequency applications, the circuits described here, or similar circuits using different National amplifiers can offer considerable advantages in the areas of power dissipation, size, and cost.

The transformer coupling offers additional flexibility through potential signal inversion, by reversing the dot convention, output DC shifting, by inserting a DC voltage in place of the ground on the secondary, and potential narrowband filtering. If higher output power levels are desired, this same approach could be used with one of National’s hybrid op amps offering higher supply voltages and greater output power capability. The CLC232, for low gains, and the CLC207 for higher gains, are particularly low harmonic distortion parts that would also benefit, from a noise figure standpoint, from transformer coupling.

This approach to noise figure improvement is applicable to any op amp with an optimum source resistance greater than the actual source resistance. With the total equivalent input noise voltage at the non-inverting input decreasing as the closed loop gain is increased (as shown in the appendix), it is advantageous to operate the op amps at high gains. The current feedback topology, pioneered by National, is particularly suitable for wideband, high gain applications.

As described in Application Notes 300-1 and OA-13, the current feedback op amp topology largely eliminates the gain-bandwidth performance limitations plaguing earlier voltage feedback designs. Therefore, running the amplifiers to higher gains, in an effort to drive down the non-inverting input voltage noise, will not sacrifice broadband performance as it would using a voltage feedback part.

Acknowledgments

Ralph Carfi, General Electric, Syracuse, N.Y. for measuring the noise figure on the CLC400 test circuit and many useful discussions on this application.

Alan Baker, R&D, National Semiconductor Corp., for review and discussion of the noise figure equation development.

Steve Smith, R&D, National Semiconductor Corp., for automating the 3rd order intercept measurement procedure.

References

1.”Current-Feedback Amplifiers, “Sergio Franco EDN, Jan. 5, 1989, page 161 (in Comlinear Corporation 1989/1991 Databook). Also, National Application Note 300-1 and Application Note OA-14.

2.”Low-Noise Electronic Design,” Motchenbacher and Fitchen; Wiley 1973, pp. 10, 34, and 127.

Appendix:

Computing the equivalent Input noise voltage, the gain, and feedback resistor values for noise figure reduction with current feedback op amps.

The equations for determining the equivalent input noise voltage for use in the noise figure calculations will be developed. Since the external resistors around the amplifier, R_f and R_g, play a large role in setting that noise, the amplifiers transfer function, which is also determined by these resistors, will be given and used to set the gain.

Figure 9 shows the necessary information to develop both the transfer function from V_i to V_o and the equivalent input noise voltage expression. As described in Reference 1, a current feedback amplifier uses a unity gain buffer from the + input to the inverting node, X_1, with the inverting node current (i_{err}) acting as the feedback signal sensed and passed on to the output through a transimpedance gain, Z_s.

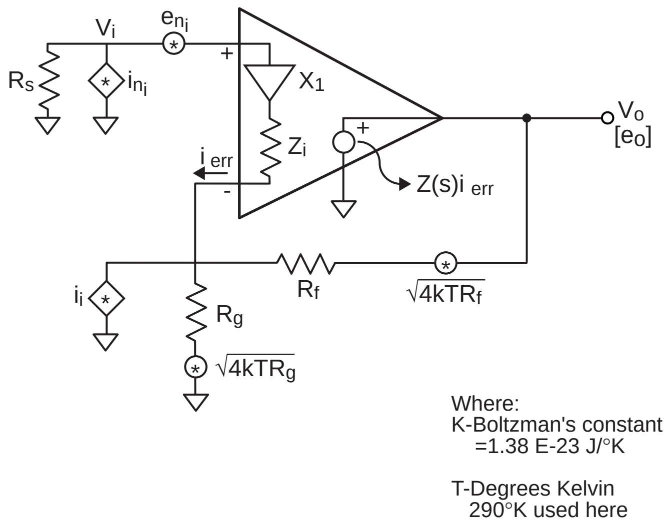

Figure 9

The goal here is to develop an equivalent non-inverting input noise voltage source to place at the non-inverting input for noise figure calculations. Normally, a noise generator for the non-inverting termination resistor would be included in this analysis. In the context of using an input transformer coupling, however, this resistor will be set by impedance matching concerns removing it as a variable for equivalent input noise voltage reduction. The effect of this resistor's noise is included in the development for noise figure. The 3 noise sources on the inverting side of the circuit must be reflected to the non-inverting side and combined with the intrinsic noise voltage, eni, already present in the model. Neglecting ini, which is left separate for later use in the noise figure equations, each noise voltage or current will develop an output voltage noise. With the non-inverting signal gain defined to be $G = (1 + R_f/R_g)$, the separate output noise voltages are:

intrinsic non-inverting input noise voltage $\rightarrow e_{ni}\,G$

inverting input noise current $\rightarrow i_i\,R_f$

combined resistor noise terms $\rightarrow \sqrt{4KTR_fG}$

Combining terms as the root sum of squared elements, and reflecting this to the non-inverting input yields

equivalent input noise voltage $\rightarrow \sqrt{\left(e_{n_i}\right)^2 + \left(\frac{i_iR_f}{G}\right)^2 + \frac{4KTR_f}{G}}$ **Eq. C**

As is apparent from this expression, both the gain and the resistor values can be used to reduce the input noise voltage. Increasing the gain and/or reducing the resistor values will both decrease the apparent input noise voltage. This effort is bounded by the intrinsic input noise voltage, e_{ni}.

Setting the gain and the resistor values needs to be done in the context of maintaining adequate phase margin for the closed loop amplifier response. Analyzing the circuit of Figure A for the V_o/V_i transfer function yields (see Application Note OA-13 for a more complete development);

$$\frac{V_o}{V_i} = \frac{1+R_f/R_G}{1+\frac{R_f + Z_i\left(1+R_f/R_G\right)}{Z_{(s)}}} = \frac{G}{1+\frac{R_f+GZ_i}{Z_{(s)}}}$$

where: $Z_{(s)} \rightarrow$ Forward transimpedance gain of the amplifier (frequency dependent)

$Z_i \rightarrow$ Inverting input impedance (considered noiseless and real)

The inverting node current is the feedback signal with an output voltage to inverting input current transfer gain given by $Z_t = R_f + Z_iG$

Every current feedback amplifier has an internal forward transimpedance gain function ($Z_{(s)}$) optimized for a certain value of Z_t. Typically, this optimization yields a 60° phase margin at the gain and feedback resistor value specified on the data sheet for guaranteed performance specs. To a first approximation, this Z_t can be held constant (maintaining maximum closed loop bandwidth with no peaking) as the desired closed loop signal gain is changed from the nominal design point. This is done by adjusting R_f vs gain. Solving for this from the above expression for Z_t yields:

$R_f = Z_t - Z_iG$ **Eq. D**

If this expression for R_f is placed into the equivalent input noise expression developed above, Eq. C, we get:

$$e_n = \sqrt{\left(e_{n_i}\right)^2 + i_i^{\,2}\left(\frac{Z_t}{G} - Z_i\right)^2 + 4KT\left(\frac{Z_t}{G} - Z_i\right)}$$ **Eq. E**

The only variable left at this point is the desired closed loop gain. The absolute resistor values have been removed with the assumption that a maximally flat frequency response is desired as the closed loop gain is changed. Again we see that increasing the gain will decrease the equivalent input noise voltage. This approach is decreasingly effective as those terms involving G become less than the non-inverting input noise voltage e_{ni}. If we target a desired ratio of the two squared terms involving G to the intrinsic non-inverting input noise voltage squared, we can develop a targeted maximum gain beyond which minimal noise reduction is achieved through further gain increases. If we call that ratio of the noise powers cc we can solve for:

$$\left(\frac{Z_t}{G} - Z_i\right) = \frac{2KT}{i_i\,2}\left[\sqrt{1+\alpha\left(\frac{e_{n_i}\,i_i}{2KT}\right)^2} - 1\right] \qquad \textbf{Eq. F}$$

From this expression, and a knowledge of Z_t and Z_i, a maximum desired gain may be derived. This yields a somewhat arbitrary upper limit on amplifier gain in that we are only trying to increase the gain until negligible improvements in the noise figure are seen. The amplifier can, of course, be operated at lower gains, with an increase in noise, or at higher gains, with little noise improvement but an eventual bandwidth limitation. If we set α to be 1/9 (saying that the reflected equivalent noise power terms at the non-inverting input are 1/9 the intrinsic input noise power due to the non-inverting input noise voltage) those terms increase the equivalent input noise voltage by only 5%. This will be the initial targeted design criteria used in the example developments.

See Application Note OA-13 for a complete development of adjusting R_f to hold a constant loop gain, and hence bandwidth, as the desired signal gain is changed.

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