Power and Thermal Considerations for High-Speed Clock Generators

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INTRODUCTION

As today's systems are operating at higher speeds and getting more portable than ever before, figuring the exact amount of the power consumed by them is becoming more critical. More accurate power calculations not only helps for optimized design of power supplies and fans, but also helps to better predict the long term reliability of systems.

Power consumption calculations, if not ignored, have been mostly an art rather than a science for most system designers. There are relatively accurate methods of determining how much power any given component consumes within a system, but due to many first order approximations the amount of the total power consumed becomes less accurate and meaningful. This inaccuracy forces the designers to use large safety factors (margins) when determining the requirements for their power supplies and fans.

Below is a brief discussion on how to calculate the power consumed under dynamic conditions for any given device. Once this value is determined for all the components in a system, other design parameters such as the power supply ratings, airflow and even the system's failure rate can be determined more accurately.

POWER CONSUMPTION SOURCES

The total power consumed within any device has two components

A. Static

B. Dynamic

The addition of these two components will result in the total power consumed within any given unit.

A. The static power has three components to it. First component is commonly referred to as the quiescent power. This power can be simply calculated by multiplying the DC supply voltage (V_{CC}) and its supply current (I_{CC}). This static power is typically ignored in the case of CMOS devices since the supply currents are very small compared to bipolar devices.

In the case of TTL compatible CMOS devices, there exists another source of static current. This current is the additional I_{CC} current forced on CMOS inputs from a high level TTL signal. For power calculation purposes, this current I_{CCT}, must be multiplied by the supply voltage and the duty cycle of the high level signal. This gives the power consumed statically per TTL compatible input for CMOS devices.

And finally the third source, is the power consumed due to the load terminations. It can be calculated as the product of the V_{OH} and V_{OL} by their respective currents as well as duty cycles.

B. **Dynamic** power consumed is the second component of the total power dissipated. It is more complicated to calculate and has more variables.

In order to look at these components closely, one must look at all the possible sources of power consumption which can be summed as the following:

1. Power consumed by the loads. This power is significant under dynamic conditions and it depends on the loads , voltage swings as well as the toggle frequency of each output.
2. Power consumed due to the internal capacitance of the device, or commonly known as the Cpd. This type of power consumption is often associated with CMOS technology devices rather than bipolar due to their inherently capacitive structures, and higher voltage swings.

   This power includes what is drawn from the power supply due to the instantaneous current spikes during output switching. This component is mostly present in CMOS devices since during output transitions, there will be a direct path from the supply to ground.
3. Input leakage power. This source of power consumption is often ignored in most calculations due to the very small amount of input leakage currents specially in CMOS devices.

These sources are present on all devices. However, depending on the process technology, some of these sources may have a very small effect on the total power consumed. In addition to the technology, loads, frequency of the operation as well as the supply voltage play major roles on how much power is dissipated within each integrated circuit.

THE FORMULA

In an attempt to put all of it together, the following formula can describe the power consumed across any given device:

$$P_{Total} = P_{Static} + P_{Dynamic}$$

where;

$$P_{Static} = (V_{CC}) * (I_{CC\ (quiescent)}) + (((V_{CC}) * (I_{CCT}) * DC_{Hi}) * n) + ((I_{OL} * V_{OL} * DC_{Lo}) + (I_{OH} * V_{OH} * DC_{Hi}))$$

where DC is the duty cycle and n is number of inputs.

Next is the dynamic power consumed, which as mentioned before, has more than one component and can be given by;

$$P_{Dynamic} = \Sigma\ (P_{Load} + P_{Cpd} + P_{Input})$$

Let us look at each component separately. P_{Load}, or the power consumed across the loads can be derived from the fact that the current thru a capacitive load can be given by:

$$I_{Load} = C_{Load} * (dV/dt)$$

where dV is the voltage swing across the capacitor (V_{swing}) and dt is the unit of time which is equal to the frequency.

Therefore

$$I_{Load} = C_{Load} * V_{swing(Loads)} * f$$

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The reason for such an easy transformation is the fact that the amount of the energy dissipated across the capacitor remains the same no matter how fast or slow it is being charged or discharged. Also since power is the product of current and voltage, the load power becomes;

$$P_{Load} = C_{Load} * (V_{swing(Loads)} * V_{CC}) * f$$

Given that different outputs may be operating at different frequencies, as is most often the case for clock generators, while each one driving a different load, the total load power must be rewritten as the sum of the power consumed across every output, as given below;

$$P_{Load} = \Sigma\,(C_{Load} * (V_{swing(Loads)} * V_{CC}) * f)$$

The next component is the power dissipated due to the internal capacitance of the device. This is also known as the C_{pd} power which comes from the fact that every device has some internal nodal capacitance which is being charged and discharged at a rate equal or below the highest frequency of the operation. Calculating this power is more important in CMOS devices since its transistors are voltage activated compared to bipolar technologies that are current activated.

This portion of the consumed power can also be written as:

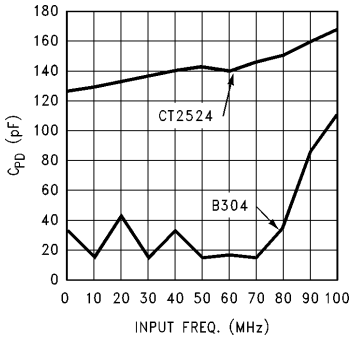
$$P_{Cpd} = C_{pd} * V_{swing} * V_{CC} * f$$

Where f is highest frequency of operating.

The critical parameter in this equation is the actual value for this internal capacitance C_{pd}. This is due to the fact that C_{pd} is a function of the frequency and is mostly a measured value.

While JEDEC Standard Committee suggests measurement of this parameter at 1 MHz, some I.C. suppliers can provide plots of this parameter across frequency which helps for more accurate calculations.

Plot1 is an example of C_{pd} across frequency for two CGS devices. CGS74B304 is a bipolar octal-divide-by-two buffer while CGS74CT2524 is a quad CMOS driver. Notice the difference between the value of this internal capacitance for Bipolar and CMOS devices across frequency.



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Plot 1. Comparison of Bipolar (B304) and CMOS (CT2524) C_{pd}

And finally the power due to the input currents. These currents (I_{INH} and I_{INL}) are in the order of a few micro-Amps for CMOS and milli-Amps for junction transistor devices. In addition to this, in many instances the inputs do not toggle at high frequencies, rather they are mostly static. Therefore, the product of this current and voltage becomes meaningless compared to the total power consumed.

Nevertheless, the formula to calculate this power is very similar to the load equation formula where:

$$P_{input} = \Sigma\, C_{input} * V_{swingH(input)} * V_{swingL(input)} * f$$

for inputs toggling at frequency f.

For most practical purposes this component of the total power is often ignored due to its small size which could be about 1 percent of the whole power consumed.

So what does it all mean? What follows are some typical examples of power calculations for comparison across different device technologies. What must be kept in mind is the fact there still exists some margin of inaccuracy and the system designers need to use a guardband of no less than 5% for obtaining the total power consumed within each unit.

BIPOLAR technologies often have much lower internal power dissipation capacitance due to the fact that they use current for biasing as opposed to voltage, as is the case in CMOS devices. This causes the C_{pd} to be less a function of frequency (as in the Plot 1). In addition, the voltage swings are no more than one V_{be} for most of the nodes. Therefore, the majority of the consumed power can be found in the supply current as well as the output loads. The total power equation can be written as:

$$P_{Total} = \Sigma\,(P_{Load} + P_{Cpd}) + P_{Static}$$

where;

$$P_{Static} = (V_{CC}) * (I_{CC}\ (\text{quiescent})) + (I_{OL} * V_{OL} * DC_{Lo}) + (I_{OH} * V_{OH} * DC_{Hi})$$

$$P_{Load} = \Sigma\,(C_{Load} * V_{swing} * V_{CC} * f)$$

$$P_{Cpd} = C_{Cpd} * V_{be} * V_{CC} * f$$

Here, again C_{pd} must be provided by the manufacturer, while the rest of the parameters in the equation above are under the designer's control.

The V_{swing} (voltage swing across each output) needs to be calculated and it will depend on design parameters such as the termination scheme used as well as the output buffer characteristics. Below is an example of such a calculation.

Here the V_{swing} is the actual voltage swing on each output, and it equals to:

$$V_{swing} = (V_{(HIGH)} - V_{(LOW)})$$

where;

$$V_{(HIGH)} = ((V_{CC} - 2V_{be})$$

$$V_{(LOW)} = V_{OL}$$

Let's use the CGS74B304 device as an example. In order to avoid any reflections and violation of output drive capabilities (I_{OH}/I_{OL}), we will terminate with an equivalent of 200Ω pull-up and 150Ω pull-down resistors.

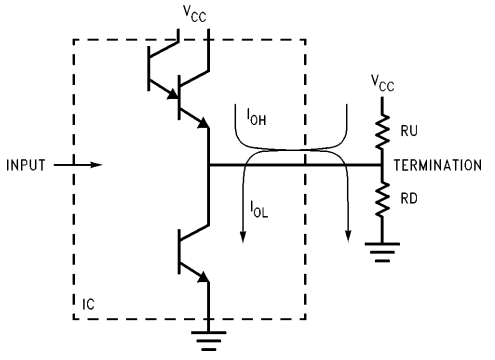

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FIGURE 1. Calculating V_{swing} for a Bipolar IC

Also, we will use a 50 pF capacitive load while driving a 100Ω line and operating at 5.0V V_{CC} with 50% duty cycle input running at 100 MHz (outputs of 50 MHz).

We get;

$$P_{Static} = (5.0V) * ((20 + 42)/2)\ mA$$
$$= 155\ mW \text{ for supply bias,}$$

and as for the terminations;

$$= (I_{OL} * V_{OL} * DC_{Lo}) + (I_{OH} * V_{OH} * DC_{Hi})$$
$$= ((V_{CC} - V_{OL})/R_{up}) * V_{OL} * DC + ((V_{OH})/R_d) * V_{OH} * DC$$
$$= (((5.0 - 0.4)/200) * 0.4 * 0.5) + (((3.6)/100) * 3.6 * 0.5)$$
$$= 4.6 + 64.8\ mW \text{ per output}$$

so the total static load becomes;

$$P_{Static} = 155 + 8 * (69.4) = 710\ mW$$

and for the dynamic portion

$$P_{Cpd} = 20\ pF * 0.7V * 5.0V * 50\ MHz$$
$$= 3.5\ mW$$

also for the loads,

$$V_{(HIGH)} = (5.0 - 1.4)\ V = 3.6V$$

and

$$V_{(LOW)} = 0.5V$$

so the average swing voltage becomes;

$$V_{swing} = (3.6 - 0.5) = 3.1V$$

So the total load power becomes;

$$P_{Load} = \Sigma\ (C_{Load} * V_{swing} * V_{CC} * f)$$
$$= 8\ (50\ pF * 3.1V * 5.0V * 50\ MHz)$$
$$= 310\ mW$$

And ignoring the input dissipation, the total power consumed becomes:

$$P_{Total} = (\Sigma P_{Load} + P_{Cpd}) + P_{Static}$$
$$= 710 + 3.5 + 310 \approx 1024\ mW$$

The case is a bit simpler for CMOS devices. Here again for the ease of calculation we will ignore the power that is consumed due to the output rise and fall transitions as well as the input leakage current.

What makes CMOS device power consumption easier than bipolar is the fact that V_{swing} is actually from supply to ground, that is approximately 5.0V for a CMOS device operating at 5V V_{CC}. So the total power equation can be written as;

$$P_{Total} = (\Sigma P_{Load} + P_{Cpd}) + P_{static}$$

where

$$P_{Load} = \Sigma\ (C_{Load} * V_{CC} * V_{CC} * f)$$

and

$$P_{Cpd} = C_{pd} * V_{CC} * V_{CC} * f$$

so the whole equation for a device with all outputs operating at the same frequency and driving identical loads can be written as

$$P_{total} = ((C_{Total\ load} + C_{pd}) * (V_{CC})^2 * f) + V_{CC} * I_{CC}\ (quiescent) + (I_{OL} * V_{OL} * DC_{Lo}) + (I_{OH} * V_{OH} * DC_{Hi}) + ((V_{CC}) * (I_{CCT}) * DC_{Hi}) * n$$

As an example we will use the CGS74CT2524 which is a 1-4 TTL compatible CMOS clock driver. For comparison we use the same frequencies and loads. That is a 50 MHz input signal with 50% duty cycle driving 50 pF of load per output at 5.0V V_{CC}. The total power consumed will be

$$P_{total} = ((4 * 50) + 140)\ pF * (5.0 * 5.0) * 50\ MHz + 80\ \mu A * 5.0V + 4 * (4.9/200)A * 0.1V * 0.5 + 4 * (4.9/100)A * 4.5V * 0.5 + 1 * 5.0V * 1.5\ mA * 0.5$$
$$= 875\ mW$$

Although the power consumption between these two cases appear to differ drastically, we must note that in the CMOS case we were only driving four outputs versus the eight used in the B304. If this would have been the case, consumed power would have been;

$$Ptotal = ((8 * 50) + 280)\ pF * (5.0 * 5.0) * 50\ MHz + 160\ \mu A * 5.0V + 8 * (4.9/200)A * 0.1V * 0.5 + 8 * (4.9/100)A * 4.5V * 0.5 + 1 * 5.0V * 1.5\ mA * 0.5$$
$$= 1746\ mW$$

In addition, as the toggle frequency increases from 50 MHz the C_{pd} value increases more in the CMOS versus the Bipolar device which remain relatively flat until it seizes to function properly (refer to Plot 1 and the datasheets for the specified maximum frequency of the operation).

ECL devices typically consume less current compared to other technologies as the frequency of the operation reaches 100 MHz or beyond. This is due to the fact that in this technology the transistors do not turn-on completely, and this allows for design which use a lower internal voltage ''swing''.

Additionally, ECL which is another bipolar technology has less junction or internal capacitance compared to CMOS devices.

These lower voltage swings, along with lower junction capacitance helps to minimize if not eliminate the dynamic power consumed due to C_{pd}.

Since the transistors are either completely turned off or are operating in the active region, no simultaneous switching current path exists from the supply to ground (no power consumed due to outputs t_{rise}/t_{fall}).

The critical power component in ECL devices is the power consumed due to the termination network. Most, if not all ECL devices require termination networks to minimize signal reflections as well as getting more predictable DC levels.

The total power consumption formula in the case of the ECL device scan be written as;

$$P_{Total} = \Sigma\ P_{Load} + P_{Static}$$

It can also be written as:

$$P_{Total} = \Sigma\ (I_{AVG} * V_{AVG}) + I_{EE} * V_{EE}$$

where I_{AVG} is the average current through each output and V_{AVG} is the average output voltage. *Figure 2,* below, is an example of such calculation for an output terminated in parallel to −2V.

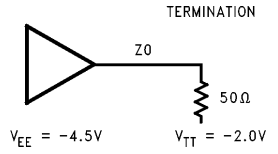

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FIGURE 2. Power Calculations for Parallel Terminated, Single-Ended ECL Device

With a V_{OHC} of −1.035V and V_{OLC} of −1.610V:

$$I_{AVG} = [((-1.035 - (-2.0))/50) + ((-1.610 - (-2.0))/50)]/2$$

$$I_{AVG} = 14.0 \text{ mA}$$

$$V_{AVG} = -1.035 + (-1.610)/2 = -1.3V$$

With a device with typical I_{EE} of −100 mA and four differential outputs, the power can be estimated to be;

$$P_{Total} = 8 * (14.0 * 1.3) + 100 * 4.5 = 596 \text{ mW}$$

For a differential pair this number would have been double this value, which makes it comparable to the bipolar and CMOS devices.

Notice that this number is independent of the frequency of the operation as well as internal capacitance of the unit.

Using different termination schemes changes this consumed power. Table I reflects the amount of the current as well as power used per output for thevenin equivalent termination as shown below in *Figure 3*.

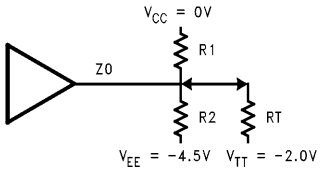

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FIGURE 3. Power Calculations for a Thevenin Equivalent Termination

TABLE I. Comparison of Power Dissipation across Different Termination Resistors

R_T	R_1 = 1.8RT	R_2 = 2.2RT	$I_{EE\ avg}$ mA	$P_{D\ avg}$ mW
50	90	113	28.2	109
62	112	140	22.7	87.9
75	135	169	18.8	72.7
82	148	185	17.2	66.5
90	162	203	15.7	60.5
100	180	225	14.1	54.5
120	216	270	11.7	45.4
150	270	338	9.4	36.3

The case for **MIXED SIGNALS** is a bit more complicated since in most instances both CMOS and Bipolar characteristics are present. Generally Mixed signals are designed such that they use both CMOS and Bipolar internal circuitry for optimizing speed and geometry, while the outputs are mainly of CMOS structure to make them compatible with the outside world.

However, the generic formula can be applied in this case as well, provided that all components of the power equation are calculated and accounted for.

POWER AND TECHNOLOGY

The examples provided previously show that the power consumption is about the same at 50 MHz and 50 pF loads. Hence the designer can look for other factors such as cost, ease of design, and the availability of components.

However, as the frequency and loads increase, the power dissipation does not remain the same across different technologies. The general rule is that CMOS devices consume more power than Bipolar technology as the frequency increases while ECL's power consumption remains relatively flat given the same operating conditions.

For this reason, ECL is the recommended technology quite often as frequencies reach beyond 100 MHz. But due to the fact that not many components need to operate above and beyond this range, designing a few ECL units on boards populated with CMOS and or Bipolar devices becomes cumbersome and difficult. This makes ECL, an acceptable solution once all the components being used on the board are such. As for Bipolar or CMOS, the choices are about the same, except that in many instances CMOS is easier to design with as well as cheaper to manufacture. For this reason CMOS has become the technology of choice for many clock generators. However this paradigm needs to be reviewed due to higher operating frequencies of today's systems. Technologies such as GTL (Gunner Transistor Logic) and or LVDS (Low Voltage Differential Signaling) which are bipolar in core, are gaining some attention due to their better noise margins as well as higher bandwidths.

THERMAL CALCULATIONS

OK, so now we know the total amount of power dissipated within each of our components and throughout the boards, and have designed the optimum power supply for the system. Problems such as the long term reliability as well as the required airflow, if any, need to be considered.

From the power, die and junction temperatures can be easily determined, and knowing these temperatures helps to answer the above questions.

Let's start from a relationship that describes how the power consumed is related to the temperature of the integrated circuits.

The Formula

The formula below allows us to determine the junction temperature of the integrated circuits. Junction temperature is the die junction temperature which is also the temperature that silicon needs to tolerate before irreversible damages such as glassification occurs. This temperature can be given by;

$$T_J = T_A + P_D * (\theta_{JA})$$

Where;

T_J is the junction temperature

T_A is the ambient temperature

P_D is the total power dissipated in Watts

θ_{JA} is the package's thermal resistance from junction to ambient and is in degrees Celsius per Watts.

In the above equation, after calculating the power, all the parameters are known except the junction temperature which can be easily determined.

The thermal characteristics or the resistance of the package in this case as in the case of C_{pd}, needs to be supplied by the manufacturer of the device. This number is typically a function of the air flow, die size and the package type and size.

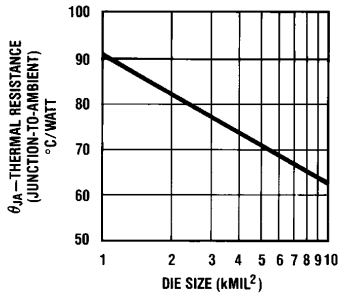
Table II, below, has some typical θ_{JA} numbers for some common packages as a reference (refer to *National Semiconductor Packaging Databook*).

As it can be seen, the package type, die size as well as air flow, play a major role in determining the thermals coefficient of each device.

Once this junction temperature has been obtained one must ask how safe this number is and how it will impact the long-term reliability of the device. But before answering these questions let us briefly discuss the factors that can influence this thermal resistance coefficient.

Die Size

Clearly as die size increases, within the same package, there is more area for the heat to be dissipated. This causes the θ_{JA} to be inversely proportional with the die size as plot 2, below reflects it.



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Plot 2. Thermal Resistance vs Die Size

Lead Frame Material

The material used in the leads and its frame (what connects the die wire-bound to the outside) has a large effect in the thermal resistance of the device since it also acts as a heat sink.

Plot 3, on the following page, compares three common lead frame materials for the same package, across different die sizes. It can be readily seen that copper is a better thermal conductor compared to Aloy42.

Airflow

Another important contributing factor to this thermal resistance. It is obvious that as the air flow increase the thermal coefficient decreases since higher airflow causes more rapid distribution of the ambient within the container, which help to cool the package, as fans do in the real world.

Mounting

Also important is the path for distribution of the heat generated. There exist a difference between board and socket mounted devices as shown by plot 5. With soldered parts the body comes in contact with the board which acts as a heat sink. While the use of sockets will provide an additional path which will limit faster distribution of head into the board. For this reason the board mounted units have better (lower) thermal resistance.

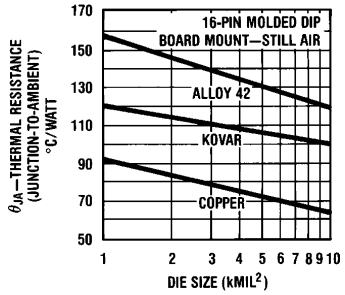
Table II. Thermal Data across Different Package Type

Package Type	θ_{JA} across Airflow (°C/W)					
	Drawing No.	Die Size	0 LFM	225 LFM	500 LFM	1000 LFM
20-Pin SOP JEDEC	M20B	10900	84	60	55	51
20-Pin Ceramic Wide Body	D20A	10000	69	49	41	31
20-Pin SOP EIAJ	M20D	3717	111	97	90	81
20-Pin Molded DIP	N20A	15388	65	49	42	39
20-Pin PLCC	V20A	2444	90	68	60	51

Mold Compounds

Mold compounds play a major role in heat dissipation since each compound has a unique thermal characteristic. Besides the actual amount used in each package type, the kind material used will impact how much and how fast the heat that is generated by the device will get dissipated thru the material used.

Plots below represent such examples.



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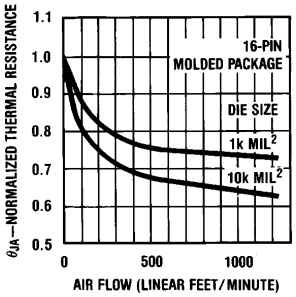
Plot 3. Thermal Resistance vs Lead Frame Material



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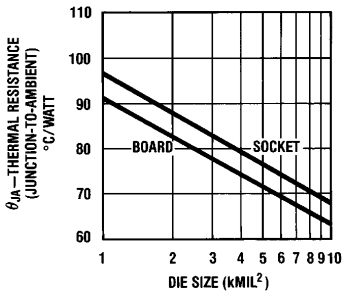
Plot 4. Thermal Resistance vs Air Flow



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Plot 5. Thermal Resistance vs Board or Socket Mount

Reliability

Going back to the original question of what a safe junction temperature is and how it will effect the long term reliability of the unit, we need to define terms such as early life, useful life and wearout life.

But before explaining these terms lets mention briefly what is meant by failure rate. Failure rate is the number of devices which are expected to fail over a period of time. On the other hand, Mean Time Between Failures (MTBF) is the average time that is expected to elapse before a unit is failed and is normally measured in number of hours versus the number of units that is used to measure the failure rate. These two measurements are used quite often interchangeably and are inversely proportional to each other as given below;

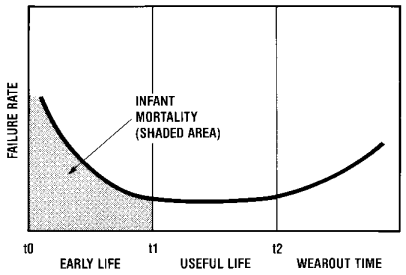
$$\text{MTFB} = 1/(\text{Failure Rate})$$

Going back to different types of failure rates, infant mortality rate, as shown in the shaded area of Plot 6, is mostly influenced by the system and application. Main contributors are electrical overstress and or excessive mechanical stressing of the units. This type of failure is often discovered during the manufacturing process as well as test and burn-in of the integrated circuits and or systems.

However, the other two types of failures are often discovered during the operation life of the units which could prove very costly and must be minimized.

In order to reduce these rates, we must be able to predict their occurrence and relate them their operating environment. For this reason, mathematical models that explain failure rate over time are often used.

One such model is the Arrhenius Model (refer to NSC's packaging databook). This model which is well documented and proven over time assumes there exists a linear relationship between the failure rate and time as well as temperature.



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Plot 6. Failure Rate vs Time

This results in an equation that shows the failure rate at a given temperature is a function of another failure at that temperature.

The ratio of these two failure rates, F, is given by below;

$$F = X1/X2 = \exp [e/K\,(1/T_2 - 1/T_1)]$$

where;

X1 is the failure rate at junction temperature one

X2 is the failure rate at junction temperature two

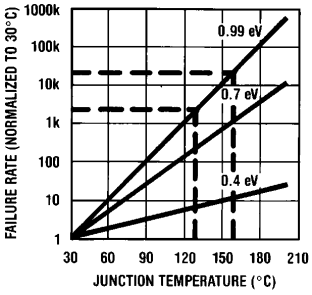
E is the thermal activation energy (eV)

K is the Boltzman constant

What this equation inspires, is the fact that there is a dramatic acceleration effect of the failure rate as the junction temperatures increase. As shown by plot 7.

Therefore, the overall goal of the system designer should be the reduction of the junction temperature of the integrated circuits to achieve the highest reliability of its product.

And as mentioned previously, choosing the right package and the right amount of air flow will determine to reduce this junction temperature which is caused by the total power dissipated within each unit.



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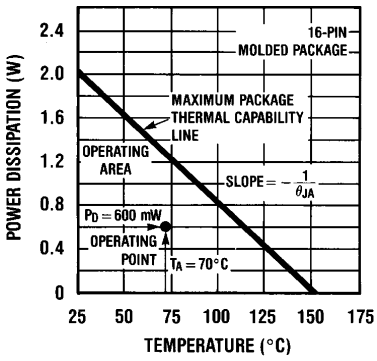
Plot 7. Failure Rate as a Function of Junction Temperature



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Plot 8. Package Power Capability vs Temperature

SUMMARY

In order to design the most cost effective and reliable system, designers need to calculate the power consumption of each component within their system as accurately as possible.

This allows for a better power supply design as well as providing enough airflow for the system to reduce the junction temperatures as much as possible.

Reducing junction temperatures will enhance the reliability and hence the useful life of their designs.

REFERENCES

National Semiconductor Packaging Databook. 1993 Edition, sections 2,3,8.

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LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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