

PCI IDE Application Note

National Semiconductor
Application Note 963
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ERRATA

Description

The current BIOS (AMI, Award) will take Read/Write action towards the "Base Address Register" when it detects the PCI device through the "PCI configuration space" during power-on self-test. Different makers of BIOS will assign different values to the "Base Address Register". However, none of these values can be used as the default value of the legacy IDE HDD device. Which means that the "IDE port I/O space" resident on the chip has been redirected by the BIOS, and the system would not be able to communicate with the IDE device.

The outcome is "System could not boot through IDE HDD". National provides hardware and software solutions and both of them will not have any impact on system performance.

Software Solution

- BIOS needs to be changed
- No changes to software drivers
- No extra glue logic

Typically, BIOS use the "Sub-class code (01h) and program interface register (00h)" to detect whether the attached device is legacy IDE controller chip or not. Currently different BIOS vendors remap IDE's Base Address Register to different address shown in the next table.

National Semiconductor is working with AMI, Award, and Phoenix to get BIOS modified to fix this anomaly.

Here are the required address changes for AMI and Award BIOS.

We suggest that the BIOS vendors make the following changes once the Legacy-mode IDE is detected.

- Keep the "Base Address Register" untouched.
- Write the default address for channel 0 and channel 1 back to the "Base Address Register" once the "Legacy IDE" is detected.

Overview

The hardware patch solution is designed to fix the problem of existing demo boards' incompatibility with existing BIOS. This solution uses a GAL to fix the problem and works with existing BIOS without any power-on procedures. But it requires software changes to run on/off the hardware patch.

Hardware Patch Solution

This document describes how to modify the existing demo board and what software drivers changes are required to turn on/off the software patch.

Hardware Patch

- Requires a PAL
- No BIOS change required
- Wire the following signals to the GAL socket

Pin #	Connect
1	PCI CLK
2	FRAME #
3	IDSEL (from the PCI local bus)
4	C_BE0 #
5	C_BE1 #
6	RST #
7	C_BE2 #
8	C_BE3 #
9	AD7
10	GND
11, 20	VCC
12	IDSEL__OUT (pin-99 or PC87410 "IDSEL")
15	AD6
16	AD5
17	AD4

For more details, please refer to the schematic of PCI-IDE controller with patch logic.

Address Register	Default Value	AMI BIOS	Award BIOS (a)	Award BIOS (b)
Reg. 0 (10h-13h)	00 00 01 F1	00 00 FC F9	00 00 D0 01	00 00 50 01
Reg. 1 (140h-17h)	00 00 03 F5	00 00 FC F5	00 00 D1 01	00 00 51 01
Reg. 2 (18h-1Bh)	00 00 01 71	00 00 FC F9	00 00 D2 01	00 00 52 01
Reg. 3 (1Ch-1Fh)	00 00 01 75	00 00 FC F9	00 00 D2 01	00 00 53 01

Award: a.) version: 4.50 date code: 002194 Pentium-S
b.) version: 4.50 date code: 122793 Pentium

PATCH LOGIC

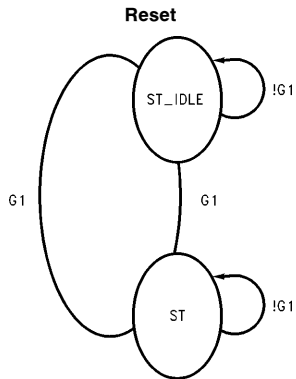
The following is the patch logic for PC87410 PCI-IDE controller with National's OPAL format. The PAL device could be either G16V8 or P16R4. See attached schematics with Patch Logic.

```
begin header
end header
begin definitions
device gal 16v8;
input clk=1, frame=2, idsel=3, cbe0=4, cbe1=5, reset=6, cbe2=7, cbe3=8, ad7=9,
AD6=15, AD5=16, AD4=17;
output (com) idsel_out=12;
feedback st=13, st1=14;
end definitions
{
CLK FRAME IDSEL CBE0 CBE1 RESET
ST ST1 IDSEL_OUT
}
```

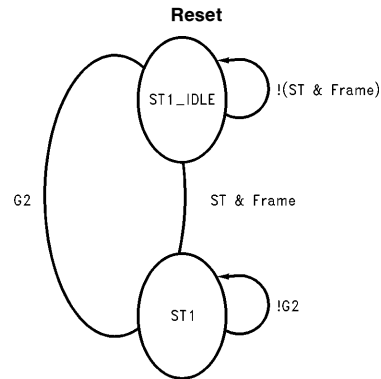
Begin Equations

```
g1 = !frame * idsel * cbe3 * !cbe2 * cbe1 * !cbe0 * ad7;
st := reset * ( st * !g1 + !st * g1 );
{st.re = reset;}
st.c = clk;
g2 = frame * !st;
st1 := reset * ( st1 * !g2 + !st1 * st * frame );
{st1.re = reset;}
st1.c = clk;
idsel_out = idsel * (st1 + ad7 + ad6 + ad5 + !ad4);
End Equations
```

State Machine: Bubble Diagrams for PCI_GAL.OPL

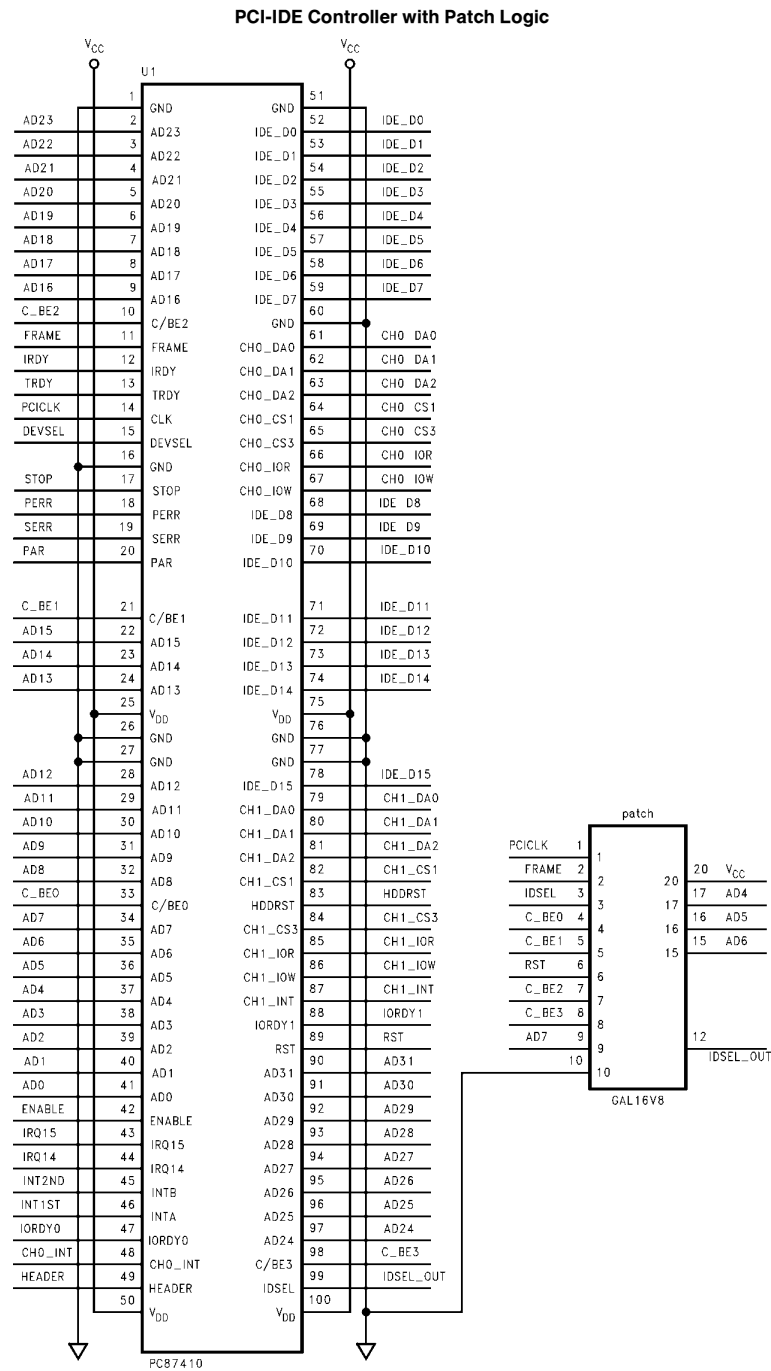


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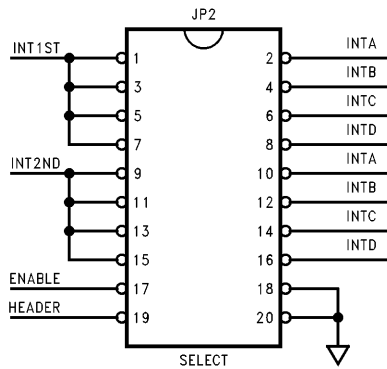
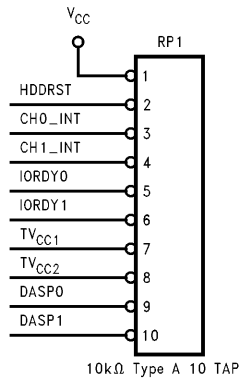
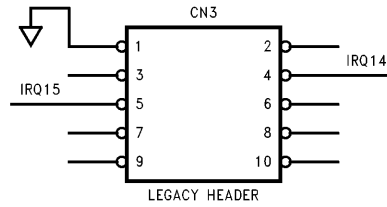
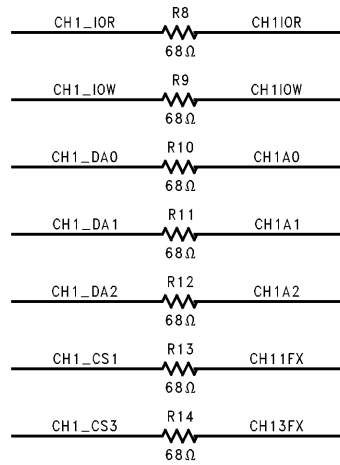
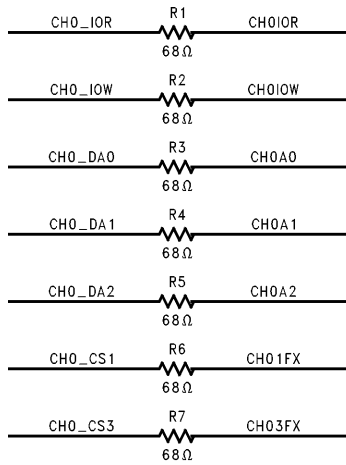
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The schematic with patch logic is as follows:



TL/F/12303-5

PCI-IDE Controller with Patch Logic



TL/F/12303-6

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BILL OF MATERIAL

a. Active Devices

Item	Quantity	Reference	Remarks and Part No
1	1	U1	PC87410 PDI-IDE Controller

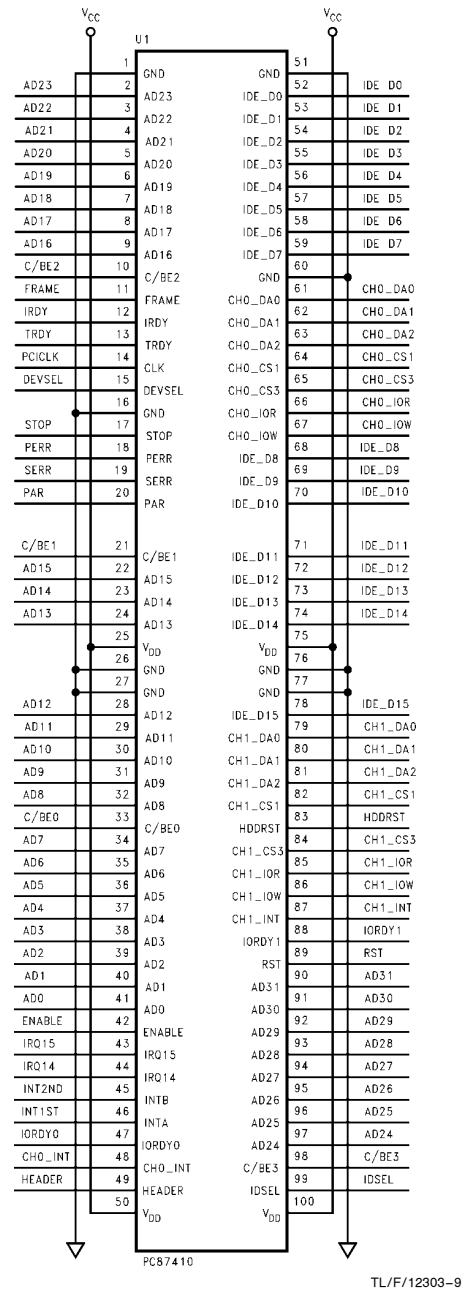
b. Passive Devices

Item	Quantity	Reference	Remarks and Part No
2	1	R1	10 k Ω Type A 10 TAP (resistor pack)
3	14	R1...R14	68 Ω
4	2	R15/R16	270 Ω
5	1	R17	560 Ω

c. Connector

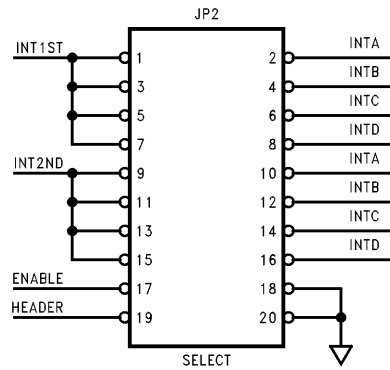
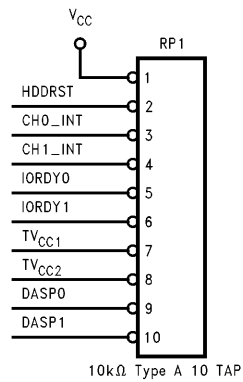
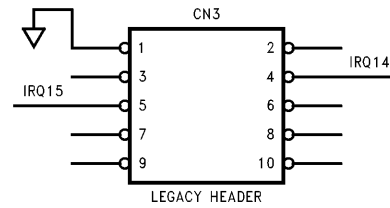
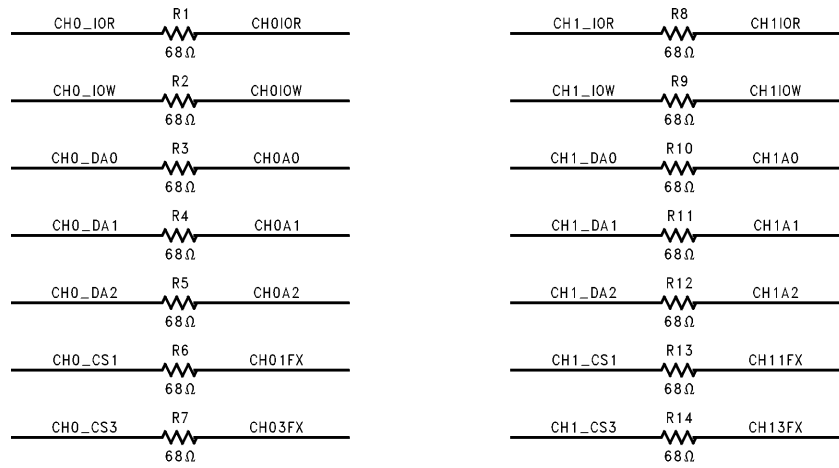
Item	Quantity	Reference	Remarks and Part No
6	1	CN1	IDE Channel 0 2 x 20
7	1	CN2	IDE Channel 1 2 x 20
8	1	JP1	To LED 2
9	1	CN3	Legacy Header 2 x 5
10	1	JP2	Selector for INTA and INTB 2 x 10

PCI-IDE Controller



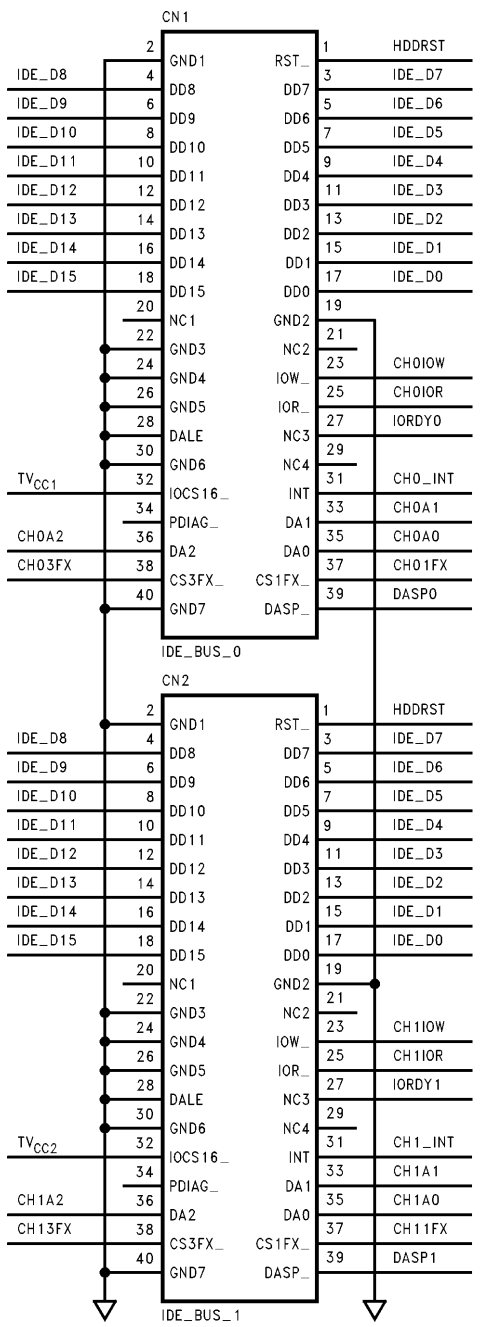
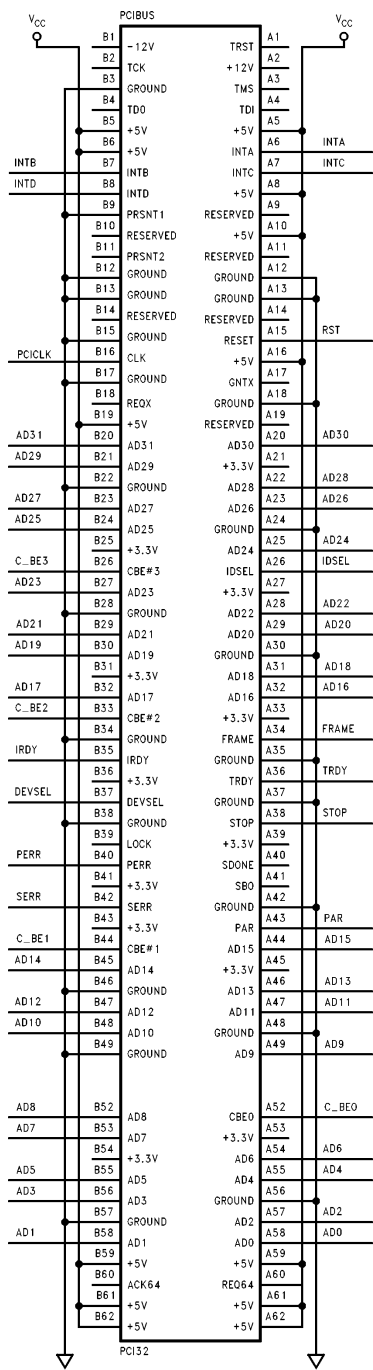
SCHEMATICS

PCI-IDE Controller



TL/F/12303-10

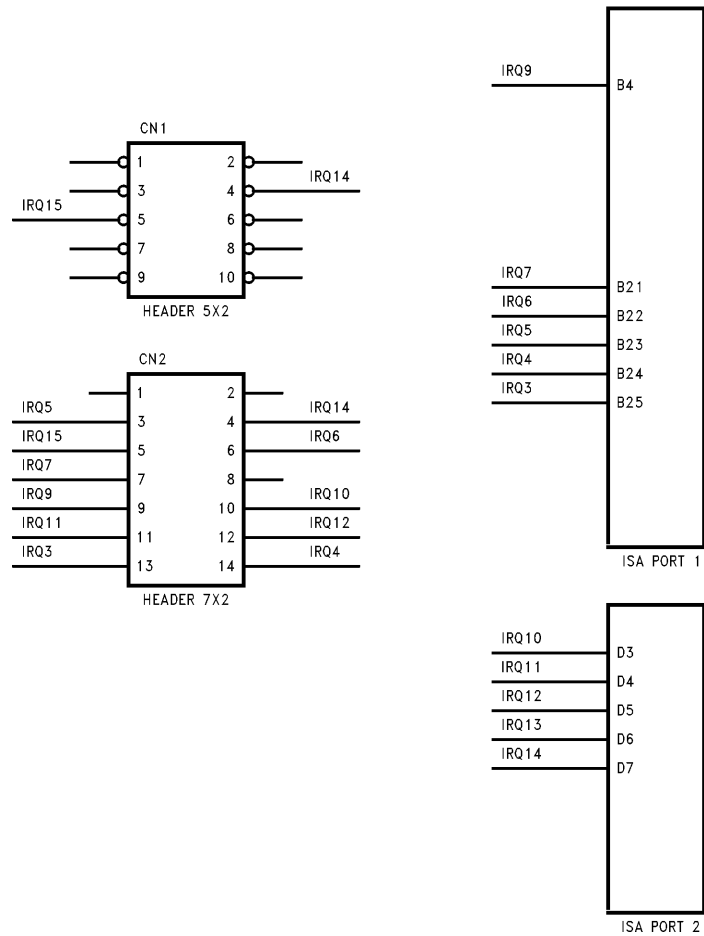
PCI-IDE Controller



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TL/F/12303-11

PCI-IDE Paddle Card



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