How to Design a HiSeC™ Transmitter

National Semiconductor
Application Note 960
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INTRODUCTION

This application note has been written to describe in detail how to design a transmitter using a National Semiconductor HiSeC Rolling Code Generator. This is the first part of a three part series on the RKE system. The second applications note (Application Note 961) explains now to implement a high security receiver. The third applications note (962) explains how to program the HiSeC. After reading the material presented in these application notes, the reader will have a thorough understanding of how to design a high security RKE system using National.

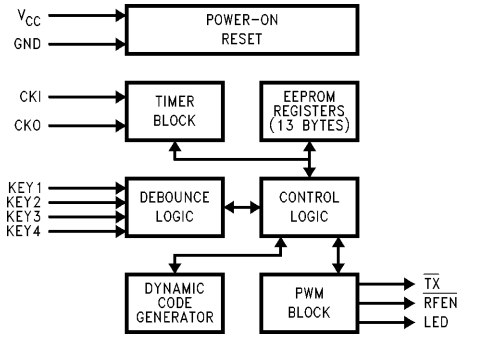

FIGURE 1. Block Diagram NM95HS01A

HARDWARE DESIGN

Figure 2 shows an RF transmitter based on the HiSeC rolling code generator chip. The two key inputs are directly connected to grounded single pole switches. The inputs have internal pull-up resistors to save external components. The part is driven from an RC clock. The LED output is connected to an LED in series with a current limiting resistor. The TX output pin controls the base of an NPN transistor which forms a tuned RF amplifier based on a SAW filter. The RFEN signal is used as the ground pin for tuned RF circuit.

HiSeC SELECTABLE OPTIONS

The HiSeC transmitter has a large number of options to tailor the part to a large number of different applications. This section describes the purpose and use of these options in detail.

BIT CODING FORMATS AND TRANSMISSION POLARITY

Eleven bit coding formats have been included in HiSeC, seven intended for use in RF applications and four for IR applications. For details of the waveforms for each format please refer to the HiSeC Rollong Code Generator Datasheet.

RF coding format 0 has a narrow bandwidth. It is relatively difficult to decode without clock recovery circuits and is difficult to work with during bench testing. However, once the clock has been recovered, decoding is achieved by exclusive ORing the data and clock streams. RF coding format 2, like format 0, has a DC level independent of the message. RF coding format 4 and the IR modes have constant transmit energy per message, assuming that power is transmitted during logic HIGH. RF coding formats 1, 3, 5, and 7 are PWM type formats which are easy to decode. RF format 7 has a low duty cycle allowing the RF transmitter to have a higher peak power. The IR modes are modulated versions of RF coding format 4 suitable for IR applications. The duty cycle and number of pulses allow the user to set the IR power. Note that the high and low bit times within the IR modes and RF mode 4 are different which is important when considering the preamble and NRZ sync timing.

The TxPol bit determines the quiescent state of the TX output line. If it is reset to 0, the quiescent output level is logic LOW. If it is set to 1, the quiescent output level is logic HIGH and the bit coding formats are inverted. TxPol = 0 is used when driving the base of an NPN transistor, TxPol = 1 is used for direct drive of an IR diode in series with a resistor.

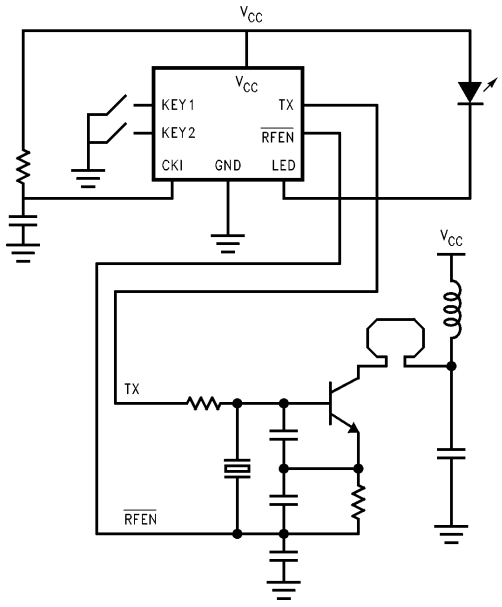

FIGURE 2. RF Transmitter using HiSeC Rolling Code Generator

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USE OF FIELDS IN TRANSMISSION FRAME

It is important to understand the purpose of each different field in the transmission frame before deciding whether to enable or disable this function.

The preamble field, if enabled, is sent on the first frame sent after transmission is initiated. Its purpose is to provide a signal to wake up the microcontroller or decoder in the receive circuit. It has a fixed format of two high bit times at logic HIGH, one low bit time at logic LOW and eight bit encoded zeroes. If desired, it can be sent in complete isolation from the frame by eight low bit times. This is achieved by enabling the sync frame in NRZ mode with contents of 00000000.

The sync field, if enabled, is sent in every frame. Its purpose is to provide a bit timing reference for the rest of the frame. The eight bits sent in the sync frame are fully programmable. The bits are encoded either using the standard bit coding format, or by using NRZ bit coding. For NRZ bit coding, the high bit time is the same as the bit encoded high time, and the low bit time is the same as the bit encoded low time, this point being important to note in cases where the high and low bit times are different, such as the IR modes. If needed, part of the sync field could be used to send key identifier data to either replace or extend the fixed identifier field.

The fixed field, if enabled, is sent in every frame. Its length is 24 bits if the FixSize bit is set to 1 and 20 bits otherwise. The field is sent in the selected bit coding format. Its contents are fully programmable. Its purpose is to provide a unique unencoded identifier for every key to facilitate receiver decoding software and to identify the particular transmitter in applications where one receiver can be used with several transmitters. It can also be used as the basis for a fixed code encoder application. The data field is sent with every frame. This 4 bit field is transmitted using the selected bit coding format. Its purpose is to indicate which keys have been pressed, whether a sync frame is being sent and whether the battery level in the transmitter is low.

The dynamic code field is sent with every frame. Its length is 36 bits if DynSize is set to 1 and 24 bits otherwise. The field is sent in the selected bit coding format. Its purpose is to provide a secure code which changes on every new transmission. Increasing the length gives additional security against random guessing. In a sync frame, this is replaced by a 40-bit initialization field. The parity field, if enabled, is an 8-bit field sent with every frame using the selected bit coding format. The purpose of the parity field is to serve as a check on the data integrity. It is a bytewise exclusive OR of all the bytes in the frame from the sync field to the dynamic code field. If the frame is not byte aligned, the parity field is calculated by zero extending the last four bits with 0000, calculating the bytewise exclusive OR of all the bytes and then swapping the higher and lower nibbles in the result. The stop bit is present in all frames. It is used to delimit the end of the frame for bit fields needing a definite end. For example, the IR modes need this delimiter to distinguish between a 1 and a 0 in the penultimate bit of the frame. For bit coding modes where delimiting is not needed, this bit is read as a 1.

SYNCHRONIZATION

There are two ways of synchronizing the HiSeC transmitters to the receivers: performing forward calculation of the code and secondly, using a sync frame. In forward calculation, the receiver calculates forward for up to a predetermined maximum number of codes (known as the code window) until the code is matched. This simple resynchronization procedure is required in cases where the receiver has missed one or more codes from the transmitter. This could occur if someone presses the keys on the transmitter without aiming at the receiver, for example if someone plays with the transmitter. A second method of synchronization is required if the code window is exceeded. This technique is also used for initialization of a newly installed receiver, for initialization of a transmitter after battery change and for adding or replacing an entirely new key. A sync frame is used for this type of synchronization. Sync frames are generated automatically on the second time any key is pressed after power up. They are transmitted for as long as the key is pressed. If the key is pressed for only a short time, a minimum of four sync frames are sent. If the AutoResync bit in the HiSeC is set to 1, sync frames can be generated on demand. The user must press K1 and K2 for a fixed length of time determined by the output of the third prescaler, typically in the range from 2.5 to 10 seconds. After this time the LED signal goes out. The user releases the keys, then presses any key to generate sync frames. Again, a minimum of four sync frames are sent.

The sync frame transmits enough information for the receiver to completely learn the key for a particular manufacturer code. The receiver software decides under what conditions to accept sync frames and to learn new keys.

The receiver software can easily detect sync frames as the data field is set to all zero implying that no key has been pressed, a condition that is impossible when sending a normal frame.

TIME-OUT

Transmitters based on HiSeC can be protected against premature battery drain caused by a key being held low for a long period which would cause continuous transmission of data frames. If the TIMEOUTEN bit is set to 1 the device will enter HALT mode after a time determined by the output of the third prescaler. Typically, this lies in the range from 20 to 80 seconds. This time-out also applies after battery change and in automatic resync mode if a key is not pressed.

TRANSMISSION INDICATION

The LED and RFEN signals can both be used for indication of transmission. The LED signal is active during a pause, whereas the RFEN signal is active during both frame and pause transmission. The LED signal is also active before the first key press and between the first key release and second key press after power up. This indicates to the user that a key should be pressed. The LED signal only lights during the first pause if the battery is low and the battery detection function has been enabled.

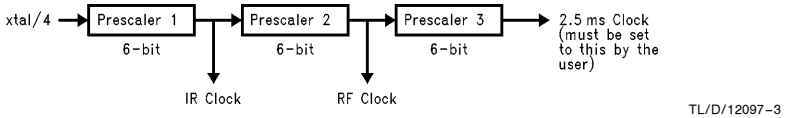

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FIGURE 3. Prescaler Block Diagram

USING THE PRESCALERS

The prescalers allow the user to set the timebase for the bit coding formats. The first prescaler is intended for use with IR applications, the second prescaler for use with RF applications. The third prescaler sets the timebase value for the key debounce, for the AutoResync and for the TIMEOUTEN modes. The SCLK signal selects which clock is used for the bit coding timebase. If SCLK = 0, IRclk is used as the timebase, otherwise RFclk is used. Both timebases can be used for all bit coding formats. For example, IRclk could be used as the timebase for an RF format if the external clock has a very low frequency.

Let the RC or crystal clock frequency be fc and the prescaler division factors for the three prescalers be P1, P2 and P3 respectively.

IR period: IRclk = 4.P1/fc

RF period: RFclk = 4.P1.P2/fc

Debounce strobe = 4.P3.RFclk

AutoResync: ARclk = 4096.P3.RFclk

Time-out period = 8.ARclk

Minimum values of P1, P2 and P3 are **2.** Minimum value of IRclk or RFclk is **12/fc.**

The prescalers are loaded with (Pn-1). E.g. to get divide by 10 on prescaler 1, load it with 10−1 = 9.

As an example consider bit coding format 5 with a bit time of 1 ms using a 4 MHz resonator. The required RFclk by referring to datasheet for RF bit coding format 5 at 1 ms is 1 ms/3 = 333 μs. Using the RFclk equation gives P1.P2 as 333 i.e., P1 = 37 and P2 = 9. So load Prescaler 1 with 37 − 1 = 36 and Prescaler 2 with 9 − 1 = 8.

The AutoResync period is adjustable in steps of 4096.RFclk = 1.36 seconds, starting at 2.73 seconds. The time-out period is 8 times this and is thus adjustable in steps of 10.9 seconds starting at 20 seconds.

LOW BATTERY DETECTION

Low battery detection is enabled by setting the CompEn bit to 1. The threshold is selected by using the BattType bit. If BattType is 1, the threshold is set for 6V batteries, otherwise for 3V batteries. The data field is set to 1111 on alternate frames if a low battery level is detected. Additionally, the LED only lights on the first pause after transmission starts and is out on following transmissions to indicate low battery level to the user.

CONCLUSION

The above sections have described how to design a transmitter using a National Semiconductor HiSec rolling code generator and a generic RF module. It has been demonstrated how the rolling code generator can offer high security in small PCE applications.

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