National's Burst EPROM Is the Only Non-Volatile Memory on the Market Today That Is Fast, Has Low Power Consumption, and Is Cheap

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ABSTRACT

This application note demonstrates the advantages National Semiconductor's Burst EPROM Family (NM27P68K, NM27P600, NM27P960) will give a system designer over various competing memory solutions. Atmel's high speed (64k x 16) EPROM, 4 interleaved EPROMs (32k x 8) with 4 multiplexers, 4 of Cypress' Burst PROMs (16k x 16), and an EPROM (64k x 16) shadowed by SRAM (64k x 16) will be examined as alternative solutions. An in-depth examination of power consumption, access time, cost, and processor performance will provide the necessary metrics to judge NSC's Burst EPROM.

NM27B210

National's Burst Family is a new high performance EPROM Family capable of synchronous "burst" accesses. Two basic read modes of operation are used to access data. The first read mode of operation is a simple (non-burst) access to memory. This type of access can be accomplished by any standard EPROM. This mode will produce one word (16 bits) of data for each address submitted. The second read mode of operation is a "burst" mode. Simply described, a "burst" access produces four words of data for each address presented. There will be some initial latency before the first word will become available, however each of the following three words will be supplied at a rate of one word per clock cycle.

ACCESS TIME

National's Burst Family is capable of "bursting" 4 words of data (4-1-1-1) to a microprocessor running at 33 MHz *(see Figure 1)*. This translates to 4 words of data in 210 ns. In comparison, Atmel's high speed EPROM (t_{ACC} = 55 ns) will output data in a (3-3-3-3) sequence and will take 360 ns. Four of Cypress' burst PROMs are capable of outputing the same amount of data in 150 ns using a (2-1-1-1) sequence. A fast SRAM can produce 4 words of data in 240 ns using a (2-2-2-2) profile. Finally, 4 interleaved EPROMs with glue logic can deliver the same 4 words in 300 ns using a (5-1-3-1) arrangement. Only 4 of Cypress' Burst PROMs are quicker than National's Burst memory. However, Cypress' memory solution is an order of magnitude more expensive than National's Burst memory and it consumes 8.3 times more power than National's Burst memory. This makes National's Burst memory the class of the field. (Please see Table I.)

PROCESSOR PERFORMANCE

Motorola's Ron Stence has done extensive analysis on how different memory access arrangements affect Motorola's 68040 processor (see Table I and Graph 1). In *The Computer Applications Journal*, (November 1993) Stence states that certain points should be considered in making a memory access as efficient as possible. He explains that the most crucial element is the first access. Insertion of an additional clock cycle during the first access will typically incur a 3% degradation in the processor's performance. The next critical point is the second access. When the second access is delayed by too many clocks, a bubble can occur in the instruction pipe. This will degrade the possible performance of the machine. A third point that Stence feels should be considered is the total number of clocks for the complete transfer. This boils down to pure access speed. The memory must be able to get information to the processor fast enough that the processor's idle time is minimal. National's Burst (4-1-1-1) memory access only degrades a 68040 0.3%. (Please see Table I.)

POWER CONSUMPTION

Low power consumption is one of the chief concerns for a system designer who is working on an application that runs on batteries. The end user no longer is satisfied with short battery life. He wants to take his PDA, Laptop, and cellular phone everywhere and not worry about battery life. For this reason National's Burst Family was designed to have the lowest power consumption possible. Compared to the other memory solutions National's Burst Family easily has the lowest power consumption. (Please see Table II.) Power consumption is calculated below.

POWER CALCULATIONS

Power Consumption = [((I_{CC} active) × (V_{CC}) × (Number of Clocks) × (Clock Period)) + ((I_{CC} standby) × (V_{CC}) × (Number of Clocks) × (Clock Period))]

4 of Cypress' Burst PROMs = [((700 mA) × (5V) × (5) × (30 ns)) + 0] = 52.5 × 10E-7 Watt Seconds

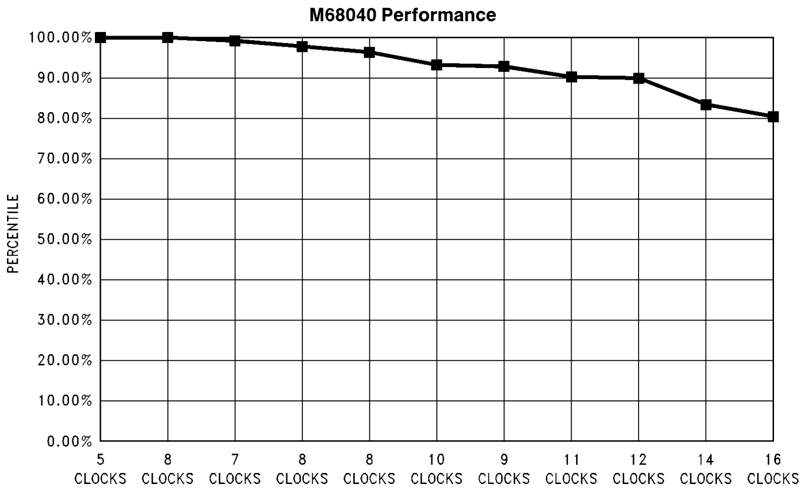
SRAM + EPROM = [((220 mA) × (5V) × (8) X (30 ns))] = 26.4 × 10E-7 Watt Seconds

Note: This calculation does not include the power consumed by the transfer of the EPROM's data to the SRAM. This transfer would take a minimum of 196,608 clock periods, during which time both the SRAM and the EPROM would be in active mode drawing a combined 260 mA.

National's Burst Family = [((60 mA) × (5V) × (7) × (30 ns)) + 0] = 6.3 × 10E-7 Watt Seconds

Atmel's high speed EPROM = [((80 mA) × (5V) × (8) x (30 ns)) + ((17 mA) × (5V) × (4) × (30 ns))] = 10.6 × 10E-7 Watt Seconds

4 Interleaved EPROMs + 4 Muitiplexers + GAL22V10 = 4 × [((25 mA) × (5V) × (10) × (30 ns))] + 4 × [((20 mA) × (5V) × (10) × (30 ns))] + [((90 mA) × (5V) × (10) x (30 ns))] = 40.5 × 10E-7 Watt Seconds



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GRAPH 1

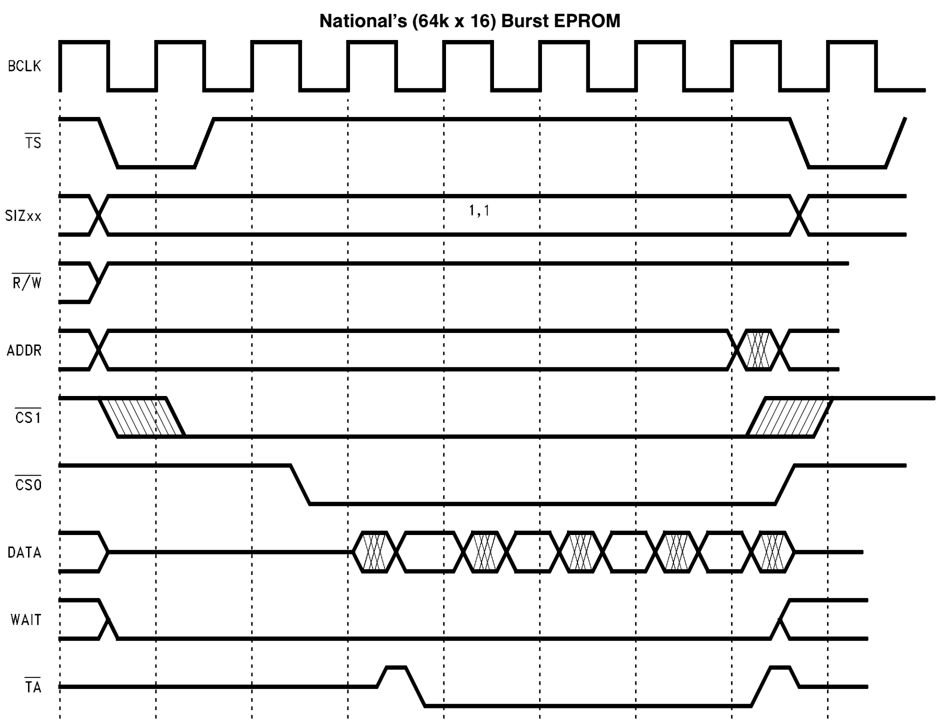

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FIGURE 1

TABLE I

Memory Access	Total Number of Clocks	M68040 Performance
2-1-1-1	5 Clocks	100.00%
2-2-2-2 No Burst	8 Clocks	100.00%
4-1-1-1	**7 Clocks**	**99.70%**
4-1-2-1	8 Clocks	97.90%
5-1-1-1	8 Clocks	96.70%
4-2-2-2	10 Clocks	93.40%
5-1-3-1	9 Clocks	92.90%
5-2-2-2	11 Clocks	90.10%
3-3-3-3 No Burst	12 Clocks	89.10%
5-3-3-3	14 Clocks	83.40%
4-4-4-4 No Burst	16 Clocks	80.20%

TABLE II. Competitive Snapshot

Alternate Solutions	4 Word Memory Access	Clock Periods	4 Word Access Time*	Processor Performance	4 Word Read Power Consumption	I_{CC} V_{CC} Active Current	I_{SB} V_{CC} Standby Current	End User Cost
Atmel's Fast (64k x 16) EPROM	3-3-3-3	12 Clocks	360 ns	89.80%	1.7X	80 mA	8 mA	3X
4 Interleaved EPROMs (32k x 8) with 4 Multiplexers	5-1-3-1	10 Clocks	300 ns	92.90%	6.4X	270 mA	85 mA	3.5X
Fast SRAM/ DRAM and EPROM	2-2-2-2	8 Clocks	240 ns	100.00%	4.2X**	220 mA	75 mA	9.3X
NSC's Burst (64k x 16) EPROM	**4-1-1-1**	**7 Clocks**	**210 ns**	**99.70%**	**X**	**60 mA**	**2 mA**	**X**
4 of Cypress' Burst of PROMs (16k x 16)	2-1-1-1	5 Clocks	150 ns	100.00%	8.3X	700 mA	50 mA	12X

*Bursting processor speed = 33 MHz.

**This calculation does not include the power consumed by the transfer of the EPROM's data to the SRAM. This transfer takes a minimum of 196,608 clock periods while both the SRAM and the EPROM are in active mode drawing 260 mA.

CONCLUSION

It should be concluded from the above analysis that National Semiconductor's Burst EPROM family offers a system designer high performance without high power consumption. Further, the low cost makes its use almost mandatory when compared to other memory solutions.

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