National's "Burst" EPROM Simplifies Designs and Improves Performance When Interfaced with Motorola's 68040/68060

National Semiconductor
Application Note 955
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June 1994

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INTRODUCTION

National Semiconductor's NM27P68K is a new high performance "Bursting" EPROM. Due to its high performance, low power consumption, and a space saving PLCC package, it is an ideal substitute for interleaved EPROM memory schemes which aim at providing bursting memory solutions at the expense of glue logic, board space and high power consumption. It also eliminates the need for expensive, power-hungry SRAM.

BURSTING

"Bursting" refers to a method used for memory accesses that begin with an initial seed address. A memory system capable of "bursting" will provide a significant improvement in the access time of subsequent addresses following the initial seed address.

NM27P68K FEATURES

— 64k x 16 organization
— Support for 25 MHz and 33 MHz system frequencies
— Burst transfer at the rate of 4-1-1-1
— Support for slower systems through a single "Wait" pin
— Automatic generation of Transfer Acknowledge ("$\overline{TA}$" signal)
— Automatic detection of transfer error ("$\overline{TEA}$" signal)
— Eliminates the need for SRAM, interleaved EPROMs, and high speed Expensive/Complex EPROM solutions
— Configurable CMOS/TTL output levels via independent power pins

NM27P68K APPLICATIONS

— High Speed Laser Printers
— Networking
— PDA's
— Settops
— All applications implementing lookup tables in ROM

68XX040—NM27P68K

Figure 1 represents a typical wiring diagram of a 68040-based system using NM27P68K to implement a high speed burst interface in between.

As illustrated, NM27P68K sits gluelessly on the Processor bus and all that is required for the burst interface is to generate the two chip-selects ($\overline{CS0}$ ans $\overline{CS1}$) needed and if necessary, the "Wait" signal.

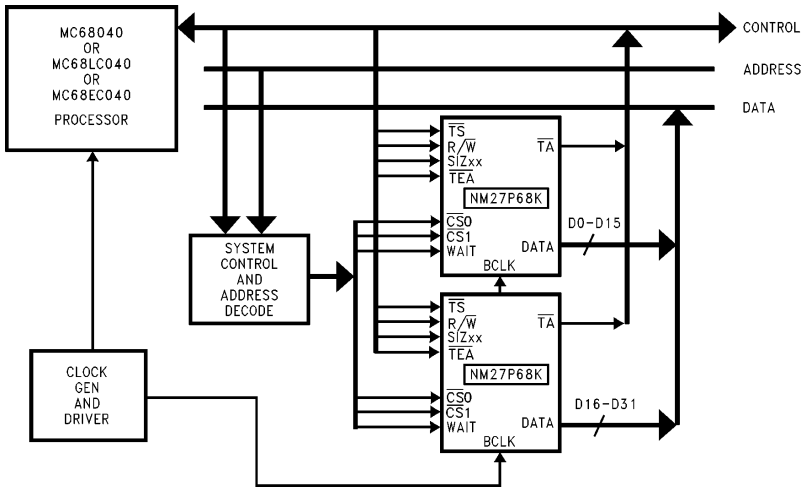
SIGNAL DESCRIPTION

Transfer Start ($\overline{TS}$)

The 68040 asserts this TRI-STATE® bidirectional signal for one clock period to indicate the start of each transfer. The NM27P68K decodes all I/O data using $\overline{TS}$ and the rising clock edge as a reference time.

Transfer Acknowledge ($\overline{TA}$)

This TRI-STATE bidirectional signal indicates the completion of a requested data transfer operation. During transfers by the 68040, $\overline{TA}$ is an input signal from the NM27P68K indicating completion of the transfer. During alternate bus master accesses $\overline{TA}$ is normally tri-stated to allow the NM27P68K to respond, and the 68040 samples it to detect the completion of each bus transfer.



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RRD-B30M75/Printed in U. S. A.

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Transfer Size (SIZ0 and SIZ1)

The 68040 can use the transfer size (SIZ0 and SIZ1) to determine whether it wants one 16-bit word or a ''burst'' (four 16-bit words) by manipulating these signals. (See Table I.)

TABLE I

SIZ1	SIZ0	Data Size	EPROM Action
0	0	Long Word	One 16-bit Word
0	1	Byte	One 16-bit Word
0	0	Word	One 16-bit Word
1	1	Line ''Burst''	Four 16-bit Word

Transfer Error Acknowledge ($\overline{TEA}$)

$\overline{TEA}$ is an error signal which indicates that an invalid bus operation or error condition has occurred. The NM27P68K uses $\overline{TEA}$ as a synchronous reset. $\overline{TEA}$ going active low at the rising edge of BCLK while $\overline{TS}$ is active, will result in the current bus cycle being terminated, resetting the state machine, and awaiting input for the next state from the microprocessor. (See Table II.)

TABLE II

TA	TEA	Action Taken
0	0	Retry Operation
0	1	Data Accepted
1	0	Bus Error
1	1	Insert Wait State

Transfer Slow Down (Wait)

The insertion of wait states is controlled by the Wait pin. The Wait pin is a one clock look-ahead into the system to see whether or not data should be read on the next rising edge of BCLK. If the system is not ready to accept data, the Wait signal should be held high. This action will cause the NM27P68K to wait and drive $\overline{TA}$ high for the next clock cycle. The system will therefore not try to read the data lines.

For fastest operation, just ground the wait pin to V_{SS}. This will ensure that the NM27P68K will operate in the fastest mode possible. (See *Figures 2* and *3*).

Burst Cycle with No Wait State

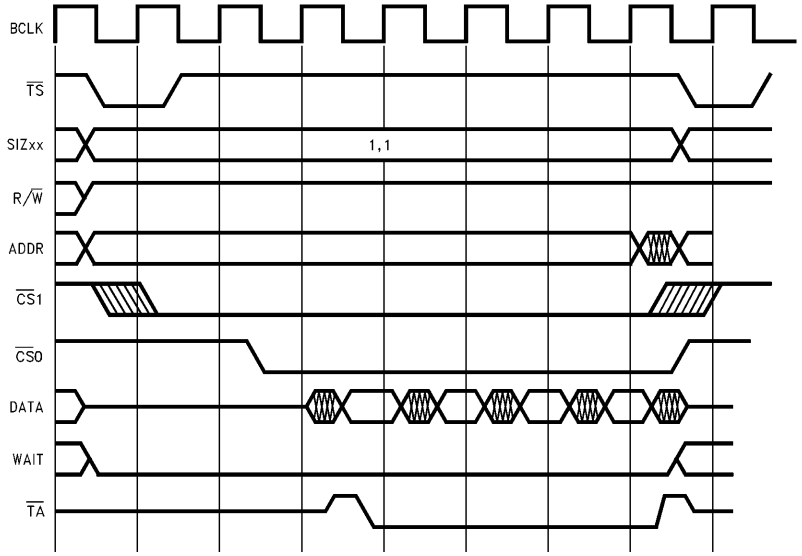

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FIGURE 2. Timing Diagrams/Details (Burst Transfer Without Wait States)

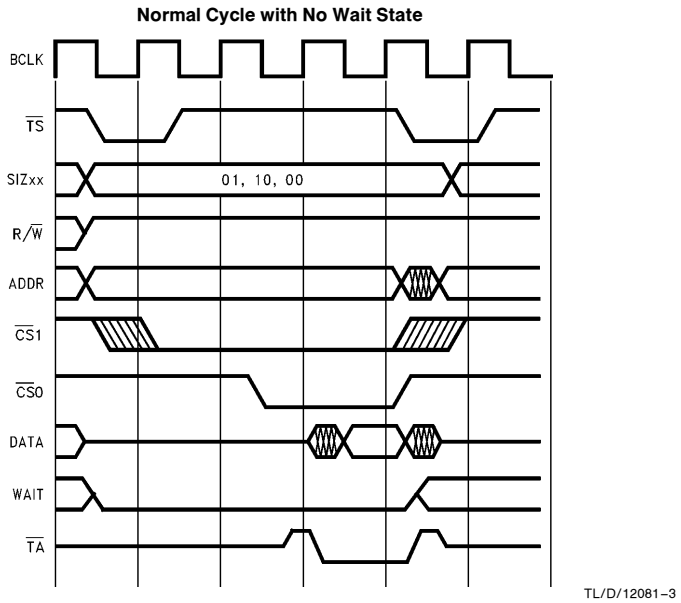

FIGURE 3. Normal (Non-Burst Transfer Without Wait States)

During ''Burst'' read operations, the Wait pin operates no differently. Wait states can be inserted anytime during the memory read. (See *Figures 4, 5, 6*).

Chip Selects (CS0, CS1)

These two signals can be hooked directly to two high order address bits for operation without address decoding.

Read/Write (R/W)

Active high input indicates a read cycle. While active low input indicates a write cycle. (See timing diagrams for additional information.)

BCLK

Memory Bus Clock is a synchronous input which controls the EPROM operation. Can accept CLK inputs up to 33 MHz.

A2–A17

Address Inputs

D0–D15

16-bit Data Bus

V_{CCIO}

The V_{CCIO} pins are used to configure the output levels between CMOS and TTL.

$V_{CC}/V_{PP}/V_{SS}$

5V power supply. Programming voltage pin. Ground.

Burst Cycle with Wait States (5-3-1-1 Pattern)

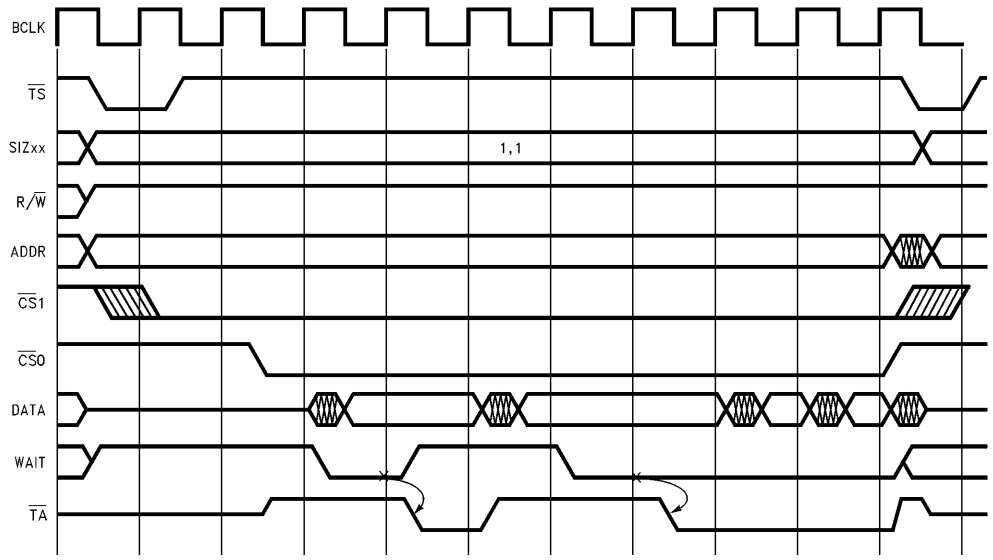

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FIGURE 4. Burst Transfer With Wait States

Normal Cycle With One Wait State

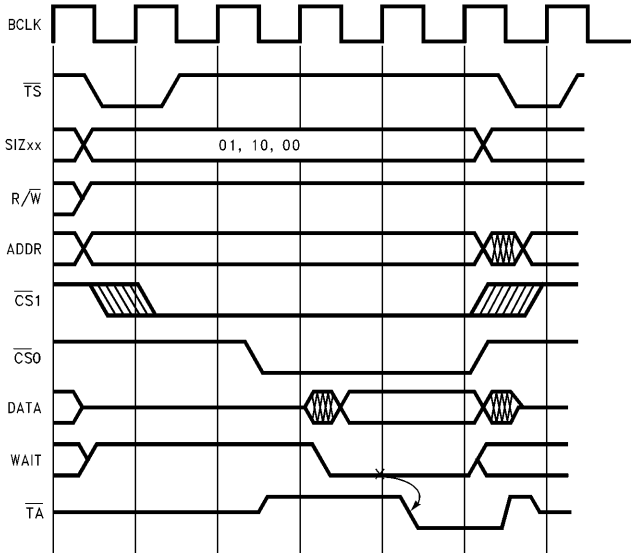

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FIGURE 5. Normal Non-Burst Transfer With Wait States

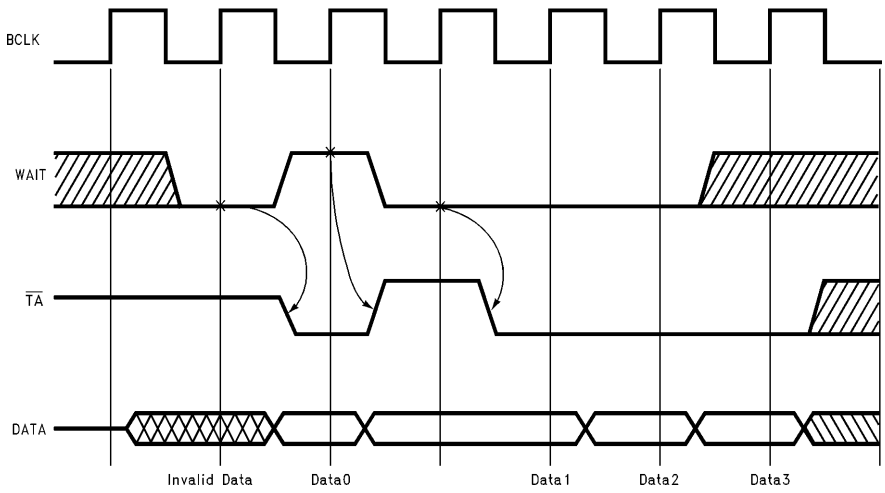

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FIGURE 6. WAIT vs TA

CONCLUSION

It should be concluded from the above analysis that National Semiconductor's NM27P68K offers a system designer high performance without glue logic or high power consumption. Further, the low cost makes its use almost mandatory when compared to other memory solutions.

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