Radiation Design Test Data for Advanced CMOS Product

National Semiconductor
Application Note 925
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ABSTRACT

Radiation test data is presented for different radiation environment as performed on National Semiconductor's FACT™ Advanced CMOS microcircuit family. Over twenty device types have been evaluated by independent investigators, users and by National.

INTRODUCTION

The increased economic pressures of a decreased U.S. military and space budget have forced equipment manufacturers to reevaluate their radiation-hardened designs. They are seeking cost-effective alternative solutions that retain the radiation-hardness assurance integrity of their systems. The FACT logic line is ideal for a wide application of radiation-hardened designs, from tactical to space environments. Data in this paper demonstrates the comprehensiveness and radiation performance of the FACT family. As a result of these attributes, users have a wide product portfolio and full applications support for FACT JAN S RHA-qualified products.

PROCESS DESCRIPTION

FACT product is fabricated on a DESC-certified JAN Class S process line at National Semiconductor in South Portland, Maine. The thin epitaxial layer [n-type-<100>] is 7.5 μm to 8.0 μm thick with a resistivity of 0.008 to 0.25Ω cm. No special process techniques are used to radiation harden the manufacturing process. The P-well design uses a self-aligned, single polysilicon gate with a double-level metallization. After gate oxidation, only low-temperature processing is employed. The gate oxide thickness is 250 angstroms. The passivation layer is PECVD [plasma enhanced chemical vapor deposition] silicon nitride. Final test is in accordance with the Defense Electronic Supply Center [DESC] certification requirements for MIL-M-38510 Level S [for space applications] and Level B [for military applications] process flows. *Figure 1* represents the cross section of the process.

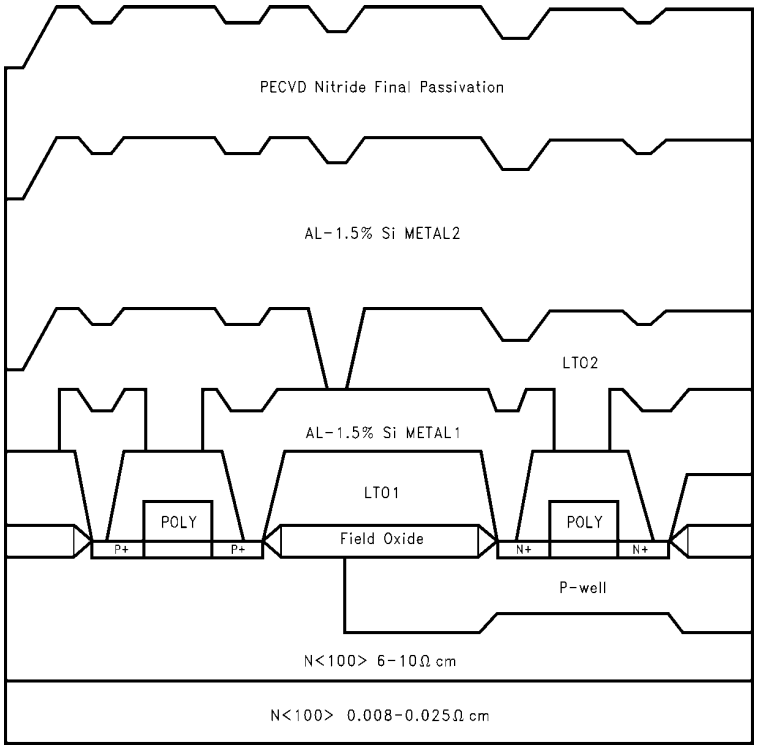

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FIGURE 1. Process Cross-Section

RADIATION TEST ENVIRONMENTS AND FACILITIES

A. Total Ionizing Dose Testing

Total ionizing dose testing was performed at National Semiconductor's Radiation Effects Lab [REL] in South Portland, Maine. This facility is one of only two total dose test facilities in the United States with a DESC laboratory suitability status. The REL was recertified in June 1992. Its gamma source is licensed by the Nuclear Regulatory Commission of the United States and certified by the National Institute of Standards and Technology [NIST]. These certifications assure that data is fully recognized by all government agencies, their contractors and sub-contractors.

Total dose testing is performed at the facility using a self-contained dry Cobalt-60 source, manufactured by Atomic Energy of Canada, Limited. The present dose rate for this gammacell is 110 rads(Si)/s. The gamma ray field is generated by eight stainless steel rods containing seven Cobalt-60 slugs each. The usable gamma field inside the test chamber is within $\pm 10\%$ of the maximum value at the central field point. In addition, a Secondary Effects Reducer is used inside the gammacell test chamber to maintain the proper radiation energy spectrum during irradiation. This reduces the low-energy dose enhancement.

The test methodology for guaranteeing FACT RHA product begins with a JAN S-fabricated wafer screened to a standby leakage current of less than 100 nA. Radiation test data has shown that wafers with high standby leakage current at wafer sort testing will not yield in a total dose environment. Once a wafer is selected for RHA total dose testing, die are packaged either in ceramic dual-in-line (CDIP) or flatpak packages. Group A electrical parameter testing is performed on the RHA sample lot. Each wafer selected for total dose testing is classified as a wafer lot. Treating a wafer as a lot eliminates variability from wafer-to-wafer or lot-to-lot. Fourteen sample devices are chosen randomly from the RHA sample lot; twelve are irradiated and two are control units. All RHA sample lots have die chosen at the DESC area, defined as that part of the wafer enclosed by $\frac{2}{3}$ of the wafer's radial dimension as drawn from the center toward the edge of the wafer.

Total dose testing on the twelve RHA sample devices is in accordance with MIL-STD-883D, Method 1019. Every product is RHA qualified under worst-case bias conditions for each radiation-sensitive electrical parameter. A radiation-sensitive electrical parameter is any electrical parameter that exceeds its Table I databook limits as a result of being subjected to total ionizing dose environment. At National Semiconductor, each device type is step-stressed in the total dose environment to determine its total ionizing dose response. After each irradiation step-stress level, a Group A electrical parameter test is performed with assigned Post-Irradiation-Parameter Limits (PIPL) for radiation-sensitive electrical parameters. Post-irradiation limits are determined from previous total dose characterization test data. If RHA sample devices pass the post-irradiation tests without parametric or functional failure, the RHA-qualified wafer is wafer-banked for future consumer use.

National Semiconductor's FACT logic is inherently radiation tolerant, versus the more expensive radiation-hardened-designed products. National guarantees a 100 krad(Si) Radiation Hardness Assured (RHA) level from certified RHA-banked wafers fabricated on its JAN S process flows. This excludes FACT products manufactured on MIL-STD-883 or commercial process lines.

B. Total Ionizing Dose Results

FACT logic product is in the process of being qualified to the JAN-RHA standard, total dose radiation level "R" (100 krads(Si)). It must be noted that National Semiconductor only subjects its JAN-certified FACT wafers to radiation testing. Total ionizing dose test results show two radiation-sensitive electrical parameters: standby leackage current (I_{CC}) and TRI-STATE® leakage current (I_{OZ}). I_{CC} is the maximum leakage current the V_{CC} pin draws with preset input conditions and all outputs unloaded. I_{OZ} is the maximum leakage current flowing through the disabled TRI-STATE output when a specified output voltage is applied.

These leakage currents are affected in the total dose environment due to radiation-induced leakage current paths generated during radiation exposure. Radiation-induced parasitic leakage paths occur due to an unhardened field oxide around the n-channel devices of a particular product type. FACT product uses a P-well design for n-channel MOSFET fabrication. As a result, two radiation-induced parasitic leakage paths are created in the field oxide. The first radiation-induced leakage path occurs between the source and the drain of the n-channel device and under the polysilicon gate along the edge of the MOSFET. This establishes a radiation-induced parasitic field oxide MOSFET which goes from enhancement mode to depletion mode. This occurs as the charge trapped in the field oxide increases with total dose until saturation. The second radiation-induced parasitic path occurs between the n-channel source and the reversed-biased n-type Epi/substrate. This is difficult to measure and predict, but significantly contributes to the overall radiation-induced leakage current within the entire device type [2]. These two parasitic leakage current sources generate the non-linear I_{CC} curves shown in *Figures 2* and *3*.

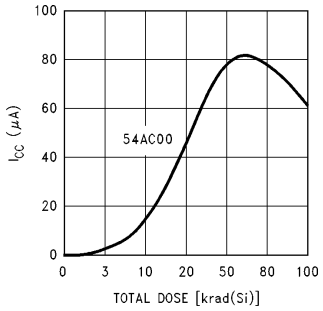

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FIGURE 2. Typical Total Dose Performance—54AC00

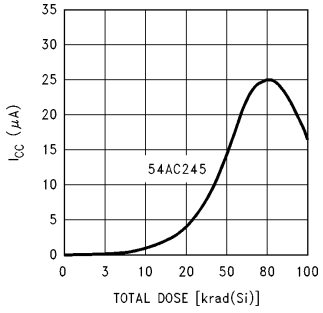

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FIGURE 3. Typical Total Dose Performance—54AC245

I_{CC} current will peak at a given total dose level and then decrease with further total dose accumulation. It is believed that this reduction in radiation-induced leakage current is caused by the field oxide becoming saturated. As it can no longer generate more trapped holes for a given volume, generation of interface states begins to dominate in the field oxide at the higher total dose levels. Trapped holes become neutralized by the radiation-induced interface states, reducing parasitic radiation-induced leakage currents. The field oxide's radiation-induced parasitic leakage paths occur with moderate dose rate irradiation. In a low dose rate (e.g., space environment), the magnitude of leakage currents is reduced significantly; its associated peak value occurs at lower total dose levels. Tables I and II summarize FACT product and the parametric degradation that occurs during total ionizing dose testing. These degraded values represent worst case.

TABLE I. Radiation Tolerant Qualified FACT AC Product (Worst Case)

Exceptions: Parameters Which Do Not Stay within Pre-Rad Values.

Device Type	Parameter	@3 krads (Si)(μA)	@10 krads (Si)(μA)	@100 krads (Si)(μA)
54AC00	I_{CC}	15	75	500
54AC02	I_{CC}	15	75	500
54AC04	I_{CC}	15	75	500
54AC08	I_{CC}	15	75	500
54AC10	I_{CC}	15	75	700
54AC02	I_{CC}	15	305	700
54AC20	I_{CC}	15	75	500
54AC32	I_{CC}	15	75	700
54AC74	I_{CC}	15	75	500
54AC86	I_{CC}	50	200	500
54AC138	I_{CC}	15	305	1000
54AC151	I_{CC}	15	75	500
54AC161	I_{CC}	15	75	1000
54AC240	I_{CC}	15	100	500
	I_{OZ}	1	23	20
54AC244	I_{CC}	15	100	500
	I_{OZ}	1	10	20
54AC245	I_{CC}	15	100	500
	I_{OZ}	1	3	20
54AC273	I_{CC}	75	350	
54AC273	I_{CC}	15	75	500
	I_{OZ}	1	3	20

TABLE II. Radiation Tolerant Qualified FACT AC Product (Worst Case)

Exceptions: Parameters Which Do Not Stay within Pre-Rad Values.

Device Type	Parameter	@3 krads (Si)(μA)	@10 krads (Si)(μA)	@100 krads (Si)(μA)
54ACT00	I_{CC}	15	75	500
54ACT109	I_{CC}	15	75	500
54ACT138	I_{CC}	15	200	1000
54ACT151	I_{CC}	15	100	500
54ACT153	I_{CC}	15	350	700
54ACT175	I_{CC}	15	75	500
54ACT244	I_{CC}	15	100	2000
	I_{OZ}	1	3	20
54ACT245	I_{CC}	15	350	2500
	I_{OZ}	1	3	20
54ACT373	I_{CC}	15	100	700
	I_{OZ}	1	3	20
54ACT521	I_{CC}	15	75	500
54ACT825	I_{CC}	15	75	500
	I_{OZ}	1	3	20

Figures 4 and *5* represent the radiation response of individual MOSFETs threshold voltage variations for p- and n-channel devices. It is important to understand these responses in order to control the process relative to radiation-induced defects. *Figure 4* represents the p-channel device's radiation response. This shows the device is driven toward more enhancement with increasing total dose accumulation, e.g., the threshold voltage becomes more negative as the quantity of trapped holes increases in the gate oxide due to further total dose accumulation. The rate of change for the p-channel threshold voltage occurs faster than the n-channel device during total dose exposure. *Figure 5* shows the total dose response for an n-channel device. Initially, the threshold voltage of the n-channel device goes toward the depletion mode of operation as the total dose accumulation is increased. At lower total dose levels, positive trapped charge in the n-channel gate oxide dominates the rate of change and direction (negative) of the threshold change. However, at higher total dose levels, threshold voltage begins to go in the positive direction or ''rebounds''; the n-channel device starts to become more ''enhanced''. The positive increase in the n-channel device's threshold voltage results from generation of interface states dominating at the higher total dose levels. Interface states dominate at higher dose levels since no more trapped holes can be generated due to limitations of gate oxide volume, e.g., it is saturated with trapped holes. *Figure 5* does not show the actual rebound effect; none have been observed up to a level of 300 krads(Si).

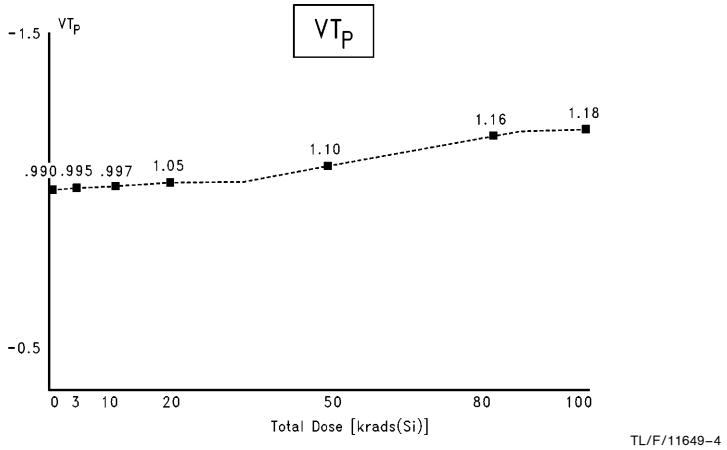

FIGURE 4. Total Dose Response, P-Channel MOSFET

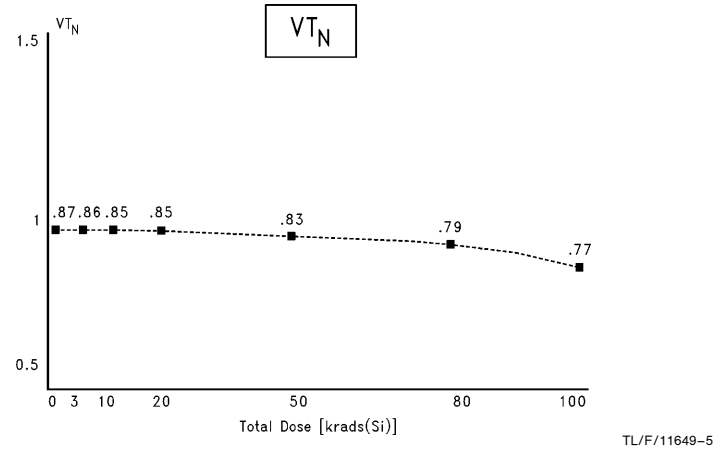

FIGURE 5. Total Dose Response, N-Channel MOSFET

Recently, MIL-STD-883D, Method 1019.4 was implemented for performing total ionizing dose testing. The new method is a conservative approach in simulating the total dose environment in space. The new methodology requires a high dose rate (50 rads(Si)/s–300 rads(Si)/s), unless otherwise specified. It also requires irradiation to 1.5 times the specified total dose level followed by post-irradiation Group A tests at 1.0 and 1.5 times the specification limit. If all RHA sample devices pass post-irradiation parametric and functional tests, devices are placed under worst-case bias at a temperature of +100°C ±5°C for one week (168 ±12 hours). At the end of the one-week accelerated temperature anneal, devices are again tested for post-irradiation parametric and functional tests. *Figure 6* depicts typical radiation response of the FACT 54AC00 (Quad 2-Input NAND Gate) when employing this new method, 1019.4. *Figure 7* represents the typical radiation response of the 54AC299 (8-Input Universal Shift/Storage Register with Common Parallel I/O Pins). Note that I_{CC} for both devices recovers significantly as a result of the accelerated aging procedures of the new method. In general, based on recent testing, most FACT product types recover and pass pre-irradiation worst-case values, typically less than 1 μA. At a 100 krads(Si) specified total dose, a small amount of interface states is generated. Since interface states affect channel mobility, and therefore propagation times, it is expected that propagation times will increase with increases in interface state accumulation in the gate oxide. However, this does not occur with FACT products at the 100 krads(Si) level (verified by observing propagation time deltas of less than 1 ns after performing the new method). Typically propagation time delta values are 300 ps–500 ps at the 100 krads(Si) level.

The switchpoint of an integrated circuit is important to a circuit designer, particularly its radiation response to total dose environment. *Figure 8* shows the typical radiation response of a 54AC08 Quad 2-Input AND Gate's switchpoint. The switchpoint degrades very slowly with total dose accumulation. At a 100 krads(Si) total dose level, the switchpoint delta voltage is 140 mV_{DC}. This degradation affects the edge rates of the function's output waveform. Because many different sizes and types of transistors are used in the function's design, the switchpoint's degraded value represents the sum effect of the MOSFETs threshold voltage changes. Other circuit parasitic effects are caused by the total dose environment.

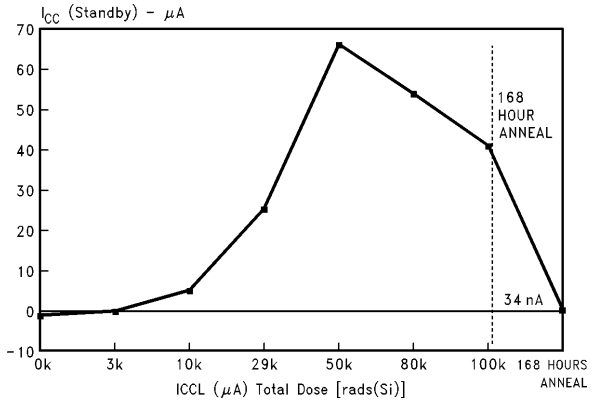

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FIGURE 6. 54AC00 Radiation Accelerated Anneal Evaluation

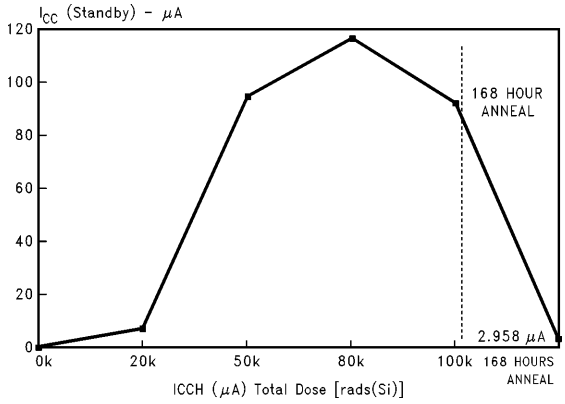

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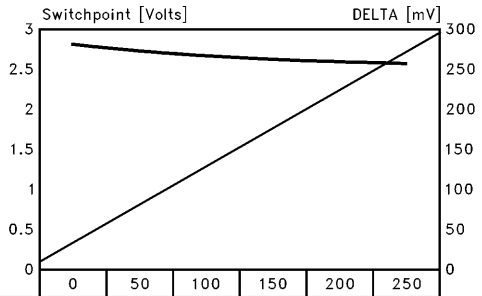
FIGURE 7. 54AC299 Radiation Accelerated Anneal Evaluation



	0	50	100	150	200	250
Switchpoint	2.8	2.71	2.66	2.61	2.58	2.56
SIGMA (+)	2.81	2.72	2.66	2.61	2.59	2.57
SIGMA (−)	2.8	2.7	2.65	2.6	2.57	2.55
DELTA [mV]	0	92	150	200	224	247

Total Dose [krads(Si)]

Inputs = High, Dose Rate = 129 rads(Si)/s.

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FIGURE 8. Switchpoint Degradation—54AC08

Variations of the radiation response between different FACT product types occurs for these reasons:

- FACT product does not use radiation-hardened design rules for circuit layout. Different MOSFET designs are used, i.e., serpentine layout and ''waffle-type'' layout. It is believed the n-channel waffle layout has more edge leakage in a total dose environment.
- The boron out-diffusion along the n-channel edge under the polysilicon gate. Even though Statistical Process Control [SPC] is employed throughout the FACT fabrication process, those process parameters which are radiation sensitive must required control mechanisms. National Semiconductor is developing an RHA Statistical Process Control program which will identify radiation-sensitive process parameters and generate the SPC control limits required to yield more consistent RHA product.
- MIL-M-38510 allows RHA-qualified product to be selected from any position on the wafer. It has been observed that RHA product selected outside the DESC required ⅔ radius has a worse radiation response than product selected within the DESC area. This radiation response variance is because die on the outside ⅓ radius of the wafer have their gate oxide and field oxide more severely overstressed from high electrical fields caused by process steps such as plasma etching. At National, all RHA-qualified product comes from within the DESC-required area for total dose testing.

C. Low Dose Testing

Low dose rate testing was performed at the University of Lowell's radiation facility in Lowell, Massachusetts. Their Cobalt-60 source was located in a water pool adjacent to a wall; steel plate covered the aperature. A low-energy dose enhancement plate was placed between the test units and the Cobalt-60 source aperature. Devices-under-test were located at a pre-determined distance from the source in order to receive the proper dose rate; this rate was verified by dosimetry measurements. The dose rate used in this total ionizing dose testing was 200 rads(Si)/hour. The total accumulated dose was 110 krads(Si).

Three National Semiconductor FACT part were investigated: 54AC245DMQB Octal Bi-directional Transceiver with TRI-STATE Inputs/Outputs, 54AC244DMQB Octal Buffer/Line Driver with TRI-STATE output, and 54AC240DMQB Octal Buffer/Line Driver with TRI-STATE outputs. The sample size consisted of one control unit and five devices-under-test. Input pins were biased HIGH (5 V_{DC}), V_{CC} = 5 V_{DC}, and output pins were unloaded for all device types. *Figure 9* shows the radiation response to low dose rate for the 54AC240DMQB; this represents the worst-case response of the three device types.

Review of the radiation response curve shows the I_{CC} current peaked at 32.5 μA; this peak occurred at 17.4 krads(Si) total dose level. When this radiation data was compared with high dose rate data, several differences were observed. The magnitude of the I_{CC} current was reduced by a factor of 10X in the low dose rate environment as compared with the high dose rate value. Another observation is that the leakage current peak occurred at 17.4 krads(Si) as compared with the high dose rate leakage current peak at 80 krads(Si). Similar differences were observed with the other two product types. I_{OZ} also demonstrated this type of low dose rate radiation response.

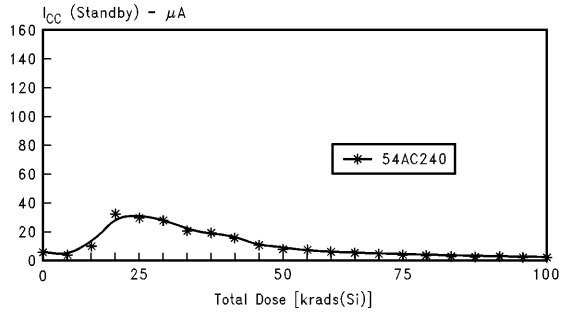

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FIGURE 9. Low Dose Rate Testing Dose Rate—0.055 rads(Si)/s

In a low dose rate radiation environment, interface state generation dominates over trapped hole generation. At low dose rates, oxide-trapped charge is neutralized while the long-term buildup of interface continues to increase. This causes a reduction in the magnitude of parasitic radiation-induced leakage current and a shift in the leakage current peak toward lower total dose levels. As the total dose radiation level increases in a low dose rate environment, the n-channel device's threshold voltage and sub-threshold currents also increase, eventually leading to functional failure. For National's FACT product, this failure level usually occurs between 250 krads(Si) and 300 krads(Si) for 54ACTXXX product; the functional failure level for 54ACXXX devices occurs between 350 krads(Si) and 450 krads(Si). In addition to functional failure occurring at low dose rate, it was observed that timing parameters begin significant degradation at the total dose levels previously mentioned. In tandem, the channel mobility continues to degrade as the generation of interface traps increases.

D. Low Voltage Total Ionizing Dose Testing

With the insertion of VHSIC (Very High Speed Intergrated Circuits) technology into military and space systems, the use of low voltage power products will also be required. These low voltage power systems provide an output voltage range of 3.0 V_{DC} to 3.6 V_{DC}. FACT AC product is specified with a V_{CC} range between 2 V_{DC} and 6 V_{DC}, and can easily be used in low voltage systems.

Reducing a device's operating voltage significantly impacts its total ionizing dose response. Much information exists which demonstrates that total dose damage is dependent on the bias voltages as applied during radiation exposure. Reduction in the device's operating voltage causes reduction in the electric fields of the gate and field oxides. As a result, the efficiency of generating trapped oxide changes and interface states is reduced with a corresponding improvement in the total dose radiation response of the device types.

Figures 10 and *11* show a comparison of the 54AC245 Octal Bi-directional Transceiver with TRI-STATE Inputs/Outputs. Comparing the two standby leakage current radiation response curves, the results indicate:

- A significant improvement in the reduction of I_{CC}.

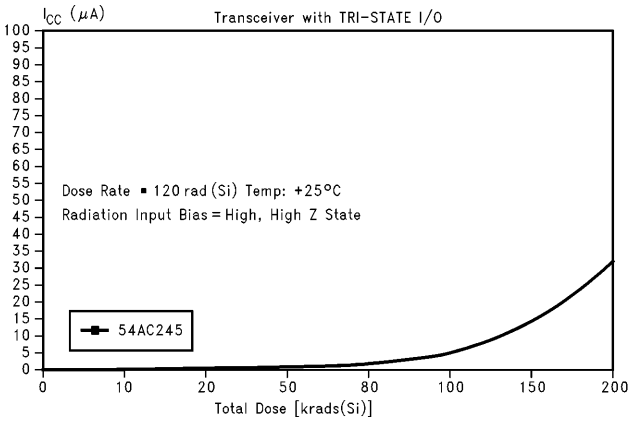

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FIGURE 10. I_{CC} (Standby) vs Total Dose 54AC245—Octal Bi-directional Transceiver with TRI-STATE I/O $V_{IN} = V_{CC} = 3.3\ V_{DC}$

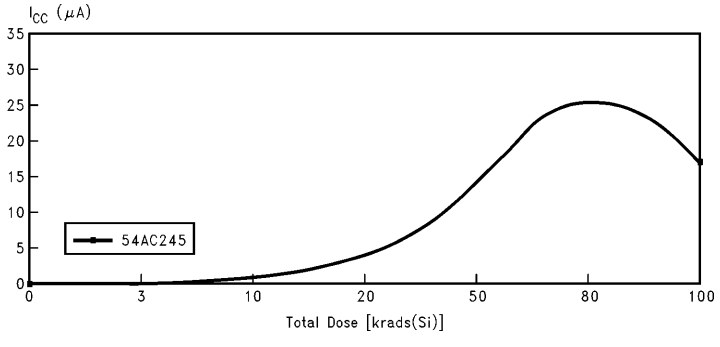

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FIGURE 11. I_{CC} (Standby) vs Total Dose 54AC245—Octal Bi-directional Transceiver with TRI-STATE I/O V_{CC} = 5.5 V_{DC}, V_{IN} = 5.0 V_{DC}

At 0.055 krads(Si)/s, standby leakage current is 31 μA and its peak value is not achieved. Additional radiation response improvements at low voltage include minimization of threshold voltage shifts, reduction in the total dose enhancement of the ''hot electron'' effect and increased latchup immunity in the transient dose rate and single event phenomena (SEP) environments. However, it must be noted that radiation-induced upset in the dose rate or SEP environments is a concern since devices in general become more easily upsetable as the power supply voltage is decreased.

E. Dose Rate Testing

A comprehensive dose rate study has been done on the FACT 54AC299 8-Input Universal Shift/Storage Register with Common Parallel Input/Output Pins. This testing was performed at the Boeing Radiation Effects Lab in Seattle, Washington, using a LINAC (Linear Accelerator) with an energy of 10 MeV. The test investigated latchup immunity using narrow pulse (50 ns) and wide pulse (1 μs) at room temperature (+25°C) and high temperature (+116°C) under static bias. The existence of latchup windows was also investigated. Another portion of the dose rate study investigated the worst-case upset threshold level using narrow pulse (50 ns) and wide pulse (1 μs) at room temperature (+25°C) and low voltage (4.0 V_{DC}) under static and dynamic bias conditions.

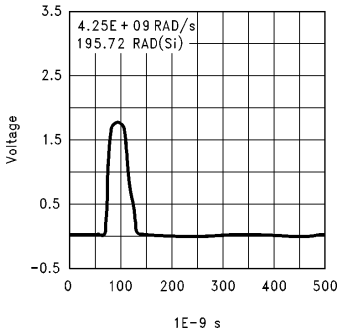
Results of this dose rate study show that narrow pulse (50 ns), high temperature (+116°C) and high operating voltage (5.5 V_{DC}) were the worst-case conditions for latchup immunity testing. No latchup occurred, no latchup windows existed and no burnout was observed up to the LINAC's maximum dose rate (10^{10} rads(Si)/s) at room temperature. Due to the heating circuit used, the highest dose rate was limited to 7.5×10^9 rads(Si)/s at +116°C. Peak surge currents indicated linearity for both narrow and wide pulses. Surge current recovery time was less than 2 μs. Peak surge currents ranged from 300 mA to 1.0A.

Dose rate upset testing results demonstrated that the worst-case conditions are low operating voltage (4.0 V_{DC}), room temperature, and wide pulse (1 μs) under dynamic bias condition with the clock pulse and dose rate pulse being coincident. Under these worst-case conditions, the measured minimum upset level was 1.9×10^9 rads(Si)/s. Another factor affecting upset level sensitivity was the output states of the devices; the worst case was outputs HIGH. *Figures 12* through *14* depict 54AC299 dose rate test data.

The top graph in each column depicts the transient radiation pulse generated by the LINAC. From these graphs, the applied pulse width can be measured. *Figure 13* applied a 1 μs pulse to the device-under-test while *Figures 12* and *14* used a 50 ns pulse. The graphs also indicate the dose rate of each pulse and the total dose value contained in each pulse and the total dose value contained in each pulse.

The second graph in each column depicts the peak surge current measured at the device's V_{CC} pin. In addition to the measured peak current value, the graph demonstrates the measured recovery time. If any of the devices has a latchup condition, the surge current would not have returned to its initial value and maintained a high magnitude.

The last two graphs in each column depict the output state of each device's output pins; only one of the output pins is shown in each graph. With one exception, the output pins change state (i.e., low-to-high, or high-to-low). The bottom graph in *Figure 13* shows an output pin that attempted to change output, but did not. This condition represents a transient upset since it returned to its initial state.



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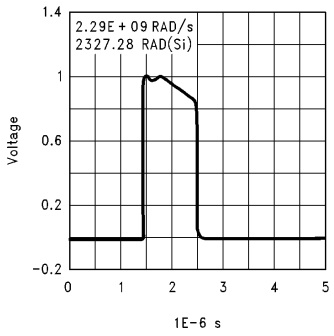

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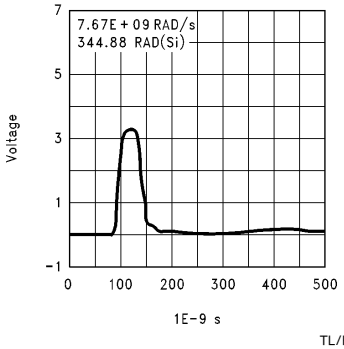

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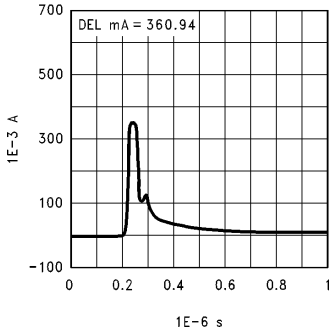

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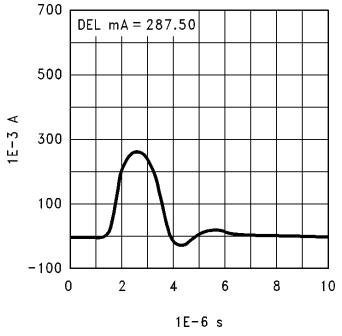
FIGURE 12. National 54AC299 Dose Rate Characterization Upset Threshold Test at +25°C



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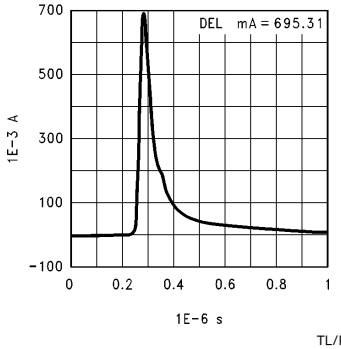

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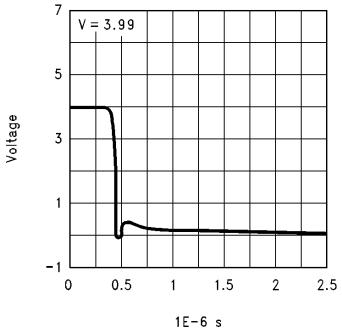

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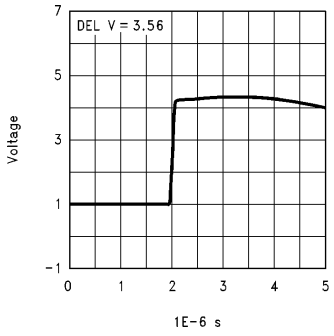

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FIGURE 13. National 54AC299 Dose Rate Characterization Upset Threshold Test at +25°C

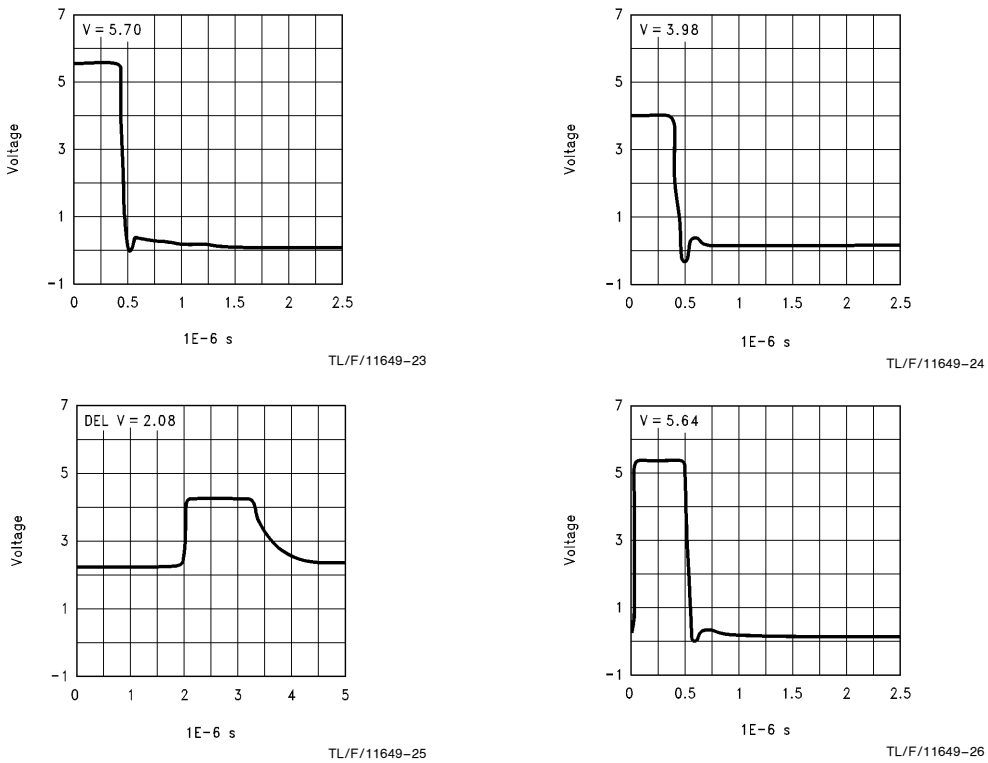

FIGURE 14. National 54AC299 Dose Rate Characterization Latchup Test at + 117°C

F. Single Event Phenomena Testing

Single event effects (SEE) testing was performed by R. Koga, Aerospace Corporation at the Lawrence Berkeley Laboratory's 88-inch cyclotron facility. Six ion species were used: Xe (603 MeV), Kr (380 MeV), Cu (290 MeV), Ar (180 MeV), Ne (90 MeV) and N (67 MeV). Ranges for the ion beams spanned 45 μm for Kr to 130 μm for N [3].

SEE test results show that FACT product manufactured on a JAN S Epi process does not latch up for Linear Energy Transfer (LET) values up to 120 MeV. Therfore, no latchup cross-section was determined. [3] SEE test also revealed various large Single Event Upset (SEU) effective LET threshold values ranging from 40 MeV/mg/cm^2–60 MeV/mg/cm^2. Table III summarizes the SEU susceptibilities for FACT logic [3].

TABLE III. Summary of SEU Susceptibilities for FACT Logic

Device	Data Code	LET Threshold [MeV/(mg/cm^2)]	Saturation Cross-Section (cm^2/device)
54AC163	8909	40	2×10^{-5}
54AC174	8922	55	3×10^{-5}
54AC299	8922	48	3×10^{-5}
54AC374	8840	50	2×10^{-6}
54ACT174	8920	60	9×10^{-5}
54ACT373	8948	40	2×10^{-4}

Figure 15 compares FACT technology with two older technologies, ALS and HCT. *Figures 16* and *17* represent the SEU test results for some of the individual FACT product tested.

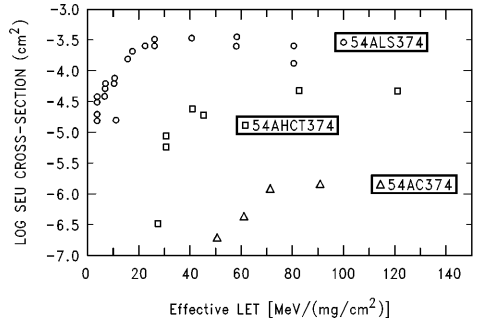

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FIGURE 15. SEU Test Results for 54AC374, 54HCT374, and 54ALS374

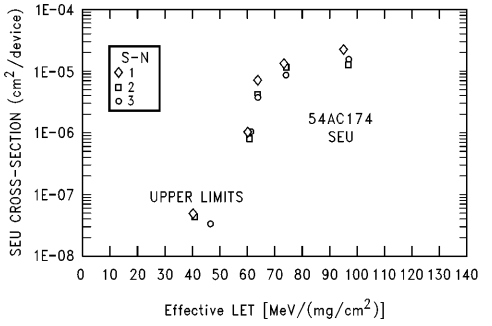

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FIGURE 16. SEU Test Results for 54AC174

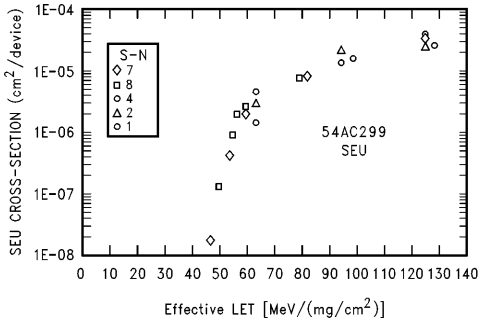

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FIGURE 17. SEU Test Results for 54AC299

G. Proton Testing

Proton testing was conducted at the University of California—Davis, Crocker Laboratory using a 76-inch cyclotron facility. The proton energy is variable from 5 MeV to 63 MeV. Several FACT product types were tested by Naval Research Laboratory personnel for proton upset and proton total dose. The test procedure was to irradiate in step-stress levels and then measure the supply radiation-induced leakage current. [4] Data supplied by NRL was on the 54AC074 Dual D-Positive Edge-Triggered Flip-Flop; testing occurred June 7, 1991. For this test, the proton particle energy was 62.5 MeV/mg/cm^2 with a flux range from 3.61 x 10^8 to 1.91 x 10^9 particle/cm^2/s. The dose rate varied from 0.049 krads(Si)/s to 0.255 krads(Si)/s. The radiation bias was 5.0 V_{DC}. Table IV shows the results of the I_{CC} total dose testing. Neither proton-induced upsets nor latchup were observed.

TABLE IV. Proton Total Dose Response—54AC074

Total Dose [krads(Si)]	Dose Rate [krads(Si)/s]	I_{CC}, Standby Leakage Current [μA]
0		0.0
1.0	0.049	0.0
2.1	0.049	0.0
4.8	0.049	0.0
7.5	0.049	20.7
21.2	0.127	95.1
28.0	0.127	202.0
34.9	0.127	268.0
48.6	0.255	558.0
62.2	0.255	593.0
76.0	0.255	677.0
89.7	0.255	582.0
103.4	0.255	553.0
117.0	0.255	474.0

SUMMARY

Radiation test data has been presented which represents typical radiation responses of the FACT product to the four radiation environments. Knowledge of these radiation responses and understanding the data is important to the circuit designer who selects the most cost-effective components without sacrificing the radiation survivability of the system.

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1. G. Messenger, M. Ash, *The Effects of Radiation on Electronic Systems,* Van Nostrand, Reinhold Company 1986, pp. 283–296.
2. T.P.Ma., Paul V. Dressendorfer, *Ionizing Radiation Effects in MOS Devices and Circuits,* Wiley-Interscience publication, 1989, pp. 179/180.
3. Koga et al., IEEE Trans. Nucl. Sci., NS-37, pp. 1869–1875, 1990.
4. W. Stapor, Naval Research Laboratory, private communication, June, 1992.

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