Designing Systems with the IC/SS Power Line Carrier Chipset

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INTRODUCTION

This application note is comprised of information helpful to designing an IC1SS-based system, including operating environment issues as well as hardware and software system design. It is arranged according to the topics listed below:

THE POWER LINE ENVIRONMENT

Communications over the power line presents a very difficult challenge to the modem designer. The power distribution network is designed to efficiently distribute power at 50 Hz or 60 Hz without consideration of its behavior at communications frequencies. Problems that arise include:

- Severe signal attenuation-impedance effects
- Severe interference such as:
  - — white noise
  - — impulse noise
  - — continuous wave sources
- Line conditions that can vary over time

Impedance Variation

In the frequency range used for IC/SS communication, power line impedance can vary widely. A capacitive load, created by power factor correctors, or filters in electronic power supplies, can produce an impedance at 90 kHz of a few ohms or less. Worse yet, the capacitive load can interact with the inductance of transformers or of the lines themselves to create an LC resonance at the carrier frequency. While at power frequencies, these capacitive loads have little effect, at IC/SS communication frequencies, they can cause problems. The higher currents needed to transmit a given power level into a low impedance line can result in greater resistive losses.

Another cause of very low effective impedance is underground cables in wet soil or under water. Such configurations generate substantial capacitive coupling to ground, and in some cases, considerable dielectric losses.

On the other hand, on an overhead line whose loads are turned off, the modem will see the characteristic impedance of the overhead line, typically around 100 ohms.

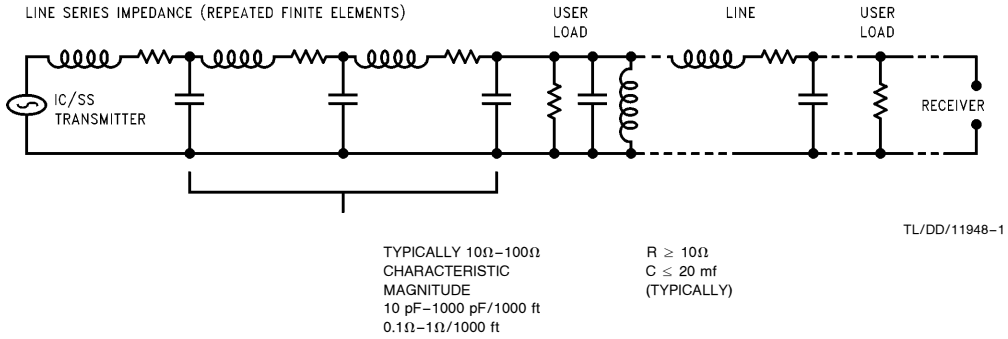

FIGURE 1. The Power Line Environment

When a line consists of an underground section followed by an overhead section, the impedance discontinuity at the junction will create reflections. These will have the effect of attenuating the signal. Situations where the overhead and underground segments alternate down the line are particularly troublesome. Each interface can produce a signal attenuation of 20 dB or more.

When these series impedances are combined with shunt loads, the result is more attenuation.

The net effect is that reliable power line communications requires a dynamic range of 90 dB, and a drive circuit which is capable of operating efficiently into a complex impedance ranging from 1Ω to 100Ω, and at any phase angle.

Noise Considerations

The designer needs to become concerned with three different types of noise on the power line: white noise, continuous wave interference, and impulsive noise.

Impulsive noise results from switching of inductive loads and can produce impulses saturating any receiver for periods of tens or even hundreds of microseconds. These impulses may have very rapid rise times, and are virtually impossible to filter out completely. Furthermore, if the front-end and coupling circuitry of the receiver are not designed with great care, it will ring in response to these impulses, at least when coupled to some line impedances, resulting in long periods of lost communications. These impulses are generally periodic with the power line, 100 Hz or 120 Hz, and many may occur during each half cycle, due to the switching of various loads.

Worse yet, these impulses are capable of ringing the power line itself. Because the network and its attached loads possess both inductance and capacitance, they may resonate at a frequency which depends on the instantaneous load, producing decaying ringing waveforms lasting several cycles at frequencies in the communications band. To the modem this looks like continuous wave jamming, at frequencies which cannot be predicted in advance because they vary with load conditions.

Finally, white noise is an issue, particularly when operating at the high levels of receiver gain that can be required.

A power line modem must operate well with respect to the classical criterion of bit error rate vs signal/noise ratio with Gaussian noise. However, it is a mistake to base an evaluation of modem performance solely on the classical criterion. The need to avoid continues-wave noise and the highly nonlinear nature of the impulse noise place demands on the filter configurations employed, and the behavior of the system in that situation.

Multipath Effects

Many power distribution systems are gridded, meaning there may be more than one path to a given point. The different paths may result in partial cancellation of the received signal due to phase differences caused by different path lengths to the same point. Signal propagation velocities vary widely with the lossiness of the transmission line. However, one can expect a 180 degree phase shift in 5000 feet (1500 meters) at 10 kHz and 500 feet (150 meters) at 100 kHz (using 0.1c as a typical propagation velocity).

Such difference in path lengths can be expected in gridded distribution systems. And because variations in loads change the effective electrical path length, any power line modem that is connected to another by roughly equal signal paths might receive equal signals at opposite phases, resulting in nearly complete cancellation.

THE IC/SS ADVANTAGE

To optimize communications in this harsh environment of the power lines, IC/SS technology incorporates many techniques which overcome power line noise. They are:

Adaptive Frequency Hopping: IC/SS communicates on one of four channels at a time, using non-coherent FSK modulation. The chip set can frequency hop based on changing noise and attenuation conditions. It only frequency hops when required, and this function is totally transparent to the user. No user involvement is necessary.

Adaptive Bit Rate: As noise levels rise, IC/SS automatically lowers the bit rate over the power line. Each time this happens, the modem doubles the signal energy per bit, giving it a better chance of getting through the noise. Your fax machine operates using the same principle: Over a noise-free telephone link, the system operates at perhaps 9600 bps. If you get a noisy phone link, the system operates at 1200 bps. The IC/SS system can use 3200, 1212, 800, and 400 bps. There is eight times the signal energy per bit at 400 bps than 3200 bps. Again, this happens automatically.

Error Coding: IC/SS uses an industry standard CRC-24 error checking code. This meets the recent IEC (IEC 870-5-1) specification for error coding.

Overlay technique: IC/SS uses a sophisticated data overlay technique. It saves good bytes in each message, and if there is an error, retransmits the packet. The software overlays the retransmitted packet over the good bytes previously saved. Using this technique, the software can build a good packet of data quickly, and efficiently, without ever getting an error-free packet. This is a powerful technique to combat noise spikes which typically corrupt bytes of data on an infrequent and random basis.

CENELEC A compliance: IC/SS was designed around the CENELEC A band requirements. IC/SS fully meets them in terms of frequency use, power input, out of band noise requirements, etc.

DETAILED SYSTEM DESCRIPTION

This section provides a detailed description of the operation of the IC/SS system, both hardware and firmware. It is necessary background information for the systems engineers, hardware engineers, and software engineers who must integrate IC/SS into a larger system.

Non-Coherent FSK

The IC/SS power line carrier modem uses Frequency Shift Keying (FSK) to overcome problems of the power line environment. FSK functions by assigning one carrier frequency (f0) to the ''0'' binary state or data bit and a second carrier (f1) to the ''1'' binary state. An example of FSK is shown in *Figure 2*. FSK has been shown to perform in cases of CW jamming, under fading conditions, and in the presence of delay distortion.

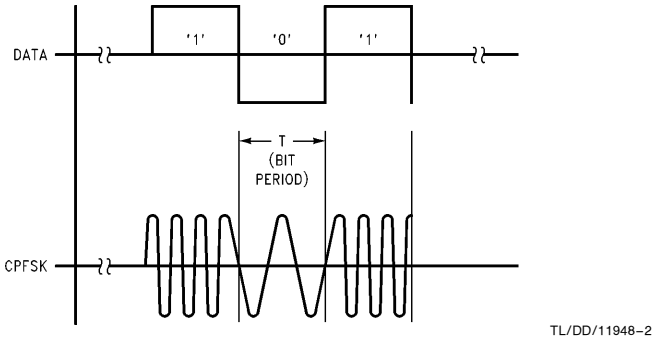

FIGURE 2. A Representation of FSK and its Associated Baseband Signal

Non-coherent FSK, used by IC/SS, uses matched filters consisting of bandpass filters tuned to the signal frequencies, f1 and f0. The signal energy is measured in each filter each bit period.

As the following description of the chip set will illustrate, the chip set consists of a transmitter and a receiver. While bandpass filtering, amplification, and digitizing are done in the analog chip, the received signal is digitally filtered in the digital chip to determine carrier frequency. The digital chip then decodes the message into binary and shifts the received data to the controller.

The transmitter portion of the IC/SS transmitter is more fully described in the next section.

Chip Set Description

This section describes the hardware elements of the IC/SS system in more detail. A diagram showing the functions and interconnecting signals of the various elements appears as *Figure 3*.

The three chips comprising the chip set are:

- System Controller
- Digital ASIC
- Analog ASIC

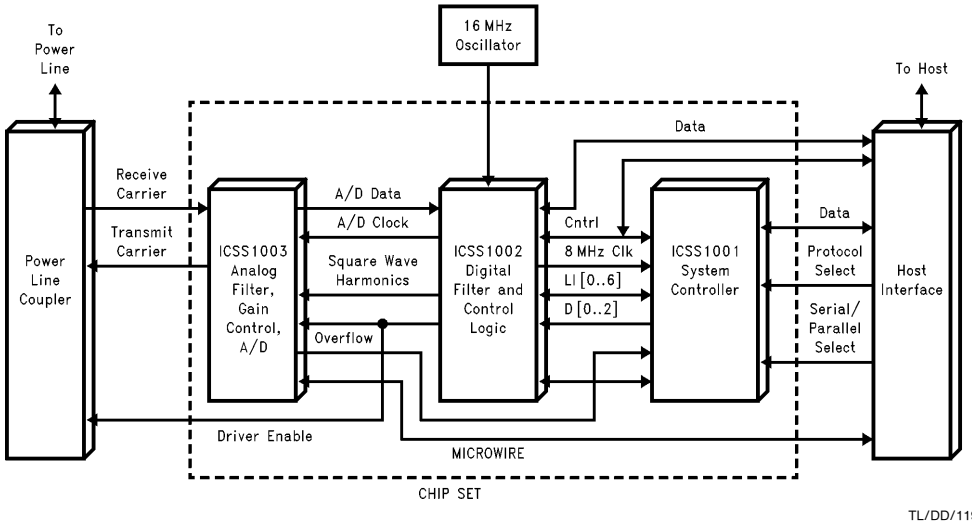

FIGURE 3. Detailed IC/SS Block Diagram

System Controller

The system controller in the IC/SS chip set is the ICSS1001. It interfaces to the digital chip and the host. Details on this controller may be found in the IC/SS chipset datasheet.

Interfaces to the digital chip include:

- RESET hardware reset of the chip set.
- SO, SI, and SK, used in the standard MICROWIRE™ serial interface that communicates between the controller and the digital chip. This includes data interchanged with the parallel port, and data controlling the bit rate and frequency usage of the digital chip.
- RAW DATA, received data prior to Manchester decoding.
- LRCD and LTXD receive and transmit clocks.
- PTT controls direction of the modem (receive or transmit).
- CSD0 through CSD2, select specific addresses internal to the digital ASIC on the MICROWIRE interface.
- WDT, a WATCHDOG™ timer input to the digital ASIC which results in system reset if not properly toggled by the firmware.

Host interface pins are:

- SER/PAR, strapped by the user and read by the internal firmware to control which host interface (serial or parallel) is active.
- NET/TRANS, strapped by the user and read by the internal firmware to control access to the command mode of the firmware through the serial port.
- RXRDY, TXRDY, provide handshake for an 8-bit parallel interface to the user. This port emanates from the digital chip, and data transfer is accomplished via the MICROWIRE interface. SER/PAR must be strapped to ground for this interface to be active.
- RTS/COMMAND, CTS/STATUS, RCD, and TXD, comprise a serial interface to the host with bidirectional flow control (details of the host interface appear in User Interface Details, page 5) SER/PAR must be strapped to V_{CC} for this interface to be active.

Digital ASIC

The digital chip is shown in block diagram form in *Figure 4*.

The system is driven by an external 16 MHz oscillator. The oscillator clock feeds a pair of binary rate multipliers, whose output frequencies are controlled by data written into their counters by the system controller. The output of the binary rate multiplier feeds a timer chain which generates the two designated carrier frequencies, as well as their third, fifth, and seventh harmonics. These harmonics are appropriately weighted and added to the fundamental carrier in the analog chip, producing a nearly sinusoidal carrier. In addition, several clocks are derived for data reception and decoding. For each of the two designated carrier frequencies, both an inphase and a quadrature clock are developed. Clocks for the low pass filters and for the bandpass filters are generated at frequencies determined by the bit rate requested by the controller.

Transmission is controlled by the system controller, through the PTT (push-to-talk) pin which enables output, and through the serial data pins (SO, SI, SK) which control the output of frequencies representing either of two frequencies in FSK modulation. Data provided by the host microprocessor is Manchester-encoded by the system controller.

When the IC/SS system is receiving data, the received signal enters the digital chip as a 3-bit digitized signal, plus overflow from the analog chip's ND converter. This data is run in parallel through four mixers, one for the in-phase (I) and one for the quadrature (Q) components of each of the two designated carrier frequencies. The mixers are implemented by forming an exclusive-or of the input with the inphase and quadrature clocks.

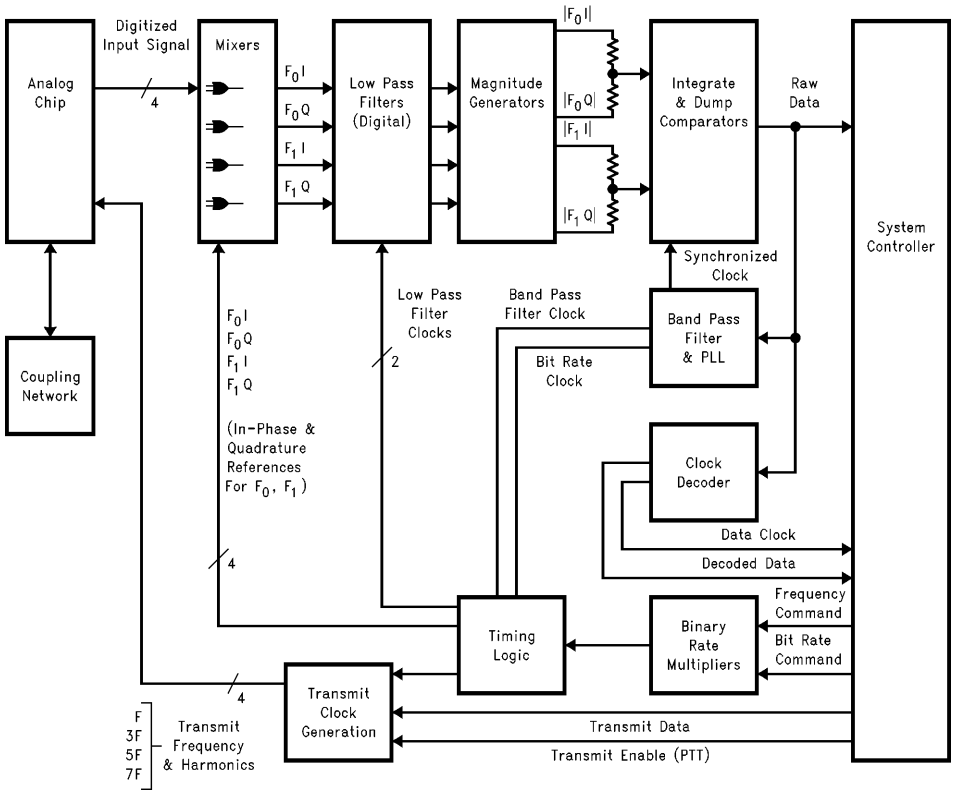

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FIGURE 4. Digital ASIC Block Diagram

The I and Q components are then run in parallel through four low-pass filters. The resulting magnitude signals are fed to a system of comparators, which compares the sum of I and Q energy on each of the two frequencies, and outputs a signal indicating which frequency has the higher energy. This last signal is a representation of Manchester-encoded data used to FSK modulate the transmitting carrier. It is manchester-decoded by the system controller and output to the host microprocessor. (Manchester-encoded data is also provided to the host microprocessor, but is not currently used.)

Bit synchronization is obtained through a bandpass filter feedback loop, which uses an initial synchronization pattern at the beginning of each packet to lock onto the f0−f1 transitions in the received signal, and synchronize the integrate and dump-function in the comparator and the manchester decoding accordingly.

Analog ASIC

Figure 5 is a block diagram of the analog chip. It shows the receive filter broadband operational amplifiers, which are connected through external resistors and capacitors. The broadband filtering is accomplished through series low pass and high pass elements. Inputs C0 through C2 switch different values of feedback resistors into the gain path, permitting gain to be set in 8 dB steps from 3 dB to 60 dB. The filtered signal is then fed to the A/D converter, which is a conventional flash converter, clocked at 1 MHz. The digital portion of the A/D converter is in the digital chip.

On the transmit side of the analog chip, the FSQWV, 3F, 5F and 7F clocks are combined in the waveshaper, which adjusts their amplitudes so that they can be added together to approximate a sinewave with the same frequency as FSQWV. This sinewave is passed through an additional filter stage, and then to an amplifier driver which interfaces to the external power amplifier stage.

User Interface Details

The user may interface to the chip set either with a four-wire serial interface or with a 15-line parallel interface.

Serial Mode

The serial interface is intended for use in applications where it is important to minimize the number of connections between IC/SS and the user. *Figure 6* shows an example host-to-IC/SS serial connection between a COP888xx family Microcontroller and the IC/SS system controller.

In serial mode, data is transferred into the chip set via TXD, and out of the chip set via RXD. Data format is byte-asynchronous, and the data rate is either 1200 bps or 300 bps. The default format is 8 data bits, no parity, one start bit and one stop bit.

RTS and CTS lines on the serial interface respectively represent control flow from the host to IC/SS and from IC/SS to the user. When RTS transitions from a low to a high, any byte currently in the process of transmission will be completed, and a maximum of one additional byte may be transmitted. When CTS transitions from a HIGH to a LOW, IC/SS will accept no more than 3 additional bytes. *Figure 7* shows a sample timing diagram.

Parallel Mode

The interconnection of the chips and the lines making up the parallel interface is shown on *Figure 19* of the IC/SS chipset data sheet. Parallel mode is enabled by connecting the SER/PAR pin on the controller to ground. Refer to *Figures 15* and *18* of the data sheet for parallel timing diagrams.

Parallel mode is intended for applications where the IC/SS chip set will reside on an 8-bit bus, with IC/SS acting like a smart UART.

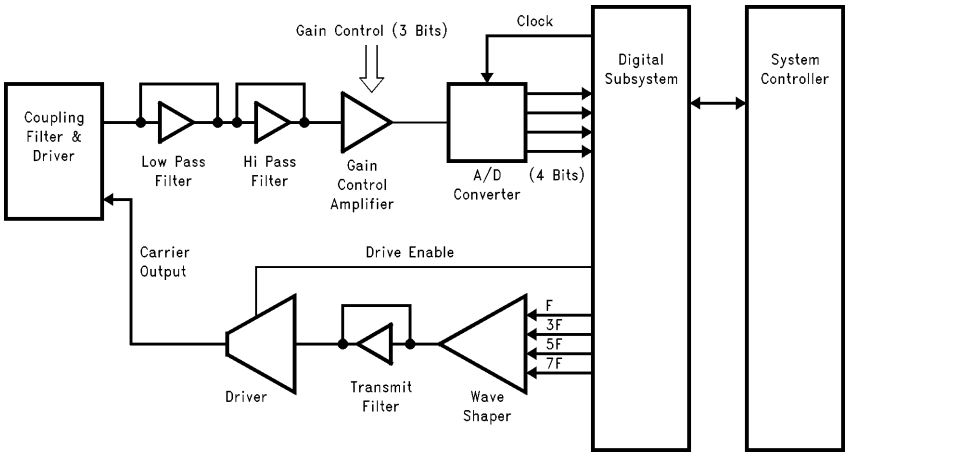

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FIGURE 5. Analog ASIC Block Diagram

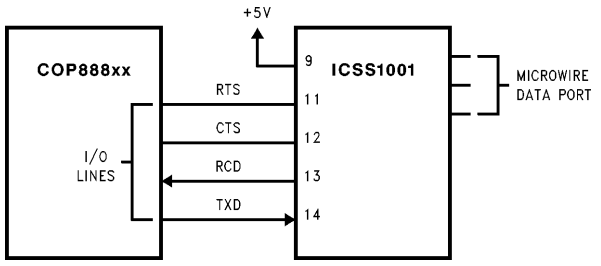


FIGURE 6. Typical Serial Connection to a COIP800

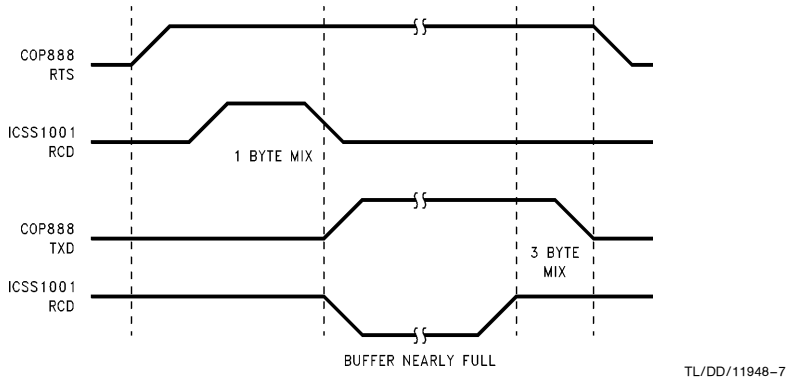


FIGURE 7. Serial Timing

The interface is enabled by setting the Chip Enable (CE on ICSS1002) at logic low, and presenting either a read or write strobe to the port.

- COMMAND is an input to IC/SS which determines if access goes to either a command register (logic HIGH) or a data byte (logic LOW).
- STATUS is an output from IC/SS, indicating whether the byte currently available for output is a status code (logic HIGH) or a data byte (logic LOW).
- RXRDY is high if a byte is available for transfer to the host.
- TXRDY is high if buffer space is available for transfer of a byte into IC/SS.

Controller Firmware Description

This section gives a more detailed description of the operation of the software portions of the system.

Network Optimization and Physical Layer Control

This section provides a brief description of the physical layer of IC/SS. This information is not necessary for use of the network, but provides information which may be helpful in understanding its performance.

The processes involved in controlling the physical layer are:

- Frequency hopping control
- Gain optimization
- Bit rate optimization
- Frequency optimization
- Synchronization and network acquisition
- Error coding and time diversity

Together, these processes comprise a feedback control system which selects a portion of the available communications spectrum so as to optimize system range, subject to the constraint of data reliability. As a secondary criterion, data rate will be maximized in those cases where doing so does not compromise range. The gain on each frequency is controlled individually to keep ambient noise below a threshold; this gain loop is inside the frequency change loop.

Frequency Hopping Control

This section describes the spectrum allocation, the coding of information bits, and the processing required for system management.

Consistent with the proposed CENELEC standard, IC/SS operates within the band of 9 kHz−95 kHz.

Frequencies must be spaced so that the principal harmonics of one do not lie close to another, otherwise distortion in the transmitted waveform of one carrier could cause interference with another frequency channel. Also, to keep the timing logic simple, it is desirable that all frequencies be generated from a common high-speed clock just by using different divisors.

Definition of Tunes

Each bit is encoded as a combination of two frequencies, together comprising a Manchester-encoded bit of information.

To take full advantage of the available spectrum without making two adjacent channels vulnerable to the same single frequency noise source, the channels should be contiguous but nonoverlapping. This leads to the following frequency allocation:

Tune	f0 (Hz)	f1 (Hz)
1	76190	61905
2	66667	52381
3	42857	23810
4	33333	14286

Tune Control

The microprocessor downloads a code into the IC/SS for each of the two frequencies of the current tune. This code is the actual divisor used in the frequency generation circuit.

Automatic Gain Control

Receiver gain is adjustable, based on signal strength and ambient noise. A separate gain value is maintained for each frequency in use. This section describes the process.

In the Master, the gain adjustment loop is fast compared to the frequency change loop; that is, changes to gain are made much more often than changes to frequency. This avoids thrashing between the gain control and frequency selection loops. Upon reset and prior to network acquisition, the gain is set at its middle value. It is then adjusted based on the number of byte errors, as determined by the parity bit. A change is made to the gain after each four packets received. Since a gain setting either too high or too low will produce inferior performance, the following peak-finding algorithm is used:

- Measure error rate at current gain value.
- Change gain and measure error rate.
  - — If error rate is better, change gain again in same direction;
  - — If error rate is worse, return to previous setting (peak found).
- When a peak is found, stay at same setting for 16 packets, then repeat the process.

Bit Rate Optimization

The Slave controls its gain autonomously, but changes its bit rate and frequency only in response to a command from the Master, or during network acquisition. Network acquisition occurs when the Slave has just been powered on, or if it loses communications. The following discussion applies only to the Master.

The Master starts at the highest bit rate. A figure-of-merit for network performance is maintained, and is updated each time a packet is received. The figure-of-merit, called BRCNT, is an 8-bit number. It is incremented if a retry of the packet is required, and is divided by two if the packet is received correctly.

If BRCNT exceeds an upper threshold, then the bit rate is decreased, unless the lowest bit rate is already in use, in which case the frequency is changed.

If BRCNT drops below a lower threshold, then the bit rate is increased, unless, of course, it is already at its maximum.

Frequency Optimization (Tune Selection)

The Master starts the network at the highest frequency channel not occupied by another master address. It will drop to another frequency channel if the system is currently not operating on the highest bit rate, and a figure-of-merit, called FHCNT, exceeds a threshold. FHCNT is calculated in the same manner as BRCNT, as a function of packet retries (see above). The Master will rotate through available frequency channels. If a collision of existing networks with other Master addresses is detected, it will be treated in the same way as unacceptable FHCNT, and will cause the Master to shift to another frequency channel.

Bit Rate and Tune Change Communication to Slaves

The current bit rate and frequency are designated in each packet. When a change is requested by the Master, it transmits four packets with the new code on the old bit rate and frequency, and then changes to the new set. Those Slaves hearing the packets change immediately; those that do not lose the network, and enter the network acquisition routine.

IC/SS NETWORK SYSTEM DESIGN ISSUES

This section addresses the key systems level questions which you must consider in designing an IC/SS network.

IC/SS as a Local Area Network

IC/SS is designed to function as a local area network (LAN), using a low voltage power distribution system as its physical distribution medium. Logically separate IC/SS networks will normally exist on different low voltage distribution networks, each feeding a separate node on a wide area network. This wide area network will typically operate at a higher speed, and may use several different types of media, such as radio and telephone.

The IC/SS network is designed to be compliant with the ISO-OSI Reference model.

The IC/SS functions provide network layer services for Host Computers to which they are connected. They assume the existence of one or more applications (in the attached Host Computers) that utilize these services.

The Network services (autopoll, broadcast, continuous link) provide a simple means to move information from point to point around the network. They support a higher level application.

For example, a host computer would contain a meter reading application. This application might use the IC/SS broadcast to tell the meters attached to Slave IC/SS modems to prepare data for future polling, then use autopoll to gather that data from the meters, and finally use continuous link to further interrogate a few of the meters, based on the data they sent back via autopoll.

IC/SS normally has no knowledge of the data being transported, only that it must guarantee that it gets from point to point correctly.

NETWORK MANAGEMENT/DESIGN ISSUES

Master/Slave Hierarchical Network

The simplest network management situation exists when each low voltage network with its IC/SS LAN is isolated from all others by the step-down transformers that connect them to the intermediate voltage distribution system. In this case the network topology linking meters and other devices attached to a particular IC/SS Master does not change in normal operation.

In the simplest case, where network topology doesn't change, the primary concerns are throughput, access time, and response time. To design a network you should proceed as follows:

- Catalog your intended traffic in terms of:
  - — Arrival rates at Masters
  - — Arrival rates at each class of Slave
- Calculate the performance of IC/SS relative to your requirements for access and response time.
- Calculate the loads your design will place on the wide area network.
- Select a wide area network technology that can meet your requirements.
- Or, redefine your system performance goals to meet the capabilities of your preferred wide area network technology.

This situation is typical in North America, and in some parts of Europe.

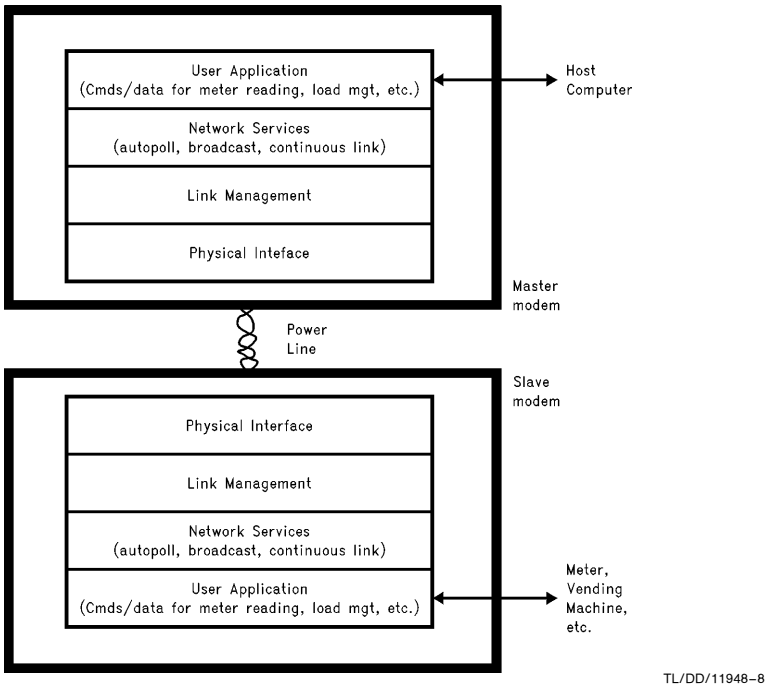


FIGURE 8. Network Operation Layer Model

Grid-Based/Time Varying Systems

In other localities, however, redundant or grid-based distribution networks may be used. In such cases a given Slave may be physically connected to different transformers at different times, and therefore to different IC/SS Masters and different ports on the wide area network. In these systems changes can occur frequently and network management becomes a more complex task.

In the case of grid-based and time-varying systems, another layer of network controls is required. This must be implemented at the host (Application) level outside the IC/SS chip set, and involves the use of various techniques for address space expansion, and for reconfiguration when the topology of the system changes.

As it is possible to dynamically change a Master to a Slave, a Slave to a Master, to have up to 4 Masters on a network simultaneously, and to utilize the reserved FF and 0 addresses, it is possible to implement a number of different network topologies, including redundant masters and peer to peer (either contention based or token passing) on IC/SS. A couple of examples follow.

Creation of a Contention Channel for Low Duty-Cycle Operation in Large Address Spaces

In traffic situations where many Slaves are on the line but have very infrequent messages to transmit, you can reduce access time, as compared to the straight polling implementation, by making use of a slotted contention channel using the mechanism described below:

Reserve Slave address FF for a contention channel which will be accessed periodically by the master through an Autopoll command to address FF alone.

When a Slave's host has no message to transmit, it must initialize that Slave to Address 00. This has the effect of causing it not to respond to any address issued from the Master. (Address 00 is used for the Master as an indicator of broadcast mode, but Slaves are blocked internally from responding on the network to this address, although they will pass data received from the network through to their hosts, and will remain synchronized to the network.)

When the Slave's host has something to send to the Master, it must switch its Slave to address FF, through a RESET command, and then transmit the desired data string to the Slave's buffer. The next time the Master polls address FF, this information will be transferred to the Master. It is necessary that the host implement a packet structure including an application-layer address for the Slave's host which is unique within the network, so the Master knows the source of the message.

The Master's host should, upon receipt of the beginning of the message from the Slave's host, respond by establishing a continuous link to Slave FF with an appropriate acknowledgment in its data stream. This will indicate that a valid host-to-host link has been established.

In the event that two or more Slaves have been set to address FF since the preceding FF autopoll cycle, both will respond, and the Master will receive a valid message from neither. It will retry four times, and then autopoll again.

If the Slave's host does not receive an application-layer acknowledgment from the Master's host within an appropriate interval, it should switch its Slave back to address 00 for a randomly determined period. At the conclusion of this period, it should switch the address back to FF and repeat the process. This random back-off procedure is similar to that used to handle collisions in Ethernet LAN systems.

The contention channel technique uses the IC/SS command set, but requires additional network-layer code in the Master and Slave hosts in order to be implemented. It is one of a number of extensions to the IC/SS protocol which were incorporated into the architecture, but not implemented in the chip set because of memory size constraints.

Because of IC/SS's Master-Slave architecture, and because channel continuity may not exist between different Slaves, improving throughput by adding carrier-sense or collision detection is generally not practical except in special cases limited to a single phase of the power distribution system. Because carrier-sense multiple access cannot be effectively implemented on a power line, a packet cannot be aborted in progress. Therefore this autopolling contention channel system behaves, with respect to capacity and access time, like a so-called ''slotted Aloha'' system.

Such a system has a maximum capacity of $1/e$ (about 0.368) times the nominal channel capacity, which in this case is the IC/SS full-duplex continuous link capacity (e = the base of the Natural System of logarithms 2.71828).

Thus, the maximum capacity, as a function of bit rate, is:

Raw Data Rate	Maximum Capacity
3200	317
1212	120
800	79
400	39

Although this is low compared to the rates in polling mode, it can be attractive in situations where there are a very large number of Slaves with infrequent messages to transmit. For example, at the $1/e$ capacity limit, and at the worst case network speed of 400 bps, 513 electric meters could each generate a 50 character reading every hour, and at 3200 bps, 4131 electric meters could do so. In this mode of operation, the internal IC/SS address space of 254 poses no limitation, since addressing would be maintained at the host level.

Contention Channel with Cyclic Data Collection

A refinement on the contention channel approach can improve performance significantly, in systems where information is to be collected from the Slaves on a cyclic rather than random basis. In this approach, the Master broadcasts the application-layer address of a Slave's host when its response is received, and then returns to autopolling FF.

Each Slave's host listens to the broadcasts, and keeps its Slave at address 00 until it hears the broadcast of an application level address which is one less than its own. It then sets its Slave address to FF. This avoids the $1/e$ inefficiency, but lengthens each unit's average network access time to one-half the time it takes to cycle through all units.

If this longer access time is acceptable, this approach increases the number of units accessed for a 50-character message in the example above to 1394 per hour at the lowest bit rate and 11228 per hour at the highest bit rate.

TECHNIQUES FOR ADDRESS SPACE EXPANSION

The IC/SS maximum of 254 Slave addresses poses an unacceptable limit in some applications. The techniques described in the previous section remove this limitation, but do so at the cost of some host-level code complexity. Several techniques for expanding the Slave address space which allow the network-layer functions to remain almost entirely within IC/SS are described in this section.

Time-Multiplexing Master Addresses

Simply by rotating through the four allowed Master addresses, the address space can be extended by a factor of four to 1016. The Master's host should perform an autopoll cycle at Master address 0, then reinitialize the Master to address 01, and so on. Slaves addresses should include the Master address as their most significant portion.

Application Address Binding and Virtual Addressing

In many systems, each Slave unit will have a unique identifier, such as a meter serial number, programmed into that Slave's host. This unique identifier would be many bytes long and would serve as the Slave unit's address at the application level. By using the random-access address FF technique described in page 9, it is possible for the Master's host to interrogate each Slave on the network, get its application identifier and assign it an 8-bit IC/SS address. The Master's host would keep a table of these assignments, allowing it to accept wide area network messages containing only the application-layer addresses and map them to the corresponding 8-bit local address.

In cases where the allowable number of Slaves on each LAN must exceed 254, but where the number active at any one time can be 254 or less, the above assignments can be made dynamically. When the address table fills, the least recently used active Slave would be sent a deactivation message to open up a slot.

Frequency-Division Multiplexing

It is also possible to frequency-division multiplex four concurrent networks by freezing each on a different frequency band through the set tune command, or two concurrent networks by limiting each to a pair of tunes by the appropriate arguments in set tune. This trades some degradation in noise immunity for a corresponding increase in aggregate data throughput.

Reassignment of Master Function

As another extension of network layer code within the host, a procedure can be implemented whereby the Master's host may solicit requests for reassignment of Mastership to Slaves, followed by a polling cycle. When a request is received, a Mastership reassignment message is sent to the requesting Slave using the continuous link mode. The Master's host then turns him into a Slave, and the Slave's host turns him into a Master.

It is important to remember that the lack of physical continuity in a power line network usually precludes all units being able to communicate directly with all others, and indiscriminate reassignment of Mastership could cause significant outages as a result. On well defined networks with guaranteed good continuity, however, this feature might be of significant value.

COMMAND DETAILS

Details of the syntax for commands sent from hosts to IC/SS Masters and Slaves, along with their responses, are presented in this section. The notation used in this section is as follows:

- <<aaa>> represents an 8-bit byte.
- <<CHAR>> where CHAR is the name of an ASCII character, represents an 8-bit byte containing that character's ACSII code.
- <<XX>> where each X is either a digit from 0 to 9 or a letter from A to F, represents a byte containing the 8-bit unsigned binary value, whose Hex representation is XX.
- [CMD] is the marker for the beginning of a command or response. In serial mode it represents an <<ESC>>, in parallel mode it represents assertion of one of the active-low signals COMMAND or STATUS.

<<data>> . . . <<data>> represents a stream of user data of arbitrary length. The user data stream is terminated when a [CMD] marker is received. In serial mode, an <<ESC>> in the user data must be coded as <<ESC>><<ESC>>. In parallel mode <<ESC>> characters are passed transparently as data.

Note: If the NET/TRANS pin on the controller is LOW (evaluation board dip switch ON), then <<ESC>> characters are passed transparently as data in either mode and no commands are recognized.

Network Commands

The following commands control the flow of data within the network.

Autopoll

Use:	Master only
Syntax:	[CMD] <<ctrl-C>> <<argument 1>> <<argument 2>>
Argument 1	lower limit of the Slave address space
Argument 2	upper limit of the Slave address space
Response	if link was acquired: [CMD] <<SO>> <<address of Slave>> <<data>> . . . <<data>>
Response	if link was not acquired: [CMD] <<SI>> <<address of Slave>>
Response	if link previously established was lost: [CMD] <<SI>> <<address of Slave>>

Function: Using address specified, modem attempts to establish a continuous link to the Slave. If link is established [CMD] <<SO>> are transmitted to the host followed by any data received from the Slave. When the Master receives a packet from the Slave with no data, the Master will assume that the Slave has transmitted all of its data. This will prompt the Master to break the link and send [CMD] <<S1>> to its host and increment the Slave address and repeat the described sequence for the next Slave. When the Slave address range is exhausted, the Master will wrap around the Slave address space and proceed with a new cycle of autopoll.

Broadcast

Use: Master only

Syntax: [CMD]<<ctrl-A>>

Response: [CMD]<<ACK>><<00>>

Function: Enter Broadcast mode of operation at the Master. Master will remain in broadcast mode until new command is issued by the host. In this mode, data received from the host will be transferred to all Slaves simultaneously. Each packet is sent eight times, but unlike polling and Continuous Link modes, each packet is not acknowledged, so delivery is not guaranteed.

Continuous Link

Use: Master only

Syntax: [CMD] <<ctrl-D>><<argument 1>>

Argument 1 Slave address

Response: if link was acquired:

[CMD] <<ACK>> <<address of Slave>>

<<data>> . . . <<data>>

if link was not acquired:

[CMD] <<NAK>> <<address of Slave>>

if link previously established was lost:

<<data>> . . . <<data>>[CMD]

<<NAK>> <<address of Slave>>

Function: Establishes continuous point-to-point link to a Slave.

Network Test Functions

The following commands provide information about the operation of the network.

Network Test Mode—Binary

Use: Master only

Syntax: [CMD] <<ctrl-B>> <<argument 1>>

<<argument 2>>

Argument 1 lower limit of the Slave address space

Argument 2 upper limit of the Slave address space

Response: [CMD] <<ACK>>

Function: Master sends a packet to each Slave in the specified address range, filled with continuously incrementing binary data. Each Slave, when it receives a packet with its address, does a software loop-back and sends the data back to the Master. The Master uses these exchanges to accumulate data on link performance.

Get Test Results

Use: Master only

Syntax: [CMD] <<ctrl-F>>

Response: [CMD] <<ACK>> followed later by:

[CMD] <<DLE>> <<byte 1>>

<<byte 2>> . . . <<byte 11>>

The following describes the contents of the byte entries. Fields are numbered from left to right.

Byte Description

1. Number of test cycles completed
2. Number of Slaves that responded
3. MSByte of the number of byte parity errors
4. LSByte of the number of byte parity errors
5. Number of post-corrected bytes in error
6. Lowest address of a Slave that responded
7. Highest address of a Slave that responded
8. Number of retries
9. Number of packet timeouts (no response to a packet)
10. Number of packet synchronization errors (first byte of packet incorrect)
11. Current tune code

The very first response from the modem after ctrl-B is the command acknowledgment indicating to the host that the command has been processed and that the modem is ready to accept new commands. The [CMD] <<DLE>> sequence follows subsequently after data has been collected.

Test Mode (ASCII)

Use: Master only

Syntax: [CMD] <<ctrl-K>> <<argument 1>>

<<argument 2>>

Argument 1 lower limit of the Slave address space

Argument 2 upper limit of the Slave address space

Response: [CMD] <<ACK>> followed later by:

[CMD] <<DLE>> <<CR>> <<LF>> <<space>>

<<high nibble of byte 1>>

<<low nibble of byte 1>>

<<high nibble of byte 2>> . . .

<<low nibble of byte 11>>

The byte numbers are the same as in the Get Test Results command above. Data is in ASCII Hex format. That means there are two ASCII characters, each either 0 through 9 or A through F for each byte. Together the pair of characters are the Hex representation of that byte.

Note: This output format is supported only in Serial mode. In parallel I/O mode ctrl-K output is identical to ctrl-B.

Function: Same as for Network Test Mode (binary) except that data is returned in ASCII format so it can be read conveniently on a terminal.

Test Mode Report Interpretation

Number of Test Cycles Completed (byte 1)

Byte 1 represents the number of test cycles that were completed. Each test cycle consists of an attempt to communicate a packet of information to some number of Slave modems. The number of Slaves that the Master will try to communicate with is identified by the address range given when the test mode command was issued. Each attempt to communicate to a single Slave consists of an initial message and up to 3 retries (total of 4 tries).

Example: Test mode command = <1B> <0B> <01> <02> (ASCII hex data) Slave 1 is connected and working, Slave 2 is disconnected. One test cycle will consist of the following message traffic on the power line:

MASTER SLAVE 1 SLAVE 2

data packet to Slave 1 →

← Echo data packet

data packet to Slave 2 →

[time-out]

data packet to Slave 2 →

[time-out]

data packet to Slave 2 →

[time-out]

data packet to Slave 2 →

[time-out]

{end of one test cycle}

data packet to Slave 1 →

← Echo data packet

etc.

Example: Test mode command = <1B> <0B> <01> <02> (ASCII hex data) Slave 1 and Slave 2 are connected and working, but the power line is very noisy. One test cycle will consist of the following message traffic on the power line:

MASTER SLAVE 1 SLAVE 2

data packet to Slave 1 →

← Echo data packet

data packet to Slave 2 →

[time-out]

data packet to Slave 2 →

← Echo data packet

Byte 2 represents the number of slaves that, within the 4 tries, correctly answered a test message from the Master. This number is accumulated over all test cycles done between test mode reports.

For example, if test mode were being performed on 10 Slaves and all responded correctly for 16 (10 hex) test cycles, then byte 2 would equal 160 (A0 hex).

Another example—if test mode were being performed on 10 Slaves, and only 5 responded correctly all the time, and the other 5 responded correctly half the time over the course of 16 (10 hex) test cycles, then byte 2 would equal 120 (78 hex). {byte 2 = (5 slaves * 16 test cycles) + (5 slaves * 16 test cycles * 0.5 response rate)}

Retries do not factor into this, the only thing that is counted is the correct communication of a Test Mode packet to a Slave.

Number of Byte Parity Errors (bytes 3 and 4)

Bytes 3 and 4 represent a 16-bit number that is the total number of byte parity errors seen in all messages generated to all Slaves over all test cycles. This number is accumulated over all test cycles done between test mode reports. Byte 3 is the most significant byte, byte 4 is the least significant byte.

For example, if you see a Test Mode report with an 02 in byte 3 and a 4E in byte 4, that would represent a total of 24E hex (590 decimal) bytes with parity errors that were seen by the Master modem over the course of the number of test cycles contained in byte 1 of the Test Mode report.

Every byte of every message sent over the power line by the IC/SS chip set has a parity bit. Each test mode message is 15 bytes long, and the probability is great that in a failed message, more than one of the bytes will have a parity error.

One of the reasons you will see so many good messages in spite of (on some power lines) a high number of bytes with parity errors is that the IC/SS chip set has a packet overlay mechanism that allow it to reconstruct a good message out of multiple bad messages (containing bytes with parity errors).

Number of Post-Corrected Bytes in Error (byte 5)

Byte 5 represents the total number of incorrect bytes seen in all messages generated to all Slaves over all test cycles. This number is accumulated over all test cycles done between test mode reports.

The determination of ''correct'' or ''incorrect'' after the IC/SS modem's packet correction algorithm is made by the Test Mode Application embedded in the Master modem. It knows what bytes it sent out to a given slave, and therefore it knows what it expects to see echoed back. If a packet contains an unexpected byte, then this is deemed incorrect, and the occurrence results in byte 5 being incremented.

''Post-Corrected'' refers to the fact that the IC/SS chip set has a packet overlay mechanism that allows it to reconstruct a good message out of multiple bad messages (containing bytes with parity errors). If the message contains an erroneous (unexpected) byte after this correction mechanism has been applied to generate a message (including data) that passes the CRC-24 check, then this is a ''Post-Corrected'' error.

This ''Post-Corrected'' error is otherwise known as a Residual Error. It represents a breakdown in an error detection algorithm, as it represents an error that is undetected by the communications system's network, link and physical layers. The choice of error detection technique combined with the bit error rate on the communications system will determine your probability of a residual error. When the bit error rate is high enough, changing enough bits in a packet, the error checking scheme can be fooled. This is possible with every commonly used error checking scheme. The IC/SS modem software (Rev B) uses a CRC-24 to error check the entire message, and parity on every byte.

The requirements for allowable Residual error rate are shown by the graph in *Figure 8* of Telecontrol Systems Integrity Classes according to IEC (IEC 870-5-1). Class 12 is applicable to IC/SS (115 VAC–240 VAC = Low voltage Network). As you can see, the Residual Error probability of IC/SS is well within spec.

Please note that other error detection algorithms (CRC-16, LRC, various XOR/rotate schemes) used with power line carrier systems do NOT meet these requirements.

Lowest and Highest Address of a Slave that responded (bytes 6 and 7)

Byte 6 represents the lowest Address of a Slave that responded to any message in any test cycle since the last Test Mode report. Byte 7 represents the highest Address of a Slave that responded to any message in any test cycle since the last Test Mode report.

Example—if test mode were being performed on 10 Slaves (addresses 5 through 14), and only 5 responded correctly all the time (addresses 5, 6, 7, 12, 13), and the other 5 (addresses 8, 9, 10, 11, 14) never responded at all, then byte 6 would equal 5 and byte 7 would equal 13.

Variation—if, in the above example, modem 5 went off line, then byte 6 would now equal 6 and byte 7 would continue to equal 13.

Total Number of Retries (byte 8)

Byte 8 represents the total number of retries done in the process of trying to communicate to all specified Slaves over all the test cycles done since the last Test Mode Report. This is the sum of the retries from three different causes.

A retry can be caused by no response to a message (time-out) from the Master to a Slave. A retry can be caused by a NAK from a Slave to a message from the Master. A retry can also be caused by the receipt of a message from a Slave that contains errors that cause it to fail the CRC-24 check (''packet error code errors''). All of these will cause byte 8 to be incremented.

Number of Packet Time-outs (byte 9)

Byte 9 represents the number of retries due to time-outs done in the process of trying to communicate to all specified Slaves over all the test cycles done since the last Test Mode Report.

When the Master sends a message to a Slave, it starts an internal timer. If this timer expires before a response (either a NAK, or a correct or mostly correct message) is received from the Slave, then this generates a re-transmission of the original message (up to 4 times). This time-out event also causes the count in bytes 9 and 8 to be increased.

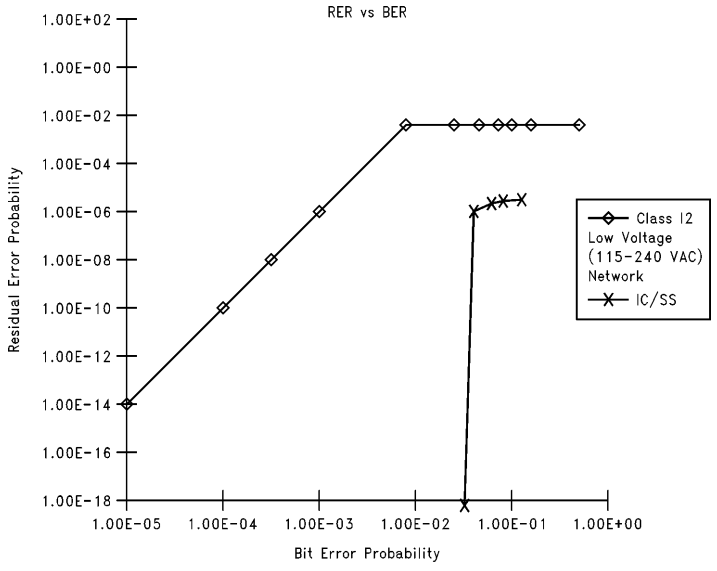
Number of Packet Synchronization Errors (byte 10)

Byte 10 represents the total number of times that the Master tried unsuccessfully to find the first three bytes of a response from the Slave in the process of trying to communicate to all specified Slaves over all the test cycles done since the last Test Mode Report. This is not the same as a time-out, as it indicates that the Master is seeing what looks like a response on the power line, but it cannot get in synch with it.

This is useful in determining if there is a problem on the power line that is causing deformation or jamming of one or more tune codes (frequency pairs) used by IC/SS. It tells you how successful the modem is in identifying that there is a message on the power line.

Number of Packet Synchronization Errors (byte 11)

Byte 11 represents the tune code in use when the Test Mode Report was generated.



TL/DD/11948–9

FIGURE 9. Bit Error/Residual Error Graph

Examples of Test Mode Report Interpretation

Example 1: Report = E0 D4 00 EC 00 01 01 80 67 0D 01

In this case, there were 224 test cycles (byte 1) and 212 (byte 2) were answered by the addressed slave within the 4 retries, so there were 12 test cycles (representing 48 messages and 12 packets) in which there was no response.

Bytes 3 and 4 indicate that there were 236 bytes that came through with parity errors. Each test mode message is 15 bytes long, and the probability is great that in a failed message, more than one of the bytes will have a parity error.

Byte 5 indicates that there were no residual (post corrected) errors.

Bytes 6 and 7 indicate that only one Slave was active and responding—address 1. Therefore it is the highest and lowest Slave address.

Bytes 8, 9 and 10 indicate there were a total of 128 messages that had to be retried. Of this 128, 103 were time-outs (likely due to no discernible response), 13 were packet synchronization errors that resulted in a retry (said retry would be after a time-out, and this time-out would be part of the 103), and the remaining 25 were likely due to a check sum failure (due to parity errors on bytes in the message).

As 48 of them are accounted for, the remaining 80 were re tries on the 212 ''good'' messages that ultimately did get through.

This set of test results was taken on a noisy line, resuiting in many bytes with parity errors. It also is likely that it was taken when the test mode first started, and the bit rate and possibly the tune code were being adjusted (by the Master modem) to work to improve the Bit Error Rate it is measuring on the line.

Example 2: Report = 38 38 00 00 00 01 01 E0 E0 00 01

In this case, there were 56 test cycles (byte 1) and 56 (byte 2) were answered by the addressed slave within the 4 retries, so for all test cycles there was at least one response from a Slave.

Bytes 3 and 4 indicate that there were no bytes that came through with parity errors.

Byte 5 indicates that there were no residual (post corrected) errors.

Bytes 6 and 7 indicate that only one Slave was active and responding—address 1. Therefore, it is the highest and lowest Slave address. There may be other Slaves on this network, but they are not responding.

Bytes 8, 9 and 10 indicate there were a total of 224 messages that had to be retried. Of this 224, all were time-outs (likely due to no discernible response). This indicates that there is likely another Slave being tested and not responding.

This set of test results was taken on a good line with one Slave responding and the other disconnected.

Chip and Physical Link Management Commands

The following commands control initialization and setup, and allow the application program to take over control of the physical layer, rather than allowing the chip set to control it.

Flush Command Buffer/Software Revision Level

Use: Master and Slave

Syntax: [CMD] <<ctrl-M>>

Response: [CMD] <<ACK>> <<byte 1>>
<<byte 2>>
byte 1 = major revision level
byte 2 = minor revision level

Function: Flushes Command Buffer and returns Master to default autopoll state (autopoll address 01). This is useful if the host software has somehow lost synchronization with the modem, or forgotten what it last sent.

This command also causes the revision level of the IC/SS firmware to be output.

Chip Reset

Use: Master and Slave

Syntax: [CMD] <<ctrl-G>> <<argument 1>>
<<argument 2>>

Argument 1: bit 0 (lsb) = lsb of address of Master for Slave
bit 1 = msb of address of Master for Slave
bit 4 = 0 if Slave, 1 if Master
bit 5 = 0 if network acquisition will be performed; 1 if it will not.

Argument 2: unit address. Allowed addresses are 1 through 254. If argument 2 is 0, then the previous address is kept.

Response: [CMD] <<ACK>>

Function: Performs soft reset of the modem, allowing change of identity and addresses.

Chip Status Request

Use: Master and Slave

Syntax: [CMD] <<ctrl-H>>

Response: [CMD] <<ACK>> << byte 1>>
<< byte 2>>
byte 1 = retry count for Master:
byte 2 = currently addressed Slave for Slave:
byte 2 = Master filter

Function: Returns status information on current chip address settings and link performance.

Set Tune

Use: Master and Slave

Syntax: [CMD] <<ctrl-E>> <<argument 1>>

Argument 1: tune code (binary number)

Valid values for lower nibble of Argument 1 are:

HEX	Function
1	Select tune 1
2	Select tune 2
3	Select tune3
4	Select tune 4
F	Re-enabled frequency hop mechanism, current tune remains unchanged

If an illegal tune code is passed as argument, the frequency hop mechanism will be re-enabled and current tune will remain unchanged.

Valid values for upper nibble of Argument 1 are:

HEX	Function
0	Use all four tunes
1	Use tunes 1 and 2
2	Use tunes 3 and 4

The following is a table of all correct combinations of the upper and lower nibble of Argument 1.

HEX	ASCII Character (PC Keyboard)	Function		
		Modem = Master/Slave	Responds to Master Whose addreess = ?	Do Network Acquisition (Y/N)*
00	<pause>	Slave***	0	Yes
01	ctrl-A	Slave***	1	Yes
02	ctrl-B	Slave***	2	Yes
03	ctrl-C	Slave***	3	Yes
10	ctrl-P	Master	0**	Yes
11	ctrl-Q	Master	1**	Yes
12	ctrl-R	Master	2**	Yes
13	ctrl-S	Master	3**	Yes
20	<space>	Slave***	0	No
21	!	Slave***	1	No
22	‘‘	Slave***	2	No
23	#	Slave***	3	No
30	0	Master	0**	No*
31	1	Master	1**	No*
32	2	Master	2**	No*
33	3	Master	3**	No*

Notes:

*If the modem is currently a Slave and being reset to be a Master, Network Acquisition will always be performed, and the state of the bit will be ignored.

**When modem is told that it is to be a Master, the 2 least significant bits of Argument 1 become its Master address. If there is another Master on the network at this address, multiple Master contention may occur, so use caution in utilizing this command.

***When the modem is told it is a Slave, then argument 2 becomes its Slave address (0 to 254). Otherwise, this argument is necessary, but will be ignored.

An <Ack> response is given to this command to acknowledge receipt of the command only. If illegal arguments are given, the modem will return to its default settings (which are similar to the results of this command). The chief difference is that the modem, while doing reset, will read the DIP switches to decide if it is a Master or a Slave and what its address should be. It will, in all cases, go through reset which will include doing network acquisition (synchronization).

Note: Bits 2, 3, 6, 7 are reserved for future use and should be zero.

HEX	ASCII Character	Function
01	ctrl-A	Select tune 1/can use only this tune code (will stay at this tune, though all 4 are enabled)
02	ctrl-B	Select tune 2/can use only this tune code (will stay at this tune, though all 4 are enabled)
03	ctrl-C	Select tune 3/can use only this tune code (will stay at this tune, though all 4 are enabled)
04	ctrl-D	Select tune 4/can use only this tune code (will stay at this tune, though all 4 are enabled)
0F	ctrl-O	Re-enable frequency hop/can use all 4 tune codes upon frequency hop
11	ctrl-Q	Select tune 1/can use only this tune code (will stay at this tune, though only 1 and 2 are enabled)
12	ctrl-R	Select tune 2/can use only this tune code (will stay at this tune, though only 1 and 2 are enabled)
1F	no ASCII equivalent	Re-enable frequency hop/can use only tunes 1 and 2 upon frequency hop
23	#	Select tune 3/can use only this tune code (wall stay at this tune, though only 3 and 4 are enabled)
24	$	Select tune 4/can use only this tune code (will stay at this tune, though only 3 and 4 are enabled)
2F	/	Re-enable frequency hop/can use only tunes 3 and 4 upon frequency hop

If the upper nibble of the argument (bits 7–4) is not 0, 1 or 2, an <ESC> <BEL> will be returned. If the upper nibble is correct, and the lower nibble incorrect (not equal one of the values in the above table), then a normal response will be returned, and the tune code will not be changed, and frequency hop will be re-enabled as indicated by the upper nibble (0 enables all 4 tunes, 1 enables tunes 1 and 2 only, 2 enables tunes 3 and 4 only.

Response: [CMD] <<ACK>> <<byte>>

byte = current tune code (in lower nibble)

Function: Master: disables frequency hop mechanism and sets current tune to the value of the argument. Slave: Sets current tune to the value of the argument.

Set Bit Rate

Use: Master and Slave

Syntax: [CMD] <<ctrl-L>> <<argument 1>>

Argument 1 bit rate code (binary number)

Valid values for Argument 1 are:

If an illegal code is passed as argument, then the bit rate machanism will be re-enabled and the current bit rate will remain unchanged.

HEX	ASCII Character	Function
01	ctrl-A	Select 3200 bps
02	ctrl-B	Select 1212 bps
03	ctrl-C	Select 800 bps
04	ctrl-D	Select 400 bps
7F	DEL	Re-enable it rate mechanism, current bit rate will remain unchanged

Response: [CMD] <<ACK>> <<byte>>

byte = current bit rate code (lower nibble)

Function: Sets the modem bit rate as indicated. If Master and Slave are forced to different bit rates, no communication will occur. If Master is forced and Slaves are left on automatic, they will find the Master.

Direct Hardware Access/Debugger

Use: Master and Slave

Syntax: [CMD]<ctrl-J>

Argument: none

Function: Suspends modem operation and provides access through the host port to the controller's internal RAM and interfaces to the digital ASIC. On exit, restarts the modem through soft boot procedure.

Description of Operation: When the modem receives a ctrl-J, the unit will output the following to the Host:

**V1.00 Micro Menu **	
1 RAM	4 RESET LTX PIN
2 LATCHES	5 SET LTX PIN
3 TOGGLE PTT	6 WARM RESET

Enter the desired number, I through 6, followed by a carriage return.

EXAMPLE: Following are instructions if you select RAM.

1. Enter 1 followed by a carriage return. The screen will display the following:

   R/W RAM (FF TO EXIT)

   Enter Address:

2. Enter a 2 digit, hexadecimal address, followed by a carriage return. The screen will prompt:

   (R/W?)

3. Type R for read or W for write. If you request Read, the unit will respond with the address and data for a read, e.g., 06/0A

   to indicate that 0A is the contents of location 06.

If you request Write, you will be prompted to enter the desired data.

Note: Careless or incorrect setting of RAM variables and latches can cause incorrect and unpredictable behavior which can only be corrected by a hardware reset. This command should be used carefully and with full understanding of what you want to accomplish.

Registers

Access to registers is provided by entering an address whose first hex digit is F, and whose second hex digit is the register address, e.g., F1 will access register 1, bit rate.

Return to the menu by selecting address FF.

Register addresses are as follows:

Register Address	Meaning	Read/Write Values
1	Bit Rate	write 0-3
2	DIP Switches	read
3	LEDs	write
4	Parallel Port	read
5	Gain	write 0-3
6	Parallel Port	write
7	Frequency	write

OTHER HARDWARE DESIGN CONSIDERATIONS

Receiver Bandpass Filter

The receiver bandpass filter design is the responsibility of the designer cognizant of both the frequencies used. Two unity gain amplifiers are provided as part of the analog chip. The external connections of the ICSS1003 analog chip are listed in Table III of the IC/SS chipset datasheet.

Transmit Power Amplifier

The transmit power amplifier design is the responsibility of the designer cognizant of both the frequencies used and the impedance of the power line environment. This amplifier ideally provides good drive capability and allow for graceful transitions between various AC line impedances without distortion or clipping of the drive waveform.

Power Coupling Networks

The power coupling network design is the responsibility of the designer cognizant of the power line environment in which the IC/SS network is used. This passive network provides coupling to the AC power line. It should be designed for optimal transfer characteristics and minimal phase distortion of the transmitted signals when presented with a typical power line impedance between the tuning frequencies. A typical coupling network is presented in *Figure 21* of the IC/SS chip set datasheet.

For input signals from the AC line, the coupler should be designed to:

- Attenuate 50 Hz to 60 Hz by at least 100 dB.
- Provide reasonably flat frequency response across the operating range of 10 kHz to 90 kHz.
- Present a high impedance to the line in the operating frequency range.
- Be critically damped to avoid ringing in response to high energy impulse noise.

In some situations, like meter reading, where the circuit may float on the line, with no external ground connection, it is possible to eliminate the transformer and replace it with an inductor, reducing both size and cost.

If coupling to multiple phases is required, as is typical at a Master unit, then these multiple phases may be coupled in parallel to one side of the transformer.

Other design considerations include designing for different voltage levels. Line-to-line voltages are double the single phase voltage. The coupling capacitor or capacitors should be AC capacitors at least the rated line voltage. If two capacitors are used in the coupling circuit, then the working voltage may be as little as one-half the voltage.

Although a Zener diode is included in the ICSS1003 analog chip, further transient protection is recommended in the primary side of the coupling network (preferably a MOV) and in the secondary side of the coupling network (presumably a transzorb). Again, like the coupling capacitors, the MOV should be rated at least the AC voltage depending on the configuration of the connections to the power line.

PCB Design Considerations

PCB design considerations should be dealt with early in design or test of the IC/SS chip set.

Good design practice includes adequate grounding, de-coupling, and separation of PC traces to avoid crosstalk.

Grounding

In IC/SS there are two grounds, analog, and digital. It is good design practice to keep the digital grounds common to the appropriate circuitry. For good performance it may be necessary to keep the appropriate ground under the corresponding analog or digital section of the board layout.

De-Coupling

Careful power supply de-coupling is an integral part of good design practice. It is recommended to place all power filter caps as close to power connections on associated chips as possible. Buried power and ground layers aid filtering because they function as an extremely effective parallel plate capacitor.

GLOSSARY OF TERMS:

Application Layer
Layer in ISO-OSI model concerned with exchanges that have meaning and value to the user, such as utility meter reading.

ASCII
American Standard Code for Information Interchange. A widely used representation of letters, numbers, special characters and control characters in computer binary form.

ASIC
Application Specific Integrated Circuit, a custom chip.

Baud Rate

The measure of data transmission speed for communications systems. More specifically it is the number of signal pulses per second, although in common usage it is the number of bits per second.

Bit Error Rate (BER)
The fraction of received bits that are in error, usually expressed as a negative power of ten. For example, a BER of 10−6 would mean that one bit in a million would be incorrect. The bit error rate at a given signal to noise ratio is a common measure of a modulation scheme's effectiveness.

Broadcast
A communications technique where one station on a network transmits a signal for all the other stations to receive.

Byte
A group of eight bits.

c
Speed of light in a vacuum. The maximum speed for any signal, which is 299, 792, 458 m/sec.

Carrier
A single frequency signal whose characteristics are varied in a time dependent way to transmit information.

CENELEC
European communities standards setting body for electric utilities. Allocates communications frequencies to be used on electric power lines.

Class A
The FCC electromagnetic compatibility (EMC) compliance category for office and industrial equipment.

Class B
The FCC electromagnetic compatibility (EMC) compliance category for home electronics.

[**CMD**]
IC/SS command designator. In serial mode it is the ASCII Escape character, in parallel mode it represents assertion of one of the active-low signals COMMAND or STATUS.

Continuous Wave (CW)
A single frequency electromagnetic signal.

COP888xx
Trade name for a line of single chip microcontrollers produced by National Semiconductor Corporation.

Coupling Network
A passive electrical circuit that connects two other circuits with different characteristic impedances.

dB
Decibel. One tenth of a bel. Originally a measure of sound intensity.

DCE
Data Communications Equipment, one of two classes of serial devices specified in RS-232C, the other being Data Terminal Equipment (DTE). Modems are typically DCE. When a DCE is connected to a DTE, the transmit lines of one are properly connected to the receive lines of the other, and vice versa. A DCE cannot be connected directly to another DCE, nor a DTE to a DTE. Instead, a null modem must be used to connect them.

DIP Switch
Dual-in-line package switch.

Driver
The software program that controls an input/output device connected to a computer.

DTE
Data Terminal Equipment, typically a computer or terminal. See DCE.

e
A mathematical constant which is the base of the natural logarithms, approximately 2.718281828459 . . .

Electronic Countermeasures
Electronic techniques that combat the effects of jamming. Frequency hopping is an example of a spread spectrum technique for electronic countermeasures.

EMC
Electromagnetic compatibility. A requirement that electronic equipment should not radiate electromagnetic energy which could interfere with other electronic equipment, particularly radio and television receivers.

Error Correcting Code
A coding scheme for data transmission that contains enough redundant information so that certain types of errors can be both detected and corrected without retransmission.

ESC
The ASCII Escape character, ''1B'' Hex.

ESD
Electrostatic discharge. The spark that occurs when an electric charge that has built up on a person or metal object is released. A major cause of damage to electronic components, especially integrated circuits.

FCC
Federal Communications Commission. United States Government's communications regulatory body.

Firmware
Computer programs that are incorporated into a chip, in contrast to software computer programs.

Flow Control
The ability in a data communications system for a receiving device to tell a transmitting device not to send any more data until the receiver is ready.

Frequency Agility
The ability of a communications system to change its carrier-frequency often.

Frequency Hopping
A communications technique where transmission carrier-frequencies are changed regularly on a prearranged basis.

FSK
Frequency Shift Keying, a modulation technique where a ''1'' is represented by one transmitted frequency and a ''0'' by another.

Hex
Hexidecimal. A number system with a base of 16. Each digit is either 0,1,2,3,4,5,6,7,8,9,A,B,C,D,E or F.

Host
An intelligent device attached to the IC/SS controller chip. It can be another microprocessor built into an IC/SS unit such as an electric meter, or the personal computer used to drive the IC/SS evaluation boards.

Hz
Hertz. The unit of frequency, one cycle per second.

IC/SS
Integrated Circuit/Spread Spectrum. Trade name for a line of power line communications products developed by CYPLEX and sold by National Semiconductor Corporation.

IEC
International Electrotechnical Commission. An international standards setting body for electrical equipment.

Impedance
A measure of an electrical circuit's response to alternating currents which is analogous to resistance for direct currents. Consists of two values, resistance and reactance, which are often combined as a single complex number. When a single impedance number is given, it is the magnitude of the complex number.

Impulse Noise
An unwanted electrical signal of very short time duration.

ISO-OSI
International Standards Organization—Open Systems Interconnect. A general model of data communications systems that segregates functionality into seven layers: physical, link, network, transport, session, presentation and application.

Jamming
Disrupting the operation of electronic systems by generating electromagnetic energy that interferes with desired signals.

kHz
Kilohertz, 1000 Hz.

LED
Light Emitting Diode. Used as an indicator on electronics equipment.

Link Layer
Layer in ISO-OSI model concerned with reliable transmission between stations.

LSB
Least significant bit.

Manchester Coding
A particular coding method for data transmission. Its design guarantees that each bit time has a zero crossing, and enough signal transitions occur so that a clock signal can be extracted from the data stream. Commonly used in Master/Slave type systems that have command/response protocols (e.g. MIL-STD-1553B).

Master
The unique modem on an IC/SS network that can initiate communications.

MHz
Megahertz, 1000000 Hz.

MICROWIRE
A proprietary high-speed serial link developed by National Semiconductor to communicate between its COP8 micro controllers and other chips.

Modulation
Varying some characteristics of a signal in a time dependent way to transmit information.

MSB
Most significant bit.

nsec
Nanosecond, 10-9 seconds, the time light takes to travel 30 cm.

Network Layer
Layer in ISO–OSI model concerned with the switching and routing of information.

Nibble
A group of four bits; one half of a byte.

Null Modem
A device with serial data connectors at both ends that is internally wired to cross connect all transmit and receive lines. See also DCE.

Ohm
The unit of measurement for impedance.

Overlay
Combining several repeated message frames, each of which is invalid, to recover the original valid frame.

Packet
A block of information of limited length, typically consisting of a header and data section. In packet communications, a user's message is broken up into packets which are transmitted and verified separately.

Physical Layer
Layer in ISO–OSI model where devices are physically connected and raw data is transmitted.

PLC
Power line communications.

PLCC
Plastic Leaded Chip Carrier, a type of integrated circuit package.

Polling
A communications technique where a group of stations on a network are interrogated one at a time by a Master Station.

PQFP
Plastic Quad Flatpak, a type of surface mount technology (SMT) integrated circuit package, physically smaller than the PLCC package.

Protocol
The agreed-upon procedures that govern communications on a network.

Pseudo-Random Sequence
A sequence of values that appear to be randomly selected but are in fact generated by a deterministic algorithm.

PTT
Push To Talk, the internal IC/SS signal that switches from receive to transmit.

Quadrature
Two signals that have a phase difference of 90 degrees.

Ringing
A phenomenon that can occur when an energy impulse is applied to a resonant electrical circuit. An alternating current signal is produced whose strength decays gradually over time.

RS-232C
An Electronic Institute of America (EIA) standard that governs digital serial communications. It specifies signal functions, voltage levels and the pin assignments on 25-pin D-shell connectors.

Reactance
The effect of a capacitor or inductor on an alternating current of a particular frequency.

Resonance
An effect that occurs when the capacitive and inductive reactances in a circuit cancel out at some frequency, resulting in a very low or very high impedance at that frequency.

Signal to Noise Ratio
The ratio of signal strength, usually expressed as energy per bit (EbN0), to noise level in a communications channel. See also bit error rate.

Slave
One of many modems on an IC/SS network that can respond to requests from the master.

Spread Spectrum
An electronic communications technique where the signal is deliberately spread over a wide range of frequencies, rather than being confined to a narrow frequency band.

Tune
Pair of frequencies used in IC/SS to encode a bit.

UCA
Utility Communications Architecture. A utility-wide data communications technology strategy developed by EPRI (Electric Power Research Institute).

WAN
Wide area network. A data communications network designed to serve a large area.

WATCHDOG Timer
A circuit that will reset the system if not pulsed periodically by the controller. Allows the system to restore itself after a power loss or other glitches.

White Noise
Random electrical signals spread uniformly in frequency throughout the spectrum.

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National Semiconductor Corporation
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090
Tel: 1(800) 272-9959
TWX: (910) 339-9240

National Semiconductor GmbH
Livry-Gargan-Str. 10
D-82256 Fürstenfeldbruck
Germany
Tel: (81-41) 35-0
Telex: 527649
Fax: (81-41) 35-1

National Semiconductor Japan Ltd.
Sumitomo Chemical
Engineering Center
Bldg. 7F
1-7-1, Nakase, Mihama-Ku
Chiba-City,
Ciba Prefecture 261
Tel: (043) 299-2300
Fax: (043) 299-2500

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductores Do Brazil Ltda.
Rue Deputado Lacorda Franco
120-3A
Sao Paulo-SP
Brazil 05418-000
Tel: (55-11) 212-5066
Telex: 391-1131931 NSBR BR
Fax: (55-11) 212-1181

National Semiconductor (Australia) Pty, Ltd.
Building 16
Business Park Drive
Monash Business Park
Nottinghill, Melbourne
Victoria 3168 Australia
Tel: (3) 558-9999
Fax: (3) 558-9998