Interfacing the DP8441 and the i486

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Atilio Canessa
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INTRODUCTION

This application note assumes that the reader is familiar with the modes of operation of the DP8441 DRAM controller and the i486 microprocessor. The nature of this application note is to give the system designer an idea of a possible memory configuration. After reading this application note, the system designer must do an analysis for his particular application.

The design's operating frequency is 33 MHz and it supports page accesses and non-burst cacheable multiple access sequence. The design constitutes a complete 128 Megabytes memory system in a 2 bank configuration. The memory array uses 70 ns DRAMs in a 16 Meg X1 architecture.

The DP8441 will perform refreshes to the memory and it will guarantee precharge times after an access or a refresh cycles. The DP8441 also arbitrates between accesses, refresh cycles and precharge. The DRAM controller inserts wait states into either accesses or refreshes to allow one or the other to finish.

The DP8441 supports byte, word or double-word writing. This is done through connecting the $\overline{BE3-0}$ from the 486 to the $\overline{ECAS}$ inputs. $\overline{ECAS}$ control $\overline{CAS}$ assertions to the DRAMs.

RESET AND PROGRAMMING

Resetting the DRAM controller is accomplished by asserting low the $\overline{RESET}$ input for at least 16 clock cycles. After reset, the DP8441 must be programmed before accessing the memory. Programming can be done by writing to an I/O address equal to the programming selection. Programming can also be accomplished during the first memory write. In the latter case the CPU writes to an address equal to the programming selection during the first write cycle after power up. $\overline{ML}$ is asserted during the programming operation.

After $\overline{ML}$ negates during the programming cycle, the DP8441 enters a 60 ms initialization period. This period is necessary for the Phase Lock Loop (PLL) to lock into place. The system must wait at least 70 ms before accessing the memory. During this time the DRAM controller performs refreshes to the memory, these refreshes make further ''warm up'' cycles unnecessary.

OPENING ACCESS

A memory access begins when the 486 outputs a valid address and asserts $\overline{ADS}$. For this design at 33 MHz, the address, the B0 (bank select) and the $\overline{ADS}$ inputs meet the set up times required by the DRAM controller. Three address lines are used to do DRAM $\overline{CS}$. The $\overline{CS}$ set up time is also met. See timing calculations.

The DP8441 will split the address from the CPU and will output the row address to the DRAMs. The appropriate $\overline{RAS}$, as decoded by B0 and the programming selection (bits C4 and C5), assert from the rising clock edge that $\overline{ADS}$ is set up to (CLK2). $\overline{RAS}$ asserting latches the row address into the DRAM. The programmed t_{RAH} will be guaranteed by the controller before switching the internal multiplexor to the column address. The controller asserts $\overline{CAS}$ to latch the column address into the DRAM after meeting the t_{CSC} (0 ns). The t_{RAH}, t_{CSC} and the time when the controller switches the row address to the column address is guaranteed by the on-board delay line based on the PLL.

The controller asserts $\overline{DTACK}$ after the programmed number of wait states to indicate to the CPU the end of the access. In this design, during opening access, $\overline{DTACK}$ asserts from the 4th rising clock edge. Since $\overline{DTACK}$ is programmed to assert from the rising clock edge, the $\overline{DTACK}$ ($\overline{RDY}$) setup time required by the CPU is easily met.

At the end of the fourth clock the 486 will either latch the data into its registers in the case of a read cycle, or it will take the data of the bus in the case of a write cycle. For every access, $\overline{DTACK}$ asserts for one clock period. $\overline{CAS}$ negates automatically from the same clock edge that $\overline{DTACK}$ negates.

PAGE ACCESSES

The 486 will finish an access when it sees $\overline{DTACK}$ ($\overline{RDY}$) low. The DP8441 DRAM controller supports page mode, and in this application note page mode is programmed. Therefore, when $\overline{DTACK}$ negates to finish an access, only $\overline{CAS}$ negates. The $\overline{RAS}$ outputs stay asserted. When the CPU requests a new access with the output of a new address and a new $\overline{ADS}$, one of two situations may occur:

1. If the new access is within the same page as the previous access (same row address), a **page hit** is detected by the on-board page comparator. In these cases $\overline{RAS}$ stays asserted and the controller outputs the new column address and asserts $\overline{CAS}$ from the next rising clock edge.
2. In cases when there is a new row address, a **page miss** is detected, and the DP8441 negates $\overline{RAS}$. Then, the controller will meet the programmed number of clock edges for precharge before asserting $\overline{RAS}$ to latch the new row address into memory.

In either case $\overline{DTACK}$ will assert after the appropriate number of programmed wait states. With a page hit $\overline{DTACK}$ asserts according to programming bits R6 and R7, $\overline{DTACK}$ during Page Mode. If there is a page miss, the access is delayed and $\overline{DTACK}$ asserts according to bits R2 and R3, $\overline{DTACK}$ during opening access.

NON-BURST CACHEABLE MULTIPLE ACCESS SEQUENCE

The 486 indicates that it wants to burst when $\overline{BLAST}$ does not assert during the last clock of the cycle. The CPU also expects the controller to finish a burst access with $\overline{BRDY}$ instead of $\overline{RDY}$. Since the DRAM controller cannot burst the 486 sequence, it will finish every access asserting the $\overline{RDY}$ input instead of the $\overline{BRDY}$ input. This action forces the 486 to provide the new address, and a new $\overline{ADS}$, for the next location to cache. Since a Cacheable Multiple Cycle Sequence happens within the same page, a page hit will be detected for every access. During this sequence, the DRAM controller will automatically assert $\overline{CAS}$ to latch the new column address into memory. The DP8441 finish every access with the assertion and negation of $\overline{DTACK}$ according to page mode programming.

REFRESH AND PRECHARGE

The DP8441 will request a memory refresh every 15 μs. During refresh, $\overline{RAS}$ will be low for 3 clock periods. The controller will also guarantee precharge of 3 clock periods.

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These timings are enough for 70 ns DRAMs. If the controller is in the middle of a page mode access ($\overline{RAS}$ asserted but no real access may be in progress) the controller will keep track of all refresh requests. When there is an access out of page, the DRAM controller will burst refresh the memory the number of refresh requests missed. If the in-page access is idle, and a sixth refresh request happens, the DRAM controller will automatically finish the access, meet the precharge time, and burst refresh the memory six times.

PROGRAMMING BITS

TABLE I

R1, R0 0, 1	$\overline{RAS}$ Low and Precharge Time 3Ts
R3, R2 0, 1	$\overline{DTACK}$ during Opening Access will Assert after $\overline{RAS}$ 2Ts
R5, R4 0, 1	Don't Care
R7, R6 0, 1	$\overline{DTACK}$ during Page Access will Assert after $\overline{CAS}$ 1T
R8, R9 1, 1	Page Size Select to 4096 for 16 Meg DRAMs
R11, R10 X, X	Don't Care
C3, C2, C1, C0 0, 1, 0, 0	Divisor Select for DELCLK to get Close to 2 MHz. 15. (33/16 = 2)
C5, C4 1, 1	B0 is not used. Staggered Refresh B1 = 0 ⟶ $\overline{RAS}$ 0,1 $\overline{CAS}$ 0,1,4,5 B1 = 1 ⟶ $\overline{RAS}$ 2,3 $\overline{CAS}$ 2,3,6,7
C6 0	Staggered Refresh Selected
C7 0	t_{RAH} = 10 ns
C8 1	Page Miss Output Selected
C9 X	Don't Care
C10 0	$\overline{RAS}$ Only Refresh Selected
C11 0	15 μs Refresh Period
B0 X	Don't Care
B1 0	Page Mode Selected
$\overline{ECAS0}$ X	Don't Care
$\overline{ECAS1}$ X	Don't Care
$\overline{ECAS2}$ 0	$\overline{CAS}$ and $\overline{DTACK}$ Clock Edge Select is the Rising Clock Edge

TIMINGS FOR THE i486 AND THE DP8440/41 INTERFACE DRAM CONTROLLER RUNNING AT 33 MHz

1. Minimum $\overline{ADS}$ Low Set Up Time to CLK High.
   1 CLK Period—CLK High to $\overline{ADS}$ Asserted (i486)
   30.3 ns − 19 ns
   11.3 ns The DP8440/41 need only 6 ns
2. Minimum Address Valid Set Up Time to CLK High.
   1 CLK Period—CLK High to Address Valid (i486)
   30.3 ns − 19 ns
   11.3 ns The DP8440/41 need only 10 ns
3. Minimum $\overline{CS}$ Asserted Set Up Time to CLK High.
   1 CLK Period—(CLK High to Address Valid + Decode Delay)
   30.3 ns − (19 ns + 8 ns)
   30.3 ns − 27 ns
   3.3 ns The DP8440/41 need only 4 ns
4. Wait States Through $\overline{RDY}$ during Opening Accesses.
   4a. Access Time from $\overline{RAS}$
      1 CLK Period + CLK High to $\overline{RAS}$ Asserted (DP8440/41) + DRAM t_{RAC}
      + Data Set Up Time (i486)
      30.3 ns + 15 ns + 70 ns + 5 ns
      120.33 ns ⟶ 4 CLK Periods (121.2 ns)
   4b. Access Time from $\overline{CAS}$
      1 CLK Period + CLK to $\overline{CAS}$ Asserted (DP8440/41) + DRAM t_{CAC}
      + Data Set Up Time (68040)
      30.3 ns + 55 ns + 20 ns + 5 ns
      110.3 ns ⟶ 4 CLK Periods (121.2 ns)
   4c. Access Time from Column Address Valid
      1 CLK Period + CLK High to Column Address Valid (DP8440/41) + DRAM t_{AA} + Data Set Up Time (68040)
      30.3 ns + 51 ns + 35 ns + 5 ns
      121.3 ns ⟶ 4 CLK Periods (121.2 ns)

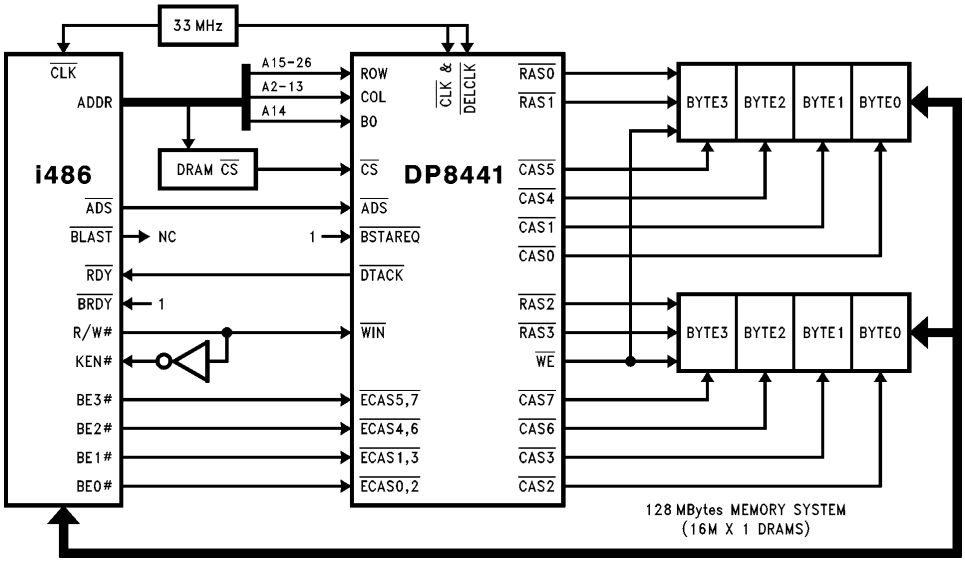
   From 4a, 4b and 4c, $\overline{DTACK}$ should assert from the 3rd rising CLK edge. Therefore program $\overline{DTACK}$ during opening accesses as 2T.
5. $\overline{RDY}$ Set Up Time (i486)
   1 CLK Period—$\overline{DTACK}$ Asserted from CLK High
   30.3 ns − 12 ns
   18.3 ns The i486 needs only 6 ns
6. Wait States Through $\overline{RDY}$ during Page Accesses
   1 CLK Period—(CLK High to $\overline{CAS}$ Asserted + DRAM t_{CAC} + Data Set Up Time
   30.3 ns − (12 ns + 20 ns + 5 ns)
   −6.7 ns ⟶ 1 Wait State. Page Accesses take 3 CLKs
7. $\overline{RAS}$ Low during Refresh

Program the DP8440/41 for 3T of refresh to guarantee 70 ns t_{RAS}. Same number of CLKs for precharge.

The AC timing parameters used in this application note were preliminary. The AC parameters have changed and the reader should refer to the latest DP8440/41 data sheet.

Note: This design doesn't burst. Every access is finished with $\overline{RDY}$ so the i486 starts every new access with a new $\overline{ADS}$ and provides a new address to the DRAM controller. During every read the design asserts $\overline{KEN}$# so it is up to the CPU to cache the next read cycles.

Interfacing the i486 and the DP8441 DRAM Controller



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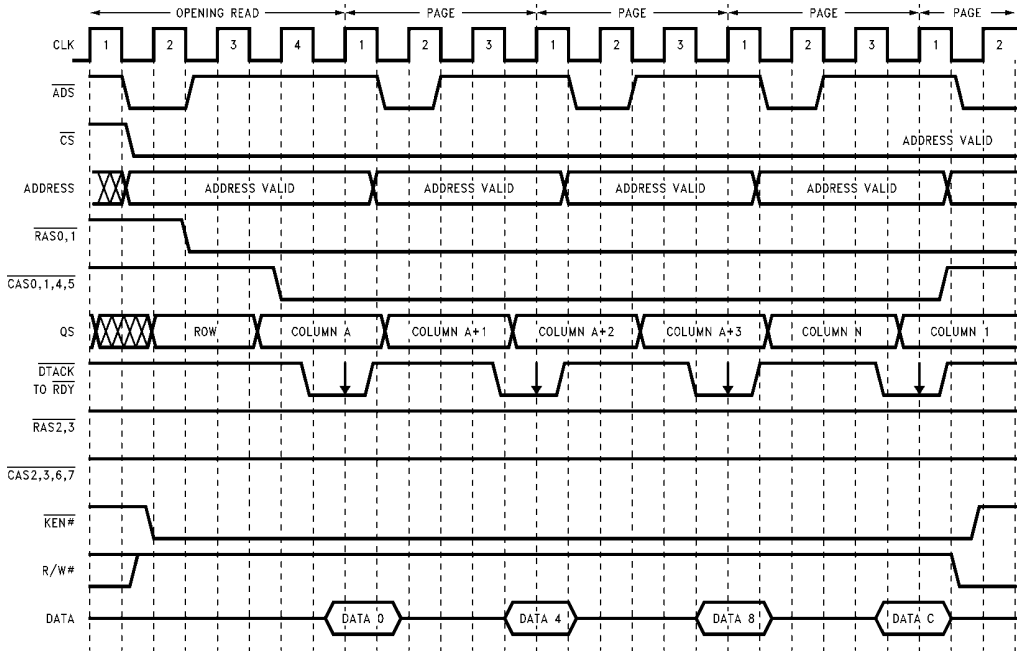
Opening and Non-Burst Cacheable Multiple Accesses. 4-3-3-3



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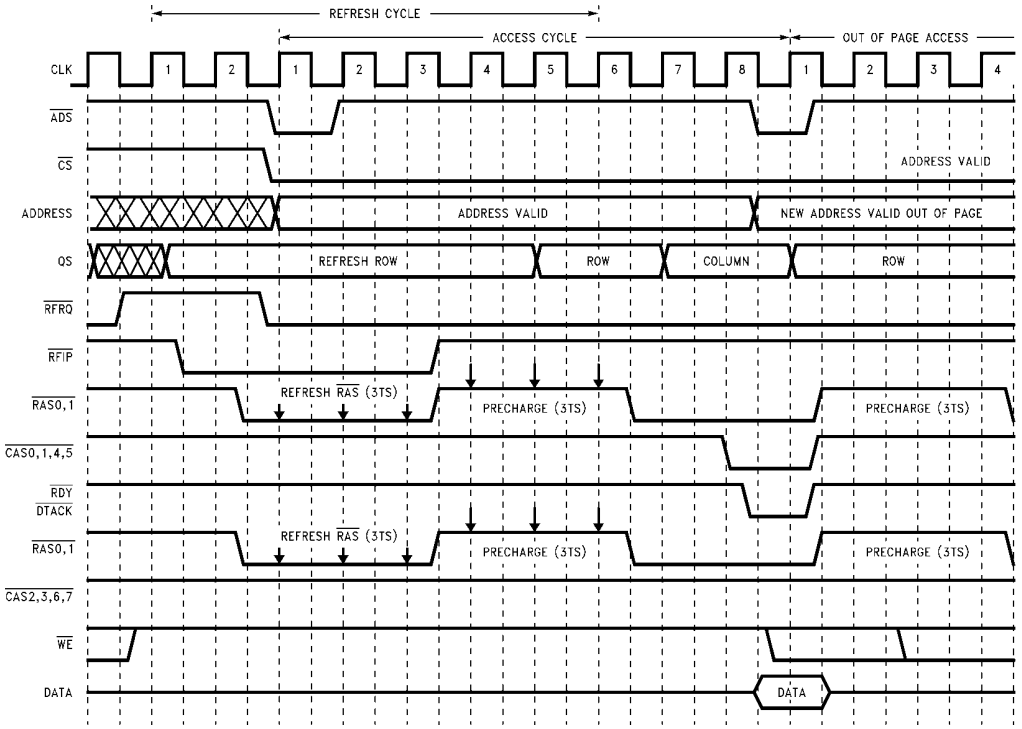
Refresh Cycle and Delayed Access



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National Semiconductor Corporation
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090
Tel: 1(800) 272-9959
TWX: (910) 339-9240

National Semiconductor GmbH
Livry-Gargan-Str. 10
D-82256 Fürstenfeldbruck
Germany
Tel: (81-41) 35-0
Telex: 527649
Fax: (81-41) 35-1

National Semiconductor Japan Ltd.
Sumitomo Chemical
Engineering Center
Bldg. 7F
1-7-1, Nakase, Mihama-Ku
Chiba-City,
Ciba Prefecture 261
Tel: (043) 299-2300
Fax: (043) 299-2500

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductores Do Brazil Ltda.
Rue Deputado Lacorda Franco
120-3A
Sao Paulo-SP
Brazil 05418-000
Tel: (55-11) 212-5066
Telex: 391-1131931 NSBR BR
Fax: (55-11) 212-1181

National Semiconductor (Australia) Pty, Ltd.
Building 16
Business Park Drive
Monash Business Park
Nottinghill, Melbourne
Victoria 3168 Australia
Tel: (3) 558-9999
Fax: (3) 558-9998