FAILSAFE Biasing of Differential Buses

National Semiconductor
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John Goldie
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OVERVIEW

Multi-Point bus configurations present two potential problems to the system I/O designer that do not commonly occur in Point-to-Point configurations. The two problems that the I/O system designer should take into account are bus contentions and the idle bus state. Bus contention occurs when more than one driver is active at a time during which the state of the bus is undetermined. Contentions may occur either by software or hardware errors. The second problem is an unknown bus state when all drivers are OFF. FAILSAFE biasing solves this problem by biasing the bus to a known state when ALL drivers are in TRI-STATE®(OFF). This application note is devoted to the topic of FAILSAFE biasing of differential buses.

INTRODUCTION

FAILSAFE biasing provides a known state when all drivers are in TRI-STATE (Hi-Z, OFF). This is especially important in bus configurations that employ more than one driver (transceiver), and is commonly known as a Multi-Point application (see *Figure 2*).

Electrical Characteristics Standard TIA/EIA-485 specifies that a maximum of 32 unit loads can be connected to a bus. A transceiver (driver/receiver pair) normally represents one unit load (see *Figure 2*). The bus is a half duplex bi-directional bus, (as data can flow in both directions), but only one driver should be active at a time. Termination is required (in most cases), and is only located at the two extreme ends of the bus. Note, that the termination shown on the left of *Figure 1* also provides a FAILSAFE bias.

BUS STATES

A FAILSAFE biased bus has only two states, HIGH (driven HIGH and FAILSAFE HIGH) and LOW (neglecting the transition region, and bus contentions). The bus can be driven HIGH or LOW by an active driver, or biased to a known state by external pull up and pull down resistors. These resistors provide the FAILSAFE bias, and the termination configuration is also known as a "power termination". The two bus states are shown in *Figure 2*.

In some applications these two states are defined as MARK/SPACE, OFF/ON, or 1/0. The definition of the two states is application dependent. When the signal transitions through the threshold region (±200 mV) the output state of the receiver is undefined. In *Figure 2*, the line is driven LOW, transitions HIGH, then the driver is disabled. The bus however, remains HIGH due to external FAILSAFE biasing.

Without FAILSAFE biasing, the receiver output would be undetermined when all drivers are OFF. The line would settle to only 1 mV–5 mV of each other ($|V_{OA}-V_{OB}|$, due to the internal input impedance network of the receiver), which is within the receiver's threshold limits (≤200 mV). If external noise is coupled onto the line, a false transition could occur, causing an error. In an asynchronous application, this false transition could be interpreted as a framing error, false start bit, or cause a false interrupt.

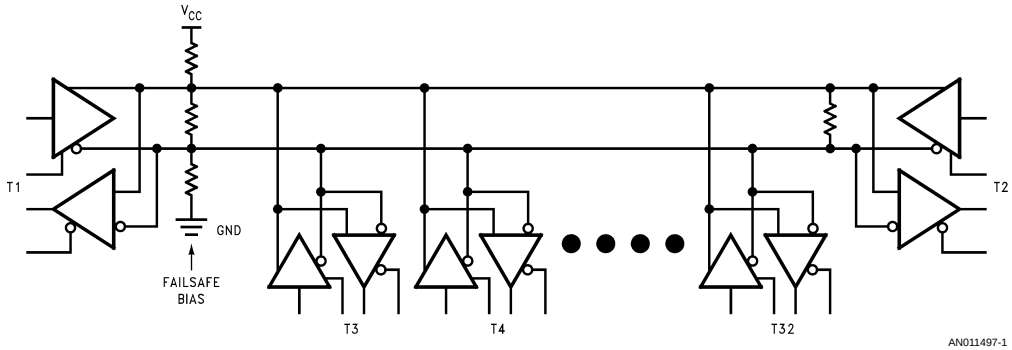
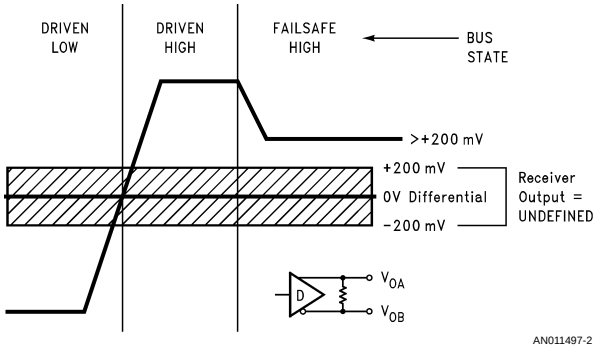


FIGURE 1. Typical Multi-Point Application



Note: Differential Plot $V_{OA} - V_{OB}$, not with respect to GND.

FIGURE 2. Bus States

SERIAL PROTOCOL

A popular format for low speed data transmission is an asynchronous protocol. A typical format is composed of 12 bits. The start bit initiates the timing sequence. This is detected by a transition from HIGH to LOW. Next are eight data bits, followed by an optional parity bit. Lastly, the line is driven HIGH for one or two bits (stop bits), signifying the end of the character. This format is illustrated in *Figure 3*. If another character is to be sent, the next start bit initiates the whole process all over again. However, if this was the last character, the line should remain HIGH until the next start bit, but the active driver is disabled. This presents a problem in multi-point applications, because between data transmissions all drivers are OFF. With no active drivers, the line is floating, and receiver outputs are undetermined. There are several solutions to this problem. One is through the use of alternate protocols (software), while the other is a hardware fix. The hardware fix uses external resistors to bias the line HIGH, when all drivers are off. The remainder of the application note describes the hardware method and the selection of component values.

In a Point-to-Point application (see *Figure 4*), the driver is normally always enabled. In this case the bus has only two states, driven HIGH, and driven LOW. FAILSAFE biasing is not needed, unless the drivers's enabling pin is also switched.

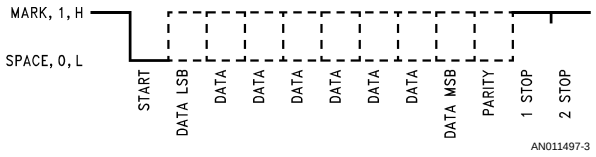


FIGURE 3. Asynchronous-UART Timing Format

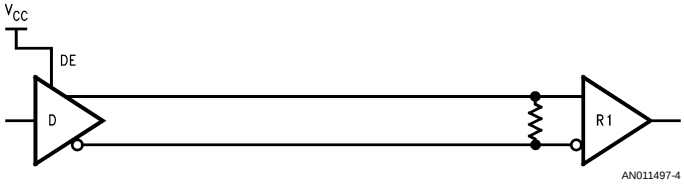


FIGURE 4. Typical Point-to-Point Application

CALCULATING RESISTOR VALUES FOR FAILSAFE BIASING

The external resistors are selected such that they provide at least a 200 mV (maximum receiver threshold) bias across the line, and not substantially load down the active driver.

In addition, the following guidelines should be met. The pull up resistor (Ra) and the pull down resistor (Rd) should be of equal value. This provides symmetrical loading for the driver. Termination resistor Rb should be selected such that it matches the characteristic impedance (Z_O) of the twisted pair cable. If the termination resistor matches the line, Rb = Z_O, there will be no reflections. At the other end of the cable, the equivalent resistance of Rc, Ra and Rd should also match the characteristic impedance of the line. In this case Rc is in parallel with Ra plus Rd (Rc//(Ra + Rd)). For this equivalent resistance to be matched to the line Rc must be greater than Z_O. Rc is typically 10Ω–20Ω greater than Z_O, but the actual value depends upon the values Ra and Rd. The FAILSAFE bias (Vfsb) is the potential dropped across the line. Note that this equation neglects cable resistance (see appendix), and that Rb is in parallel with Rc (Req = Rb // Rc). Therefore, the FAILSAFE bias is simply a voltage divider between Req, Ra, and Rd. The worst case occurs at V_{CC} − 5%, Ra and Rd + % tolerance, and Rc and

Rb − % tolerance. Under the worst case conditions the FAILSAFE bias must be greater than 200 mV for the receiver output to be in a guaranteed state.

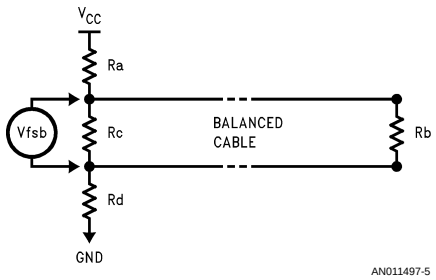


FIGURE 5. External FAILSAFE Bias Resistors

Example calculations for selecting FAILSAFE bias resistors:

Note: For this example assume the cable has a characteristic impedance (Z_O) of 120Ω

Step 1 Assume that Rc and Rb are equal and are selected to match Z_O.

$Rc = Rb = Z_O = 120\Omega$

Step 2 Calculate the equivalent resistance of Rc//Rb.

$Rc // Rb = 120\Omega // 120\Omega = 60\Omega$

Step 3 Calculate the Pull up and Pull down resistor values knowing that the FAILSAFE bias is 200 mV, and V_{CC} = 5V.

$Vfsb = V_{CC} (Req/(Ra + Req + Rd))$

solving for R' (defined as Ra + Rd)

$R' = ((Req)V_{CC}/Vfsb) - Req$

$R' = ((60\Omega)5V/0.2V) - 60\Omega = 1440\Omega$

Since Ra and Rd are equal, $Ra = Rd = 1440\Omega/2 = 720\Omega$

Step 4 Recalculate the equivalent resistance of Rc//(Ra + Rd).

$Rc//(Ra + Rd) = 120\Omega//(720\Omega + 720\Omega) = 110\Omega$

Since the equivalent resistance is close (within 10%) to the characteristic impedance of the cable (Z_O), no further adjustment of resistor values is required.

However, for the perfectionist, the matched value of Rc can be calculated by setting the following equation to Z_O and solving for Rc.

$$Z_O = Rc // (Ra + Rd)$$

$$\therefore Rc = 131\Omega$$

Now the equivalent resistance (Req = Rc // Rb) becomes 131Ω // 120Ω = 62Ω, which is very close to the original 60Ω. Standard value resistors values can be substituted to ease resistor selection, availability, and cost, before recalculating the FAILSAFE bias potential. Using a 5% tolerance table we find the following standard resistor values:

Ra = 750Ω, Rb = 120Ω, Rc = 130Ω, Rd = 750Ω

In order to verify that the selected values meet the criteria the following calculations should be completed:

1. $Rc//(Ra + Rd)=Z_O$
   $130\Omega//(750\Omega+750\Omega)=120\Omega$
2. $Req=Rb//Rc$
   $120\Omega//130\Omega=62\Omega$
3. $Vfsb = V_{CC} (Req/(Ra+Req+Rd))$
   $5V(62\Omega/(750\Omega + 62\Omega + 750\Omega)) = 200$ mV

Based on the example shown above, and a twisted pair cable with characteristic impedance of 120Ω, it has been determined that a 750Ω pull up and pull down resistor will provide a FAILSAFE bias of 200 mV. This value could be decreased slightly to provide a greater bias (>200 mV), and to meet the worst case power supply and resistor tolerance conditions. However, the value of Ra and Rd should not be reduced too low in order to minimize loading seen by the driver. This example illustrated that the largest values used for the pull up (Ra) and pull down (Rd) resistors should be 750Ω. The pull resistors should not be decreased substantially. Because when the driver is active (ON), it is required to develop a minimum of 1.5V across the cable termination. Using low impedance pull resistors further loads down the driver, making the 1.5V differential voltage even more difficult to meet.

Figure 6 illustrates the fully loaded (32 unit loads) TIA/EIA-485 bus with an external FAILSAFE bias network. Note that the FAILSAFE bias (Power Termination) is only located at one end of the bus. The other end employs a single resistor termination. The power termination is commonly located on the Master node of a Master/Slave bus configuration. This assures that the power to the pull up resistor is always on.

Before looking at the driver's load, the receiver's input impedance needs to be modeled to understand its effect upon the driver. The TIA/EIA-485 standard specifies a high receiver input impedance and an Input Voltage vs Input Current curve. An input impedance of 12 kΩ or greater is typically required to meet the V_{IN}/I_{IN} curve. A common mistake is to model the receiver's input impedance as a differential resistance, which is seen between the input pins. The input resistance is correctly modeled as a series resistor to a voltage reference node (AC ground point). The TIA/EIA-485 standard also allows for 32 unit loads to be connected in parallel. Therefore, the driver could see 32 12 kΩ resistors in parallel on each line. This is equivalent to a 375Ω resistor to an internal voltage reference point.

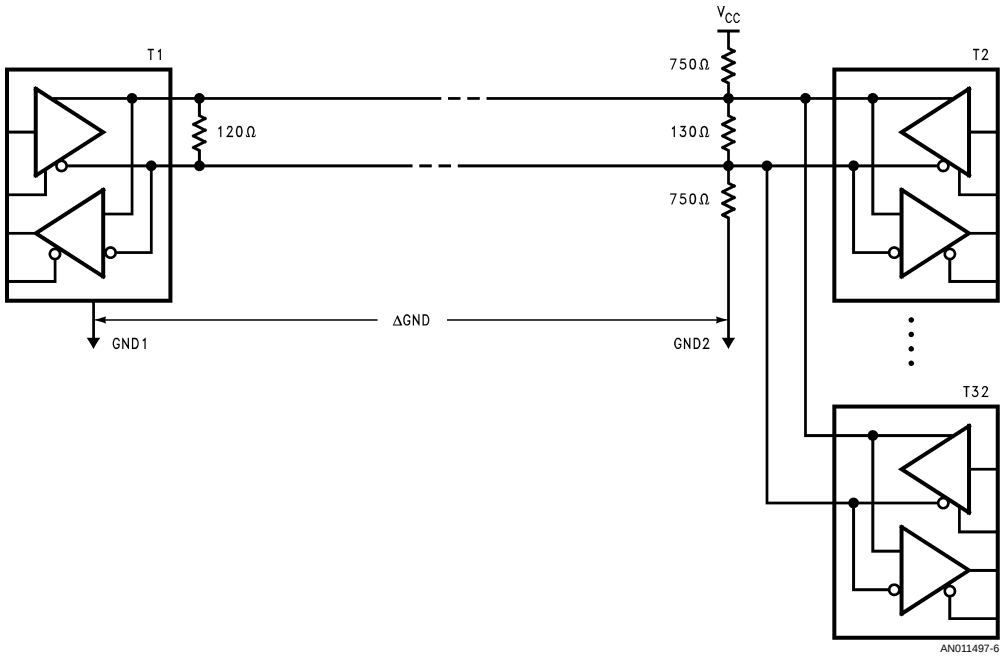


FIGURE 6. Fully Loaded TIA/EIA-485 Bus

The test circuit shown in *Figure 7* models the fully loaded TIA/EIA-485 bus. The 375Ω resistors that model the 32 parallel receiver input impedances, have been changed to 330Ω for two reasons. First, an active driver would also see 31 Tri-stated driver leakage currents (I_{OZ}), which is equivalent to 31 times 100 µA or 3.1 mA. This is equivalent to roughly 3 more unit loads. Therefore, 12 kΩ divided by 35(32 + 3) equals 342Ω. This value is further reduced to 330Ω to select standard value resistors. The dashed box represents 32 receiver loads and 31 passive driver leakage loads. The V_{CM} power supply models the maximum ground shifting specified (allowed) by TIA/EIA-485 (±7V). The differential voltage (VOD), measured across the 62Ω load (120Ω//130Ω), is required to be greater than 1.5V in magnitude by TIA/EIA-485.

Test data taken on three popular National TIA/EIA-485 drivers are shown in Table I. With the common mode voltage varied from −7V to +7V, all of the devices meet the 1.5V minimum differential voltage (VOD column).

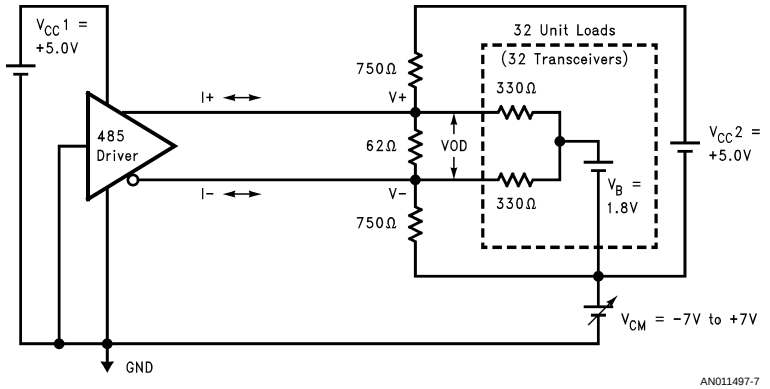


FIGURE 7. Full Load Equivalent Test Circuit

TABLE 1. Test Data for TIA/EIA-485 Drivers

Device	V_{CM} (V)	I− (mA)	I+ (mA)	V− (V)	V+ (V)	VOD (V)
DS3695	0	−41.7	+38.4	3.39	1.44	1.95
	−7	−56.1	+23.5	3.18	1.24	1.94
	+7	−13.4	+69.1	3.78	1.77	2.01
DS96172/4	0	−43.4	+42.4	3.25	1.14	2.11
	−7	−59.6	+28.0	3.08	0.94	2.14
	+7	−12.0	+70.4	3.47	1.46	2.01
DS96F172/4	0	−49.5	+45.3	3.67	1.33	2.34
	−7	−63.5	+30.6	3.47	1.14	2.33
	+7	−19.2	+74.2	4.00	1.71	2.29

Note 1: Current into device pin is defined as positive, current out of device pin is defined as negative, VOD ≥ 1.5V (TIA/EIA-485).

OPEN INPUT FAILSAFE FEATURE

All of National's TIA/EIA-485 receivers support the *OPEN INPUT FAILSAFE* feature. This feature provides a known state (HIGH) on the receiver output for the following cases, which are illustrated in *Figure 8*. The OPEN INPUT FAILSAFE feature is integrated into the input stage of the device. Normally high value (typically 120 kΩ) bias resistors pull the plus input high, and the minus input low. The value is large enough to properly bias the receiver when the inputs are open (non-terminated).

VALID OPEN INPUT CASES:

A. Unterminated Cables — With restrictions on data rate, stub length, and cable length, it is possible to construct an interface without termination resistors. Normally the cable length is very short with respect to the driver's rise time and the reflections that occur die out long before the next transition. For the idle line, the impedance seen acros the receiver input pins is very large (open) and thus the receiver output will be a HIGH state.

B. Unconnected Nodes — In a Multi-Point configuration, up to 32 nodes can be connected to the twisted pair. Termination should only be located at the two extreme ends of the cable. Therefore, if a middle node is disconnected from the cable, the OPEN INPUT FAILSAFE feature will put the receiver output into a stable HIGH state.

C. Unused Channels — If a high integration receiver IC (multi-channel) is being used, and all channels are not required, the unused channel(s) inputs can be left as no-connects. The OPEN INPUT FAILSAFE feature will force the unused channel into a stable HIGH state. This prevents the unused channel picking up external noise and oscillating, thereby increasing the power supply current (I_{CC}).

In all three cases, the impedance seen across the receiver input pins is very large or open, (∞) in contrast to a low impedance termination resistor of 150Ω or less. For these cases the receiver output will be HIGH. If the termination resistors were connected across the receiver input pins, then the receiver output is undetermined, unless the bus employs FAILSAFE biasing resistors.

SUMMARY

External FAILSAFE bias resistors can be used to solve the idle line state problem that commonly occurs in Multi-Point applications using asynchronous protocols. This is a well accepted hardware approach to solving the idle line state problem. In fact many complete INTERFACE standards have accepted this method. Examples include the Differential SCSI-1 and 2 (Small Computer System Interface) specifications, as well as the IPI (Intelligent Peripheral Interface) standard. This application note provides guidance to selecting proper resistor values that will provide an adequate FAILSAFE bias (Vfsb) while minimizing the loading effect on the driver.

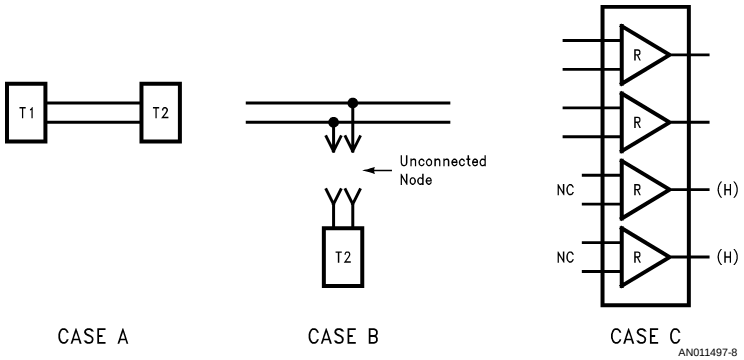


FIGURE 8. Applications of OPEN INPUT FAILSAFE Feature

APPENDIX

A more elaborate calculation that takes into account the DC resistance of the twisted pair cable is provided in this appendix. (See *Figure 9*). For this example assume the following:

Ra = Pull Up Resistor
Rb = Slave End Cable Termination Resistor
Rc = Master End Cable Termination Resistor
Rd = Pull Down Resistor
Re = Cable DC Resistance
Rf = Cable DC Resistance
Rdcr = Re + Rf
Vfsbm = FAILSAFE Bias Potential @ Master end of cable
Vfsbs = FAILSAFE Bias Potential @ Slave end of cable

and

1. Ra = Rd for symmetrical loading
1. REQ = Rc//(Ra + Rd)
   REQ = (Rc(Ra + Rd))/(Ra + Rc + Rd).

Note 2: Assume V_{CC} = 5V ± 5%.

Note 3: Resistor Tolerance = ±2%.

Note 4: Worst Case occurs at V_{CC} − 5%, Ra and Rd + 2%, Rb and Rc − 2%.

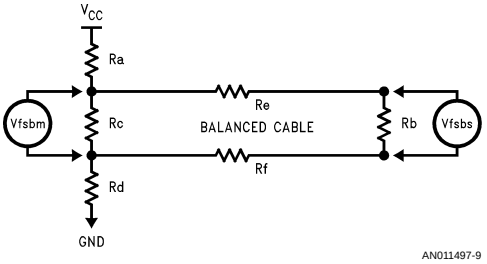


FIGURE 9. A-1. Cable Model

Equations:

FAILSAFE Bias at the Master end of the cable is:

$$Vfsbm = \frac{Rc//(Rb + Rdcr)}{Ra + Rd + (Rc//(Rb + Rdcr))}V_{CC}$$

$$Vfsbm = \frac{Rc(Rb + Rdcr)}{(Ra + Rd)(Rc + Rb + Rdcr) + Rc(Rb + Rdcr)}V_{CC}$$

The FAILSAFE Bias at the Slave end is simply a voltage divider between the cable DC resistance and the Slave end termination resistor.

$$Vfsbs = \frac{Rb}{Rb + Rdcr}\,Vfsbm$$

REFERENCES

1. EIA Standard EIA RS-485, Standard for Electrical Characteristics of Generators and Receivers, for use in a Balanced Digital Multipoint Systems, EIA, Washington, D.C., 1983.
2. EIA Standard EIA RS-422-A, Electrical Characteristics of Balanced Voltage Digital Interface Circuits, EIA, Washington, D.C., 1978.
3. FAILSAFE Lab Notes, Gary Murdock, National Semiconductor, 1987.

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