Futurebus+ BTL Grounding Scheme

National Semiconductor
Application Note 835
Joel Martinez
June 1992

Due to the high current and very high speed capability of the Futurebus+ driver output stage, device ground pin allocation, circuit board layout and bus grounding are critical factors that affect the system performance. The series inductance on any ground path should be minimized to improve ground noise and ringing. The voltage spike generated by an inductor is described by the equation;

$$V = L \, di/dt$$

where,
- V Voltage
- L Inductance
- di Change in Current
- dt Change in Time

Ground bounce is dependent on the rate at which current changes with respect to time. Reducing the current passing through the inductor and minimizing the inductance will reduce the noise.

It is desirable to have multiple ground pins to distribute the current among several ground paths, thereby reducing the ground bounce. There are many ground pins on the transceivers which can be categorized into three types, Bn GND, GND and QGND. These grounds are electrically isolated within the device to reduce noise coupling between them. Externally the grounds should be connected to a common point. The driver is capable of sinking up to 80 mA with a rise and fall time of 3 ns typical. Assuming that L = 10 nH, the noise spike will be (10 nH) (80 mA/3 ns) = 266 mV per output which is acceptable. Improper ground pin allocation can have devastating consequences. In the following example, we will assume a 9-bit device with a single ground return. The noise spike from this will be (10 nH) (80 mA/3 ns) (9 output) = 2.4V which is unacceptable. For this reason, each driver output has a dedicated ground return, Bn GND. QGND, quiet ground, is used for DC circuits such as bandgaps, and current sources. QGND, the most critical of the ground pins, is a reference point to the bandgap circuit which sets the receiver threshold and other non-switching circuits. The purpose of isolating QGND is to keep the receiver threshold at the same reference as signals coming off the backplane. Noise coupled to this ground, which should be avoided, will have a direct effect on the receiver threshold. GND is used for other logic circuits.

The goal is to isolate QGND from high current switching signals. The principles above can be applied to printed circuit board design using Futurebus+ transceivers. *Figure 1* and *Figure 2* illustrate these principles. The board shown on *Figure 1* has two ground planes. Both ground palnes are connected to each other and to the backplane ground at the connector. In a Futurebus+ board, a third of the connector pin array is allocated to ground along with the power ground pins which are not shown. QGND is isolated from Bn GND on separate ground planes. GND should be connected on the same plane as Bn GND, as shown on *Figure 1*. In *Figure 2*, there is a single ground plane which connects GND and Bn GND. QGND is connected to the connector ground pin via a PCB trace. These traces should not carry any switching currents and should be kept as short as possible. There are many ways to layout and construct the grounding scheme for a board as long as you adhere to these principles.

1. Reduce the ground path inductance from the transceiver to the backplane.
   - A. Short traces.
   - B. Ground planes and wide traces.
   - C. Use vias to connect ground pins to ground planes.
   - D. Use as many connector pins for ground as possible.
   - E. Place transceivers as close to the connector as possible.
2. Isolate Bn GND's from QGND's.
   - A. Separate ground paths common at connector only.

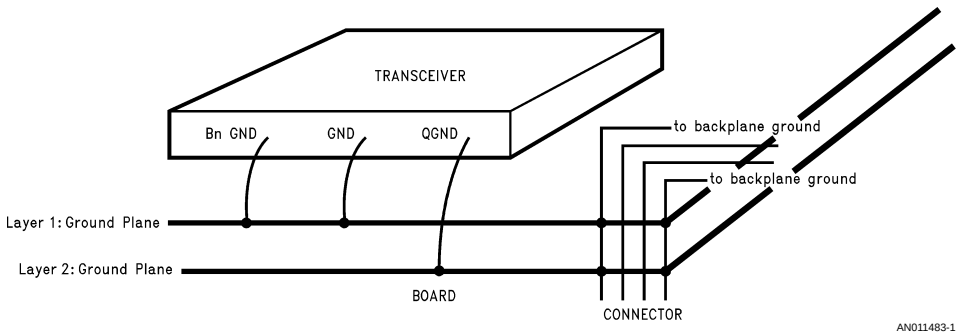

FIGURE 1. Ground Structure with Two Ground Planes

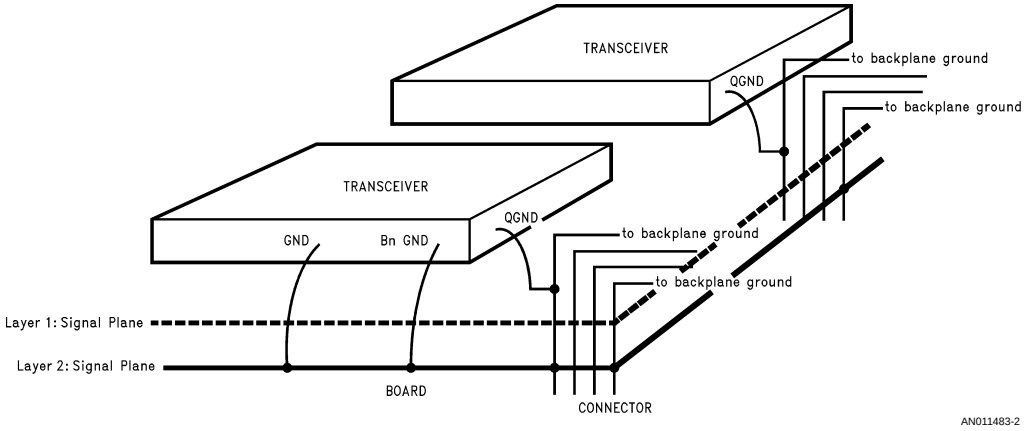

FIGURE 2. Ground Structure with One Ground Plane

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com

www.national.com

National Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 1 80-530 85 85
English Tel: +49 (0) 1 80-532 78 32
Français Tel: +49 (0) 1 80-532 93 58
Italiano Tel: +49 (0) 1 80-534 16 80

National Semiconductor Asia Pacific Customer Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: sea.support@nsc.com

National Semiconductor Japan Ltd.
Tel: 81-3-5620-6175
Fax: 81-3-5620-6179