Processor Oriented EPROM (POP™) Simplifies Design/ Improves Performance

National Semiconductor
Application Note 830
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INTRODUCTION

EPROMs are widely used for non-volatile code/data storage in a variety of systems ranging from computers to instrumentation. A number of applications like laser printer engines and analytical instruments (e.g. spectrometers) rely heavily on look-up tables for their operation. The performance in all such applications can be improved by using high-speed EPROMs and data buffers, which demand a premium price.

National Semiconductor has introduced a new family of EPROMs, called *Processor Oriented EPROMs* (POP), which will improve the performance without requiring faster speed EPROMs. One of the members of POP Family is *Immediate Access EPROMs.* These devices improve the interface to 32-bit popular microprocessors like '030 and X386.

The POPs improve the interface by addessing two areas: guaranteed data hold time at the end of EPROM access cycle and faster data bus disable time. In this application note we will show how the use of *Immediate Access EPROMs* help in the system performance improvement. Two cases are studied—the first is a 68030-based system and the second is a X386-based system. For each case the design with the standard EPROM and the POP is discussed. It will be shown that to get the same performance as with 120 ns 27P512 (POP), 80 ns (for '030 design) and 70 ns (for X386 design) 27C512 (standard) EPROMs are required. The general guidelines apply to any standard microprocessor and some microcontrollers.

TARGET APPLICATIONS

- High Performance Computers
- Instrumentation—Look-Up Table Based
- Digital Switch (PBX)
- Laser Printer Engines
- Automotive Controllers

A: 68030-EPROM INTERFACE

Figure 1 shows the block diagram of EPROM interface to 68030-25.

For 68030 CLK input is the specified processor frequency clock and all the timing is specified with respect to CLK. For 25 MHz 68030 CLK period is 40 ns.

The 68030 supports two types of read and write operations—asynchronous and synchronous. Lower performance systems may utilize asynchronous interface, where 8- or 16-bit EPROM data bus is used and multiple transfers are required to fetch a 32-bit operand. Higher performance systems use 32-bit EPROM data bus and do a synchronous data transfer. The fastest synchronous read operation requires two clock cycles for completion as shown in *Figure 2.*

The cycle begins with valid address and control signals on 68030 output pins. The buffered address is applied to the EPROM. The control logic decodes the address and enables the EPROM. After the EPROM access time the data is available for reading to the processor. The control logic issues $\overline{\text{STERM}}$ signal to the 68030 to indicate the cycle is over. Due to longer access time for EPROMs, one will have to introduce wait states before $\overline{\text{STERM}}$ is returned. Table I defines the relevant AC specifications for the read operation for the 68030. With the basic timing explained let us see what the interface looks like in detail.

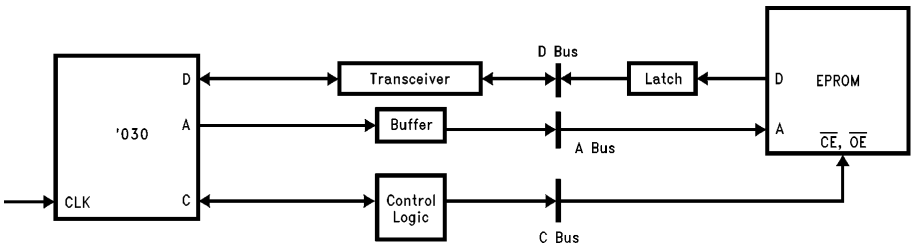

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FIGURE 1. 68030-EPROM Interface Block Diagram

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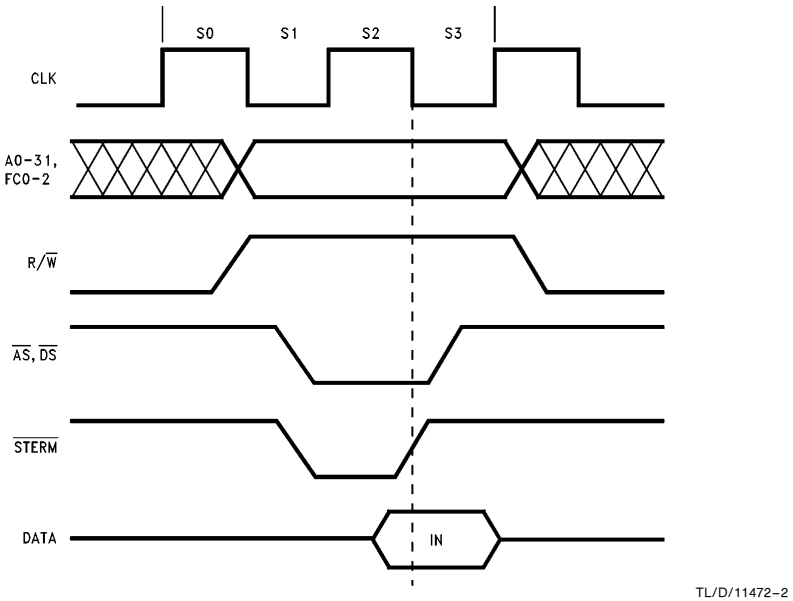

FIGURE 2. The Fastest Synchronous Read Cycle (68030)

TABLE I. AC Specifications for 68030 Read Operation (Synchronous)

		Min	Max
CLK Period	(t1)	40 ns	80 ns
A0–A31, R/$\overline{W}$ Valid after Rising Edge of CLK	(t6, t18)	0 ns	20 ns
$\overline{AS}$, $\overline{DS}$ Valid after Falling Edge of CLK	(t9)	3 ns	18 ns
D0, D31 Setup before Falling Edge of CLK	(t27)	2 ns	
D0, D31 Hold after Falling Edge of CLK	(t30)	8 ns	

DESIGN WITH STANDARD EPROM

Figure 3 shows the complete EPROM interface to the 68030. Due to the synchronous interface 32-bit EPROM data bus (four 27C512s) is used. The 68030 design requires the use of address strobe ($\overline{AS}$) signal to qualify the chip selects. The decoder PAL 16L8-7 (7.5 ns delay) uses the address and $\overline{AS}$ to generate $\overline{EPROMCS}$. F244 is used to buffer the processor address.

The LATCHENABLE signal latches the EPROM data in F373, so that 68030 data hold time requirements can be met. The output enable signals applied to the EPROM and the F373 are used to enable and disable the data bus. The control PALs use CLK and $\overline{CLK}$ (inverted CLK) to generate the various control signals. $\overline{EPROMSTERM}$ indicates the end of EPROM read cycle. The memory controller uses this signal to issue $\overline{STERM}$ to the processor.

Figure 4 shows the timing diagram for 27C512 read cycle. For a (4 + ½) cycle EPROM access (the '030 reads the data on the falling edge of CLK), 120 ns 27C512s are required as shown in Equation 1.

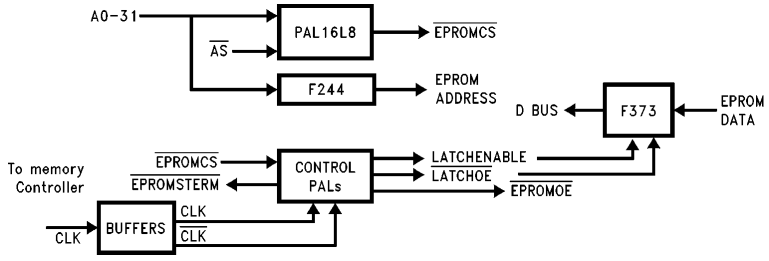

FIGURE 3. Complete EPROM Intertace to 68030

For (n + ½) clock cycle accss the EPROM timing equation is,

t_2	+ t_9	+ Max {t_{PAL}, t_{PD}244}	+ t_{ACC}
½ CLK period	$\overline{CLK}$ to $\overline{AS}$ delay	Max {PAL delay, 244 delay}	EPROM access time
+ t_{PD} 373	+ t_{PD} (transceiver)	+ t_{27}	≤ (n + ½) * (t_{CLK})
latch delay	transceiver delay	data setup time to 68030	

Substituting the values from the 68030 datasheet,

For a 4.5 clock cycle access

$20 + 18 + 7.5 + t_{ACC} + 5 + 5 + 2 \leq 4.5 * (40)$ .....(1)

$t_{ACC} \leq 123$ ns

For a 3.5 clock cycle access

$20 + 18 + 7.5 + t_{ACC} + 5 + 5 + 2 \leq 3.5 * (40)$ .....(2)

$t_{ACC} \leq 83$ ns

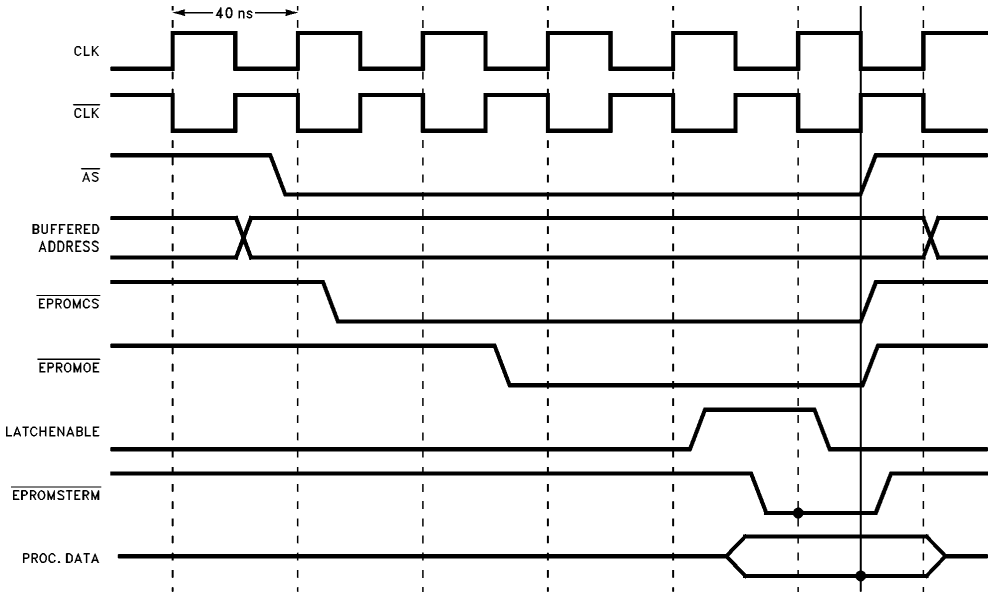

FIGURE 4. Timing Diagram for 27C512 Read Cycle

About 3 ns margin takes care of delays due to trace lengths, clock skews and loading effects. $\overline{EPROMSTERM}$ is generated during the fifth cycle, to be sampled on the rising edge of CLK in the sixth cycle so that a new operation can begin after a total of **six clock cycles.**

DESIGN WITH POP (27P512—120 ns)

The 68030 Interface to POP looks very much the same as the Standard EPROM interface. Because the Immediate Access EPROM has a minimum of 7 ns hold time, F373 latch is no longer required. A buffer is introduced in place of the F373, assuming a large load on the data bus. $\overline{EPROMSTERM}$ can be generated one cycle early as compared to the standard EPROM Design. The complete timing diagram is shown in *Figure 5.*

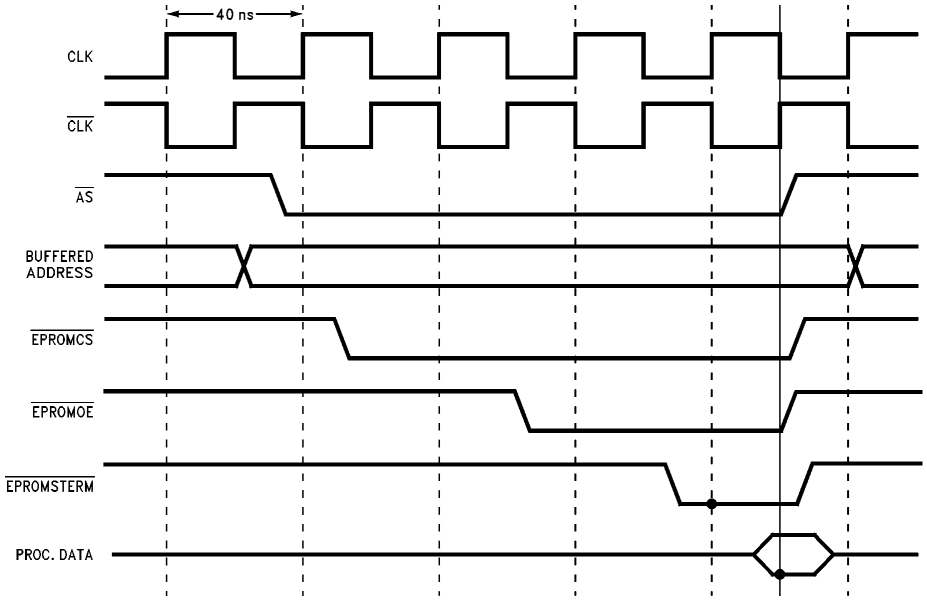

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FIGURE 5. Timing Diagram for 27P512 Read Cycle

The access to the EPROM still takes four-and-half cycles for 120 ns 27P512. Due to the data hold feature of the 27P512, EPROMSTERM is generated one clock cycle early and a new operation can begin immediately after a total of **five clock cycles**. The combination of 7 ns minimum hold time of 27P512 and 3 ns minimum delay from AS to EPROMCS satisfies the data hold time requirement of 8 ns in 68030 read operation. Thus, with POP, faster EPROM read cycles are possible as compared to the standard EPROM. To achieve the same pertormance with the standard EPROM, 80 ns 27C512 will be required as opposed to 120 ns 27P512 as shown in Equation 2. In the standard design the fast decoding logic used cannot guarantee that EPROMCS can be maintained for 8 ns after falling edge of CLK. In fact, that is why F373 was used to capture EPROM data in the previous scheme.

If the loading on the data bus is light, due to faster disable time of the POP the buffer at the output of the 27P512 can be omitted leading to a simpler, compact design. In the standard EPROM even if the loading is light an additional buffer is required to ensure that the EPROM does not drive the data bus into the next cycle.

B: X386-EPROM INTERFACE

Figure 6 shows the block diagram of EPROM interface to the X386-20. The X386 requires CLK2 input, which is the double frequency clock, and all the timing parameters are specified with respect to this clock. For 20 MHz X386, the CLK2 period is 25 ns.

The X386 supports a variety of read and write cycles. For the EPROM interface the non-pipelined accesses are considered. The fastest non-pipelined read cycle (henceforth called ''read cycle'') requires two bus states as shown in *Figure 7.* The cycle begins with valid address, byte enables and control signals on the X386 output pins. The buffered address is applied to the EPROM. The control logic decodes the address and enables the EPROM. After the EPROM access time the data is available for reading to the processor. The control logic issues READY signal to the processor and the cycle is over.

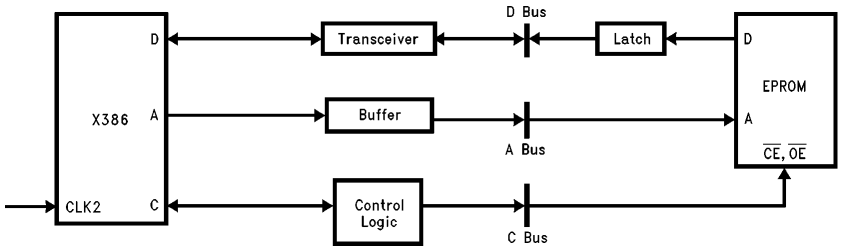

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FIGURE 6. X386—EPROM Interface Block Diagram

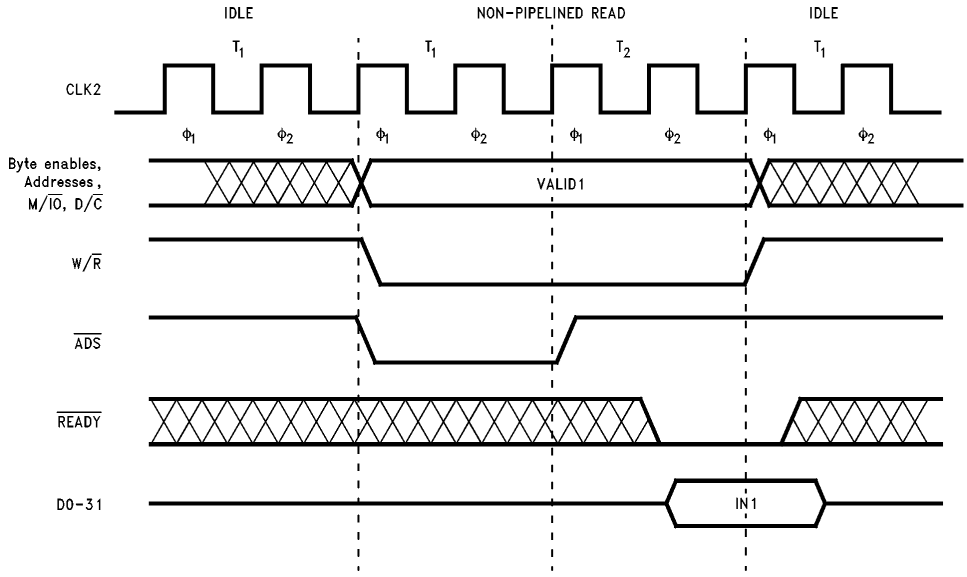

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FIGURE 7. The Fastest Non-Piplined Read Cycle

Due to longer access times for EPROM, one will have to introduce wait states before READY is returned. Table II defines the relevant AC specifications for the read operation. With the basic timing explained let us see what the interface looks like in detail.

TABLE II. AC Specification for X386 Read Operation

	Min	Max
CLK2 Period (t1)	25 ns	125 ns
A2–A31, Valid after Rising Edge of CLK2 (Phase 1) (t6)	4 ns	30 ns
W/R, M/IO Valid after Rising Edge of CLK2 (Phase 1) (t10)	6 ns	28 ns
D0, D31 Setup before Rising Edge of CLK2 (Phase 1) (t21)	11 ns	
D0, D31, Hold after Rising Edge of CLK2 (Phase 1) (t22)	6 ns	

DESIGN WITH STANDARD EPROM (27C512)

The X386 data bus is 32-bit wide whereas, 27C512 has a 8-bit data bus. A variety of options are possible for interfacing these two different width data buses. The X386 has BS16 input, which informs the processor whether the current cycle is a 16-bit cycle or not. By using this input—we can design 16-bit EPROM interface, that uses two 27C512s in parallel. In this case, we need to generate A1, from the byte enables (BE0–BE3). The A1 generation logic is not shown, but can be derived easily. The interface is shown in *Figure 8.*

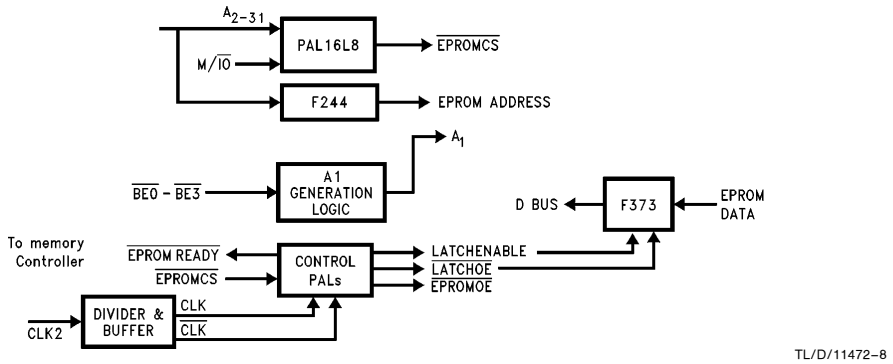

FIGURE 8. Complete EPROM Interface

The F244 is used to buffer the processor address to be applied to the 27C512 address bus. PAL16L8-A (25 ns delay) decodes the address and M/$\overline{IO}$ signal to generate $\overline{EPROMCS}$ signal. The LATCHENABLE signal latches the EPROM data in F373, so that X386 data hold requirements can be met. The output enable signals applied to the EPROM and the F373 are used to enable it and disable the data bus. These need to be synchronized for the proper timing relationship. The double frequency CLK2 signal is used to derive two half-frequency signals, CLK and $\overline{CLK}$, which drive the EPROM control PALs. $\overline{EPROMREADY}$ signal indicates the end of EPROM read cycle. The memory controller uses this signal to issue $\overline{READY}$ to the processor.

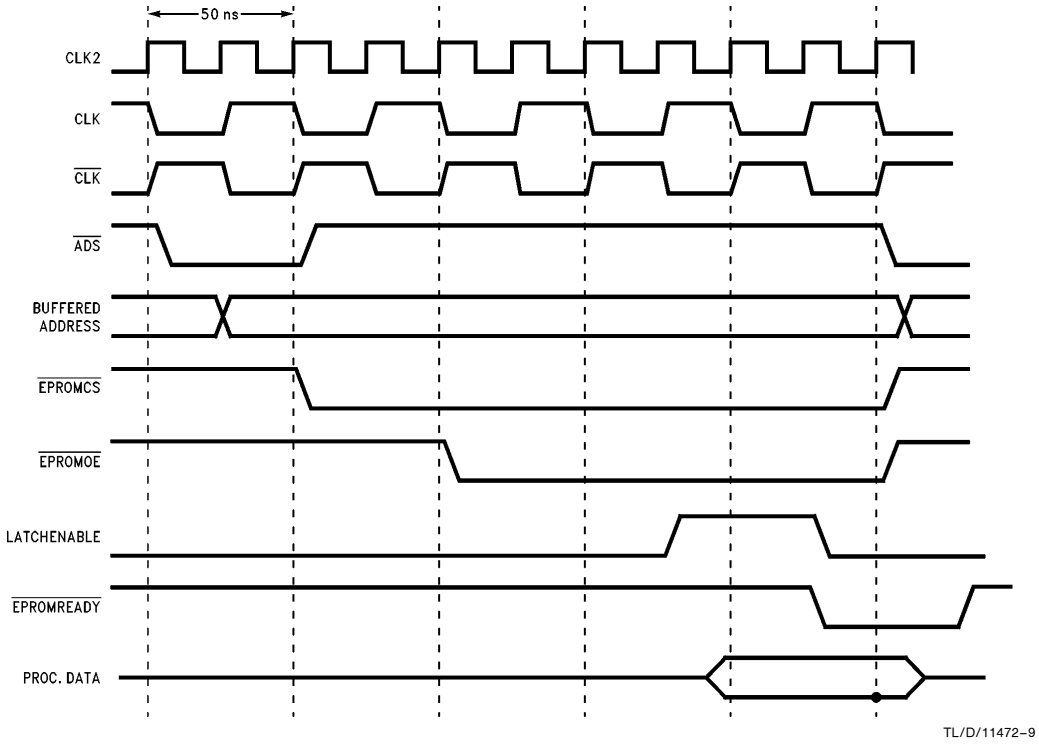

FIGURE 9. Timing Diagram for 27C512 Read Cycle

Figure 9 shows the timing diagram for the 27C512 Read Cycle. For a 4-cycle EPROM access, 120 ns 27C512 are required as shown in Equation 3 below.

About 4 ns margin takes care of delays due to trace length, clock skews and loading effects. $\overline{\text{EPROMREADY}}$ is generated in the fifth cycle, so that, a new operation can begin after a total of **five cycles.**

DESIGN WITH POP (27P512)—120 ns

The interface to the POP looks very much as the standand EPROM interface. The address decoder, A1 generation logic and the address buffer are unchanged. Because the Immediate Access EPROM has a minimum of 7 ns data hold time, the F373 latch is no longer required. A buffer is introduced in place of the F373, assuming a large load on the data bus. $\overline{\text{EPROMREADY}}$ can be generated one clock cycle earlier as compared to the standard EPROM design cycle. The complete timing diagram is shown in *Figure 10.*

The access to the EPROM still takes four cycles, for 120 ns 27P512. Due to data hold feature of the 27P512 $\overline{\text{EPROM READY}}$ is generated one clock cycle early and a new operation can begin immediately after a total of **four cycle.** 7 ns minimum data hold time of the 27P512 satisfies the data hold time requirement of 6 ns in the X386 read operation. Thus, due to hold time feature of Immediate Access EPROM, faster EPROM read cycles are possible as compared to the standard EPROM. To achieve the same performance as 120 ns POP, 70 ns standard EPROM are required as shown in Equation 4.

For n clock cycle access the EPROM timing equation is,

t_6	+ Max {t_{PAL}, t_{PD}(buffer)}	+ t_{ACC}	+ t_{PD} (latch)
CLK2 to address valid	Max {PAL delay, buffer delay}	EPROM access time	buffer delay
+ t_{PD} (transceiver)	+ t_{21}	≤ (n) (2) t_{CLK2}	
transceiver delay	data setup time to X386		

Substituting the values from the datasheet,

For a 4-cycle access

$$30 + 25 + t_{ACC} + 5 + 5 + 11 \leq 4 * (50) \quad \ldots\ldots (3)$$

$$t_{ACC} \leq 124 \text{ ns}$$

For a 3-cycle access

$$30 + 25 + t_{ACC} + 5 + 5 + 11 \leq 3 * (50) \quad \ldots\ldots (4)$$

$$t_{ACC} \leq 74 \text{ ns}$$

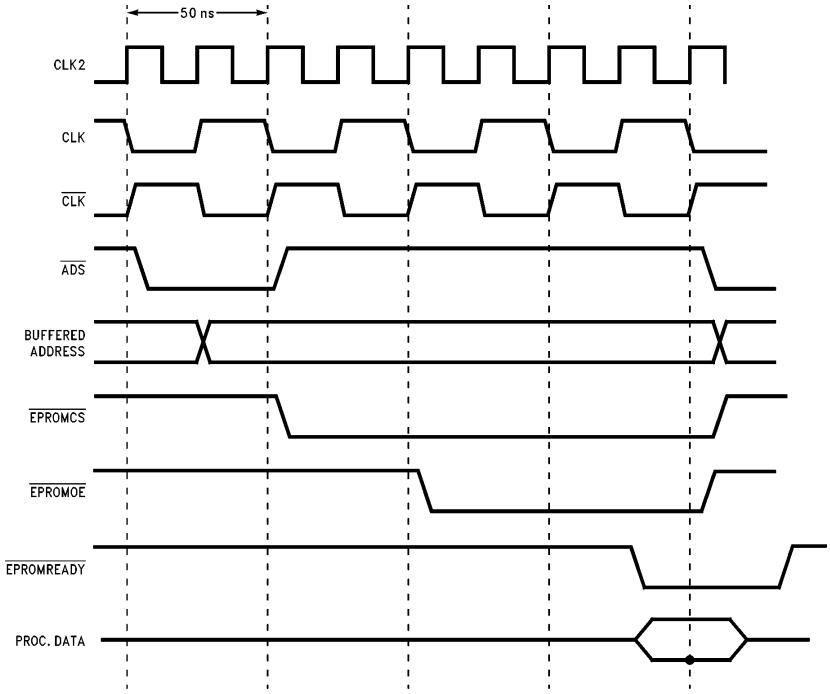

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FIGURE 10. Timing Diagram for 27P512 Read Cycle

In the Immediate Access EPROM design the data buffer at the output of 27P512 can be omitted depending on the application. Due to the fast disable time of the 27P512 (25 ns as opposed to 50 ns in the 27C512), if the loading on the data bus is light the 27P512 outputs can directly drive the data bus. In such a case, even simpler and compact design is achieved.

CONCLUSION

National's POP family of devices are ideal for the popular processor based design (e.g. '030 and X386), which demand performance from the non-volatile storage devices without paying significant cost penalty. For the same access time the number of wait states is reduced leading to a maximum of 20% performance improvement. Standard faster access EPROMs can be designed in, but with extra components and added complexity of design. Depending on the loading conditions the external buffer at the POP output can be omitted without causing data bus contention. The reduced component count leads to compact PCB real estate which reduces design and manufacturing costs.

The performance improvement is achieved though two features offered by the POP devices. The data hold feature guarantees data at the EPROM output pins at the end of access cycle. The fast data float feature assures that EPROM will release the data bus much faster compared to the standard EPROMs. As shown in this application note EPROM memory subsystem can be easily designed with POP with improved performace and reduced component count.

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