Reflections: Computations and Waveforms

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OVERVIEW

In this application note, the logical progression from the ideal transmission line to the real world of the long transmission line with its attendant losses and problems is made; specifically, the methods to determine the practicality of a certain length of line at a given data rate is discussed. Transmission line effects on various data formats are examined as well as the effects of several types of sources (drivers) on signal quality. A practical means is given to measure signal quality for a given transmission line using readily available test equipment. This, in turn, leads to a chart that provides the designer a way to predict the feasibility of a proposed data-transmission circuit when twisted-pair cable is used. This application note is a revised reprint of section three of the Fairchild Line Driver and Receiver Handbook. This application note, the second of a three-part series (see AN-806 and AN-808), covers the following topics:

- The Initial Wave
- Cut Lines and a Matched Load
- Kirchoff's Laws and Line-Load Boundary Conditions
- Fundamental Principles
- Tabular Method for Reflections — The Lattice Diagram
- Limitations of the Lattice Diagram Method
- Reflection Effects for Voltage-Source Drivers
- Reflection Effects for Matched-Source Drivers
- Reflection Effects for Current-Source Drivers
- Summary — Which are the Advantageous Combinations?
- Effect of Source Rise Time on Waveforms

INTRODUCTION

In AN-806 it was determined that transmission lines have two important properties: one, a characteristic impedance relating instantaneous voltages and currents of waves traveling along the line and, two, a wave propagation velocity or time delay per unit length. In this chapter, both $Z_0$and δ are used to compute the line voltages and currents at any point along the line and at any time after the line signal is applied. Also, concepts of reflections and reflection coefficients are explored along with calculating methods for voltages and currents.

THE INITIAL WAVE

Application Note AN-806 also showed that for most practical purposes, where fast rise and fall time signals are concerned, the characteristic impedance of the line actually behaves as a pure resistance $(R_0 = \sqrt{L/C})$.

Figure 1 shows a generator comprised of a voltage source (magnitude V), a source resistance of R_S ohms, and a switch closing at time t = 0 connected to a lossless, infinite length transmission line having a characteristic resistance, R_0. Because the relationship of V_{IN} to I_{IN} is known as $V_{IN} = R_0 I_{IN}$, the lossless transmission line can be replaced with a resistor as shown in *Figure 2*. The loop equation is.

$$I_{IN} (R_S + R_0) = V \quad (1)$$

Substituting V_{IN}/R_0 for $I_{IN}$and collecting terms shows

$$V_{IN} = V\left(\frac{R_0}{R_0 + R_S}\right) \quad (2)$$

This shows that both source and characteristic resistances act as voltage dividers for the source voltage V. *Figure 3* shows voltage and current steps for the various source resistances. Source resistances of less than R_0 produce initial voltage steps on the line which are greater than half the compliance of the source voltage, V. A matched source ($R_S = R_0$) produces voltage steps exactly half of V and source resistances greater than R_0 produce an initial voltage step less than one half V in magnitude. Generators can be classified into three categories:

- Voltage source types where $R_S < R_0$
- Matched source types where $R_S = R_0$
- Current source types where $R_S > R_0$

Waveforms of these types will be discussed more fully in AN-808 on long line effects. Suffice to say that initial voltage wave amplitude depends greatly on source resistance. Voltage source type drivers produce higher amplitude initial voltage waves in the line than either matched source or current source type drivers.

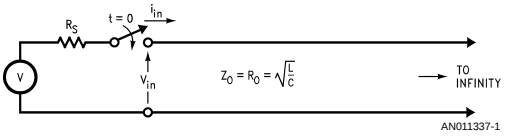


FIGURE 1. Generator Driving an Infinite Transmission Line

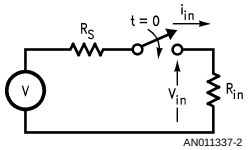


FIGURE 2. Thevenin Equivalent for Initial Wave

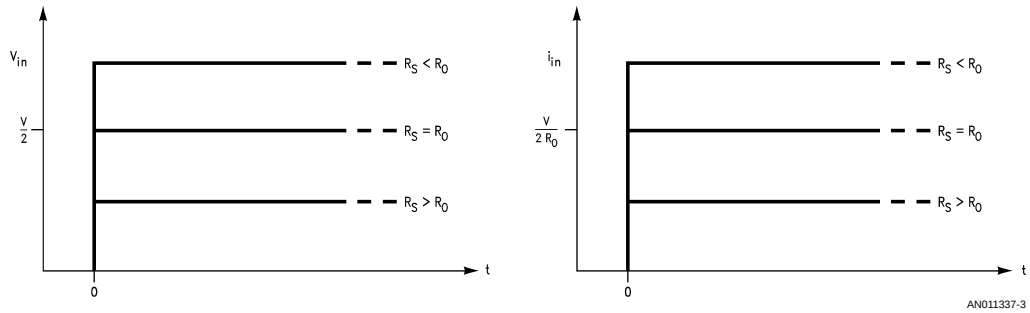


FIGURE 3. Voltage/Current Steps for Three Source Resistances

CUT LINES AND A MATCHED LOAD

In examining an infinite, lossless line (*Figure 4*), it is already known that the ratio of line voltage to current is equal to the characteristic resistance of that line. The line is lossless, and the same voltages and currents should appear at point x down the line after a time delay of xδ. If the line at point x is cut, and a resistor of value R_0 is inserted, there would not be a difference between the cut, terminated finite line and the infinite line. The v_x and i_x waves see the same impedance (R_0) they were launched into at time t = 0, and indeed, the waves are absorbed into R_L (= R_0) after experiencing a time delay of τ = xδ. So, from an external viewpoint, an infinite-length lossless line behaves as a finite-length lossless line terminated in its characteristic resistance.

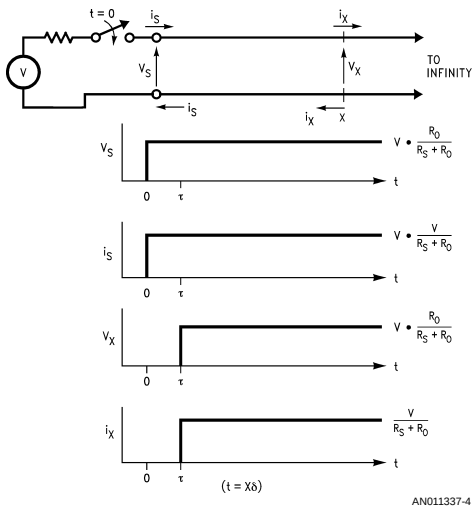


FIGURE 4. Voltages and Current on an Infinite Length Line

KIRCHOFF's LAWS AND LINE-LOAD BOUNDARY CONDITIONS

The principle of energy conservation, widely known and accepted in the sciences, applies as well to transmission line theory; therefore, energy (as power) must be conserved at boundaries between line and load. This is expressed in an English language equation as follows.

$$\left[\begin{array}{c}\text{Power available at}\\ \text{the line end}\end{array}\right] = \left[\begin{array}{c}\text{Power absorbed}\\ \text{by the load}\end{array}\right] + \left[\begin{array}{c}\text{Power not absorbed}\\ \text{by the load}\end{array}\right]$$

Figure 5 shows power available at the line end is derived by the following formula. (This is assuming in-phase current and voltage.)

$$P_x = i_x \bullet v_x = \frac{v_x^2}{R_0} \quad (3)$$

The power *absorbed* by the load will be

$$P_L = v_L \bullet i_L = \frac{v_L^2}{R_L} \quad (4)$$

while power *not absorbed* by the load is represented by

$$P_r = v_r \bullet i_r = \frac{v_r^2}{R_0} \quad (5)$$

Here, the r subscript stands for reflected (not absorbed) power, voltage or current, respectively.

Applying Kirchoff's laws to point x in *Figure 5*, the current to the load is

$$i_L = i_x - i_r \quad (6)$$

and voltage across the load is

$$v_L = i_L R_L = v_x + v_r \quad (7)$$

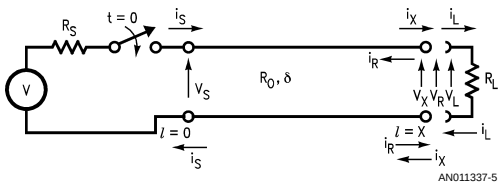


FIGURE 5. Boundary Conditions at the Line/Load Interface

To find the ratio of v_r to v_x so that it can be ascertained how much power is absorbed by the load, and how much is not absorbed (therefore, reflected), substitute $v_x/R_0$for i_x and v_r/R_0 for i_r into *Equation (6)*.

$$i_L = \frac{v_x}{R_0} - \frac{v_r}{R_0} \tag{8}$$

Rearranging *Equation (7)* and substituting for i_L in *Equation (8)* yields

$$\frac{v_x + v_r}{R_L} = \frac{v_x}{R_0} - \frac{v_r}{R_0} \tag{9}$$

The minus sign associated with v_r/R_0means, in this case, that the reflected voltage wave v_r travels in the −x direction toward the generator.

Collecting like terms of *Equation (9)* yields

$$v_x\left(\frac{1}{R_0} - \frac{1}{R_L}\right) = v_r\left(\frac{1}{R_0} - \frac{1}{R_L}\right) \tag{10}$$

So,

$$v_r = v_x \frac{\left(\frac{R_L - R_0}{R_0 R_L}\right)}{\left(\frac{R_L + R_0}{R_0 R_L}\right)} = v_x\left(\frac{R_L - R_0}{R_0 + R_L}\right) \tag{11}$$

and the desired relation for v_r/v_x is

$$\frac{v_r}{v_x} = \frac{R_L - R_0}{R_0 + R_L} \tag{12}$$

This ratio is defined as the voltage reflection coefficient of the load ρ_{VL}

$$\rho_{VL} \equiv \frac{v_r}{v_x} = \frac{R_L - R_0}{R_0 + R_L} \tag{13}$$

A similar derivation for currents shows

$$\rho_{IL} = -\frac{R_L - R_0}{R_L + R_0} = -\rho_{VL} \tag{14}$$

For the remainder of this application note and AN-808, the v or i subscript on the reflection coefficient is dropped, and ρ_L is assumed to be the *voltage* reflection coefficient of the load. Similarly, applying Kirchoff's laws to the source-line interface, the voltage reflection coefficient of the source is

$$\rho_S = \frac{R_S - R_0}{R_S + R_0} \tag{15}$$

The current reflection coefficient of the source has the same magnitude as ρ_S, but is opposite in algebraic sign.

When a traveling wave v_x, i_x meets a boundary such as the line load interface, a reflected wave is instantaneously generated so that Kirchoff's laws are satisfied at the boundary conditions. This is the direct result of the conservation of energy principle. Referring again to *Figure 5*, the effects of three different termination resistance R_L values are shown.

Case 1, $R_L = R_0$

In this case, R_L is equal to the characteristic resistance of the line. Using *Equation (13)*, the voltage reflection coefficient of the load ρ_L is

$$\rho_L = \frac{R_0 - R_0}{R_0 + R_0} = \frac{0}{2R_0} = 0 \tag{16}$$

Since $v_r/v_x = \rho_L$, then $v_r = \rho_L\, v_x = 0$ and no reflection is generated. This agrees with the discussion of cut lines and matched load where a line terminated in its characteristic impedance behaves the same as an infinite line. All power delivered by the line is absorbed into the load. The waveforms appear as shown in *Figure 6*. The wave starting at the source at time t = 0 is reproduced at point x down the line after a time delay of $t = x\delta = \tau$.

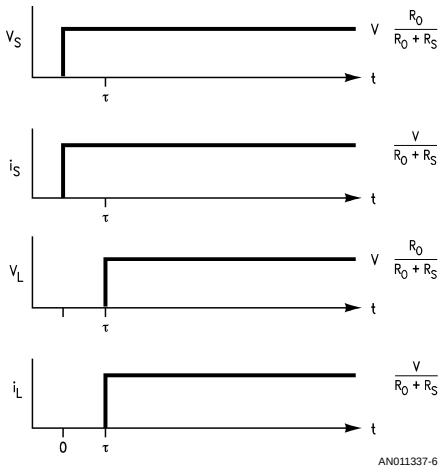


FIGURE 6. Waveforms for $R_L = R_0$

Case 2, $R_L > R_0$

To simplify this case, assume that $R_S = R_0$. This means that the initial voltage is

$$V\frac{R_0}{R_0 + R_0} = \frac{V}{2} \tag{17}$$

Also assume $R_L = 3\,R_0$, then the load voltage reflection coefficient is

$$\rho_L = \frac{3R_0 - R_0}{3R_0 + R_0} = +\frac{1}{2} \tag{18}$$

The voltage wave arriving at point x at time t = xδ generates a reflected voltage wave of magnitude

$$v_r = \rho_L v_x = \left(+\frac{1}{2}\right)\left(\frac{V}{2}\right) = \frac{V}{4} \tag{19}$$

and the load voltage is

$$v_L = v_x + v_r = \frac{V}{2} + \frac{V}{4} = \frac{3V}{4} \tag{20}$$

The reflected voltage wave v_r generated at t = xδ = τ travels back down the line toward the source arriving at the source at time t = 2xδ = 2τ. This wave will be absorbed without generating another reflection because R_S was picked to equal R_0, making ρ_S equal to zero. The source voltage is now

$$v_s + v_r = \frac{V}{2} + \frac{V}{4} = \frac{3V}{4} \tag{21}$$

and equilibrium is achieved.

If the circuit in *Figure 5* is analyzed using simple circuit theory and neglecting the transmission line effects, it is easily seen that

$$v_S = v_L = V\frac{R_L}{R_0 + R_L} = \frac{3V}{4} \tag{22}$$

This agrees exactly with *Equation (21)* and will always be the case. After all reflections cease and the circuit reaches equilibrium, the steady state voltages and currents on the line are the same as those produced using simple dc circuit analysis. Waveforms for $R_L > R_0$ (specifically $R_L = 3\ R_0$) appear in *Figure 7*.

In general, the case where $R_L > R_0$is viewed in the following manner. Because the line is capable of delivering more power than can be instantaneously absorbed by the load, the excess power is returned to the source and absorbed in the source resistor (assuming $R_S = R_0$).

An upper limit on the voltage reflection coefficient is found by allowing R_L to go to infinity. In this case, *Equation (13)* goes to +1.

Case 3, $R_L < R_0$

In this case, again set $R_S = R_0$and allow R_L to equal $R_0/3$. The initial wave, as before, is

$$v_S = V\frac{R_0}{R_0 + R_S} = \frac{V}{2} \tag{23}$$

and the load voltage reflection coefficient is

$$\rho_L = \frac{R_L - R_0}{R_L + R_0} = \frac{\frac{R_0}{3} - R_0}{\frac{R_0}{3} + R_0} = -\frac{1}{2} \tag{24}$$

Therefore, the reflected voltage wave v_r is

$$v_r = \rho_L\frac{V}{2} = -\frac{V}{4} \tag{25}$$

which starts propagating back toward the source at time t = τ. The load voltage at time t = τ is

$$v_x + v_r = \frac{V}{2} + -\frac{V}{4} = +\frac{V}{4} \tag{26}$$

The (−V/4) reflected wave arrives back at the source at time t = 2τ. Because R_S is set equal to R_0, ρ_S is, then, equal to zero and no reflected wave will be generated. The voltage at the source is now

$$v_S + v_r + \rho_S v_r = \frac{V}{2} + -\frac{V}{4} + 0 = \frac{V}{4} \tag{27}$$

From a dc circuit analysis, the steady state voltage is

$$V_{SS} = V\frac{R_L}{R_L + R_0} = \frac{V}{4} \tag{28}$$

This agrees with the result of *Equation (27)*. The waveforms for Case 3 ($R_L < R_0$) appear in *Figure 8*.

An interpretation of the actions occurring when load resistance is less than the characteristic line resistance is as follows: when power available at the line end is less than the power the load can absorb, a signal is sent back to the source saying, in essence, “send more power”.

It has been shown that a ratio of line and load resistance (ρ) can be used to calculate the voltages and currents in terms of a wave arriving at the boundary, possibly generating a reflected, reverse-traveling wave to satisfy the conservation of energy principle at the line-to-load boundary. This ratio is

$$V_{SS} = V\frac{R_L}{R_L + R_0} = \frac{V}{4} \tag{29}$$

where R_B represents the resistance into the boundary, R_B is R_S when considering the source-to-line interface and R_B would be R_L when considering the line-to-load interface. It is obvious that if discussing impedances, then $Z_S$would be substituted for R_S in *Equation (29)*, and there may be some phase angle between the voltage and current waves.

The forward traveling wave, v_x, plus the reflected wave, v_r, is equal to the load voltage (V_L). Since v_r is ρ_L v_x, this can be expressed as

$$v_x(1 + \rho_L) = v_L \tag{30}$$

This quantity (1 + ρ) can be defined as the voltage *transmission* coefficient of the load and it is known that

$$\frac{v_L}{v_x} = (1 + \rho_L) \tag{31}$$

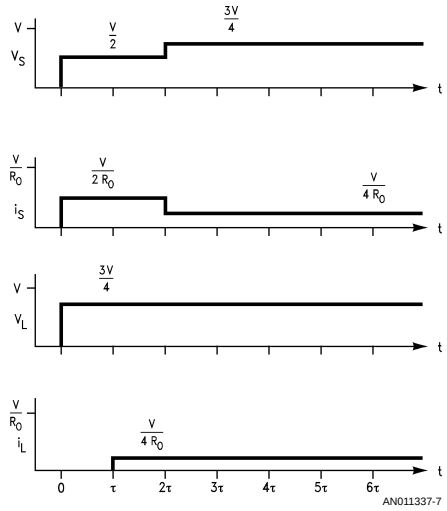
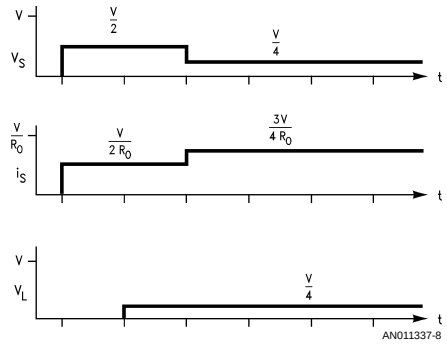


FIGURE 7. $R_S = R_0$, $R_L = 3R_0$



$$R_L = \frac{R_0}{3}$$

FIGURE 8.

The cases with various load resistances can be summarized.

	Condition		Circuit at time t = τ (one line delay time)
1.	$R_L = R_0$	$\rho_L = 0$	No reflection is produced — circuit reaches steady state immediately.
2.	$R_L > R_0$	$\rho_L > 0$	Positive voltage reflection — wave is sent back toward source. Voltage at load is higher than steady stage voltage (overshoot).
3.	$R_L < R_0$	$\rho_L < 0$	Negative voltage reflection — wave is sent back toward source. Voltage at load is lower than steady state voltage (undershoot).

FUNDAMENTAL PRINCIPLES

Before examining the algorithm for keeping track of reflections, there are two principles to keep in mind.

- Energy (as power) is conserved at boundary conditions (as explored previously)
- The principle of linear superposition applies. This means any arbitrary excitation function can be broken down into step functions, or ramps. The reaction of the circuit to each part can be analyzed, and the results can be added together when finished. This means that a positive pulse of duration t is examined by superimposing two step functions, one positive and one negative, starting after a delay of t (*Figure 9*). It also means the voltage at any point on the line is the sum of initial voltage plus the sum of all voltage waves that have arrived at or passed through the point up to and including the time of examination. Also, the current on the line is, at any point, the sum of initial current plus any forward or reverse traveling currents passing the point up to and including the time the current is examined.

It has also been established that the steady state solution for voltages and currents on the line can be found by simple dc circuit analysis.

In examining reflection effects for the remainder of this application note, the following conventions are used.

A voltage or current wave traveling *toward* the point of interest will have the subscript "i" for *incident* wave,

A voltage or current wave traveling *away* from the point of interest will have the subscript "r" for *reflected* wave,

The subscript "S" means the parameter applied to the *source* ($v_S$for the voltage at the source, etc.), and

The subscript "L" means the parameter applied to the *load* (v_L for the voltage at the load, etc.)

Sign conventions for voltage waves and their associated currents are shown in *Figure 10*.

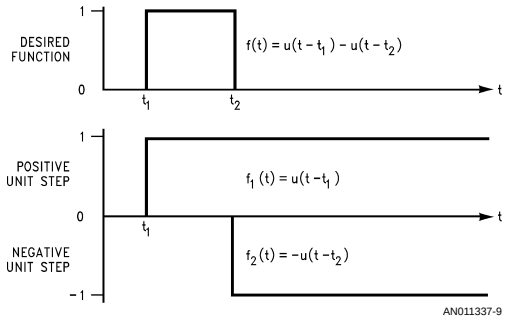


FIGURE 9. Superposition of Simple Waveforms to Form More Complex Excitations

TABULAR METHOD FOR REFLECTIONS — THE LATTICE DIAGRAM

The waves going up and down the line can be monitored by drawing a time scale, as a vertical line with time increasing in the down direction, to represent the location on the line under examination. Because voltages at the source and load ends of the transmission line are normally of primary interest, two time scales are necessary. Drawing arrows from one time scale to the other as in *Figure 10* shows the direction of travel of the waves during a specific time interval. Since the main concern is only with the waveforms at the line ends, time scales are ruled off in multiples of the time delay of the line τ. If a unit-step type wave is launched from the source at time t = 0+, it is known that the magnitude of the wave will persist unchanged until a wave arrives back from the load after a round trip delay time of two line delays. The source time scale then is incremented in multiples of 2 mτ where m = 0, 1, 2, 3,… Likewise, the first wave arrives at the load after a single time delay, so the first increment ruling on the load time scale is τ, or one time delay of the line. Because the subsequent waves arrive back at the load in increments of 2τ, the load time scale is ruled off in multiples of (2m + 1)τ where m = 0, 1, 2, 3,… The operation of the lattice diagram is discussed using the example in *Figure 11* which is the lattice diagram for the associated circuit.

time t = 0− (just before the switch closes)

The voltages at the source and load are equal with a magnitude of $v_{initial}$. Assume that no initial voltage is present. So, in this case, the voltage at the source and load equals zero.

$$V_{initial} = v_S(0-) = V_L(0-) = 0$$

time t = 0+ (just after the switch has closed)

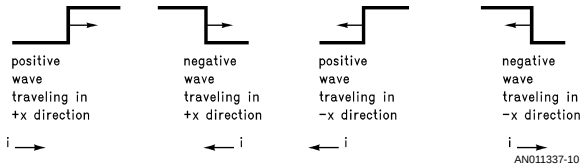
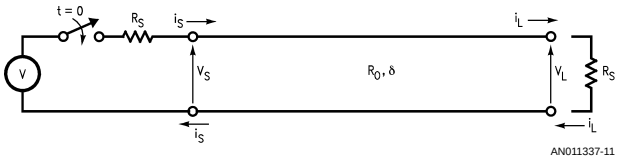
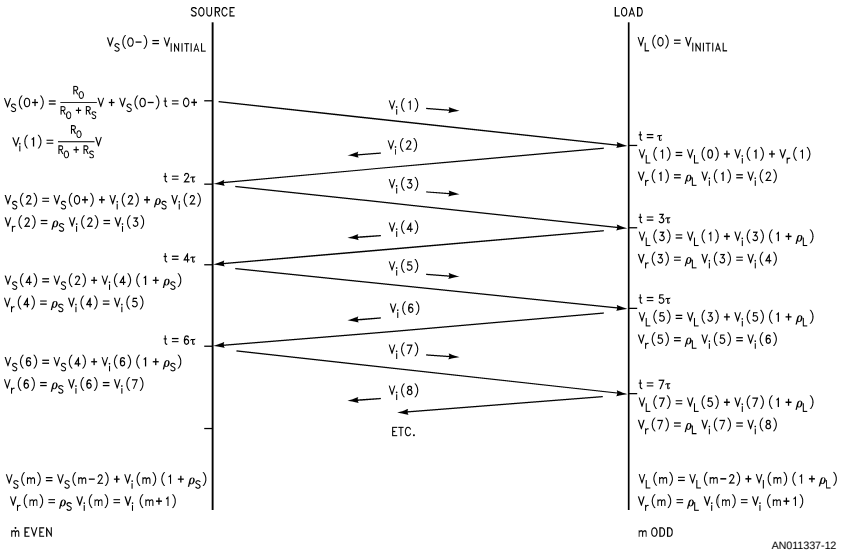


FIGURE 10. Sign Conventions for Waves



(a) Line Circuit to be Analyzed



(b) Lattice Diagram

FIGURE 11. Reflection Bookkeeping with the Lattice Diagram

The first wave $v_i(1)$ is launched at the source and begins to travel toward the load end of the line. As previously mentioned, a voltage divider action between R_S and R_0 is used to derive the magnitude of the initial voltage wave.

$$v_i(1) = V \frac{R_0}{R_0 + R_S}$$

At this time, the voltage at the source is the sum of the initial voltage plus the voltage wave $v_i(1)$ just generated.

$$v_S(0+) = v_S(0-) + v_i(1) = 0 + V \frac{R_0}{R_0 + R_S}$$

Because the switch closure represents a step function, the source voltage remains at this level until a wave returns after reflecting from the load at time $t = 2\tau$.

time $t = \tau$

The incident voltage wave $v_i(1)$ now arrives at the load and generates a reflected voltage wave

$$v_r(1) = \rho_L v_i(i); \rho_L = \frac{R_L - R_0}{R_L + R_0}$$

where ρ_L is the voltage reflection coefficient of the load. The reflected voltage wave $v_r(1)$ immediately starts traveling back toward the source becoming the incident voltage wave $v_i(2)$ which arrives back at the source at $t = 2\tau$. The voltage at the load is now the sum of the initial voltage plus the incident voltage wave $v_i(1)$ that just arrived plus the reflected voltage wave that is just departing.

$$\begin{aligned} v_L(1) &= v_L(0-) + v_i(1) + v_r(1) \\ &= 0 + v_i(1) + \rho_L v_i(1) \\ &= v_i(1)\,(1 + \rho_L) \end{aligned}$$

Again, because of the step function excitation, the load voltage remains unchanged until the new wave arrives at time $t = 3\tau$.

time $t = 2\tau$

$v_i(2)$ now arrives at the source and generates a reflected voltage wave $v_r(2)$ of magnitude

$$v_r(2) = \rho_S v_i(2); \rho_S = \frac{R_S - R_0}{R_S + R_0}$$

where ρ_S is the source voltage reflection coefficient.

The reflected voltage wave $v_r(2)$ starts back toward the load end of the line and becomes the incident voltage wave $v_i(3)$ arriving at the load at time $t = 3\tau$. The voltage at the source is now the sum of the voltage that was there plus the incident voltage wave just arrived plus the reflected voltage wave just departed for the load.

$$v_S(2) = v_S(0+) + v_i(2) + v_r(2)$$
$$= v\frac{R_0}{R_0 + R_S} + v_i(2) + \rho_S v_i(2)$$
$$= v\frac{R_0}{R_0 + R_S} + v_i(2)\,(1 + \rho_S)$$

time t = 3τ

$v_i(3)$ arrives at the load generating $v_r(3)$

$$v_r(3) = \rho_L v_i(3)$$

$v_r(3)$ departs back toward the source becoming $v_i(4)$ to the source. The load voltage is now

$$v_L(3) = v_L(1) + v_i(3)\,(1 + \rho_L)$$

time t = 4τ

When $v_i(4)$ arrives at the source and generates $v_r(4)$, then

$$v_r(4) = \rho_S v_i(4)$$

starts back toward the load to become $v_i(5)$ to the load. The load voltage is now

$$v_L(4) = v_L(2) + v_i(4)\,(1 + \rho_L)$$

This process can continue ad infinitum or until no measurable changes are detected. The reflection process at that time is considered complete and the line assumes a steady state condition. Steady state conditions can be found by applying simple dc circuit theory to source load circuits.

Summarizing this lattice diagram method, any time t = mτ and m > 1, the following relationships exist:

If m is odd, the $v_i(m)$ wave is arriving at the load and generates a reflected wave

$$v_r(m) = \rho_L v_i(m)$$

This becomes $v_i(m + 1)$ as it starts toward the source. The voltage at the load at time t = mτ will be

$$v_L(m) = v_L(m - 2) + v_i(m)\,(1 + \rho_L)$$

This is the sum of the voltage that was there before the wave arrived, i.e., $v_L(m - 2)$, plus the wave arriving $v_i(m)$ and the reflected wave $v_r(m)$ departing.

If m is even, the $v_i(m)$ wave is arriving at the source and generates a reflected wave

$$v_r(m) = \rho_S v_i(m)$$

This becomes $v_i(m + 1)$ as it starts toward the load. The voltage at the source is now

$$v_S(m) = v_S(m - 2) + v_i(m)\,(1 + \rho_S)$$

This is the sum of the voltage that was present $v_S(m - 2)$ plus the incident wave arriving $v_i(m)$ plus the reflected wave departing $v_r(m)$.

The voltage and current at the source end of the line for a lossless line can be expressed as a summation.

$$v_S(t) = \frac{R_0}{R_S + R_0} \bullet \left[e(t)u(t) + \left(1 + \frac{1}{\rho_S}\right)\sum_{n=1}^{\infty} \rho_S{}^n\,\rho_L{}^n e(t - 2n\tau)u(t - 2n\tau)\right] \quad (32)$$

$$i_S(t) = \frac{1}{R_S + R_0} \bullet \left[e(t)u(t) + \left(1 - \frac{1}{\rho_S}\right)\sum_{n=1}^{\infty} \rho_S{}^n\,\rho_L{}^n e(t - 2n\tau)u(t - 2n\tau)\right] \quad (33)$$

where e(t) is the generator voltage as a function of time, and u(t) is the unit step function.

Likewise, the load voltage and load current for the lossless line can be expressed as a summation.

$$v_L(t) = \frac{R_0}{R_S + R_0} \bullet (1 + \rho_L)\left[\sum_{n=0}^{\infty} \rho_S{}^n\rho_L{}^n e(t-(2n + 1)\tau)u(t-(2n + 1)\tau)\right] \quad (34)$$

$$i_L(t) = \frac{1}{R_S + R_0} \bullet (1 - \rho_L)\left[\sum_{n=0}^{\infty} \rho_S{}^n\rho_L{}^n e(t-(2n + 1)\tau)u(t-(2n + 1)\tau)\right] \quad (35)$$

A similar expression of summation can be developed for the voltage (or current) at any point along the line at any time.

Because the lattice diagram is tabular in method, a computer program can be written relieving the designer of bookkeeping and repetitive calculations. A BASIC computer program for lattice diagrams appears in *Figure 12*.

LIMITATIONS OF THE LATTICE DIAGRAM METHOD

Before using the lattice diagram to explore reflection effects with various source and load characteristics, it is necessary to pause at this point and examine the models used by the lattice diagram.

First, both the line driver and receiver are simulated either by a constant input or output resistance. The source has two voltage sources and a switch representing the internal source voltage at a time less than zero and equal to (or greater than) zero. The receiver is represented by a single resistor shunting the line end opposite the driver site. The line itself is represented by its characteristic resistance R_0 and its total one-way time delay (τ). This is equal to length times propagation delay per unit length. This model is shown in *Figure 12*.

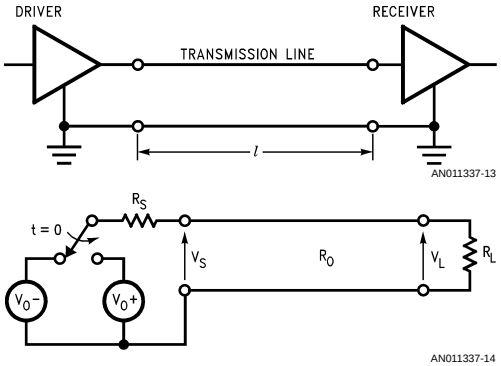


FIGURE 12. Model Used for Lattice Diagram Method

Because most data communication circuits are voltage types, that is, the receiver senses the line voltage to decide if a logic One or logic Zero is present, the primary interest is in voltages at the source and load as a function of time. Major exceptions include the current loops used in teletypewriters, telegraphs, and burglar alarm systems. The majority of data communications circuits used in computers, peripherals, and general controllers are voltage types.

The lattice diagram method cannot easily use source or receiver current/voltage relationships that are non-linear; i.e., not purely resistive. For non-linear current/voltage characteristics such as found in diodes, a graphic method can be used called the reflection diagram or the Bergeron method.

Note: A French hydraulic engineer, L.J.B. Bergeron developed the method to study the propagation of water hammer effects in hydraulics. See references, AN-806.

Signals exchanged using lattice diagrams are of the unit step variety. When ramps or more complex waves are exchanged, the complexity of the bookkeeping increases dramatically. Additionally, the lines are presumed to be lossless, although a constant line attenuation factor could be accommodated without excessive bookkeeping. These limitations should be kept in mind when examining various source and load resistance combinations and their reflection characteristics.

There are three classes of source resistance, $R_S < R_0$, $R_S = R_0$ and $R_S > R_0$. There are also three classes of load resistance, $R_L < R_0$, $R_L = R_0$ and $R_L > R_0$. This gives nine types of single driver, single receiver line circuits. Each circuit will be examined in turn to determine reflection effects for these combinations with evaluations of each combination for voltage type communications.

REFLECTION EFFECTS FOR VOLTAGE SOURCE DRIVERS

Initial waves launched by a voltage source type driver ($R_S < R_0$) are greater than one-half the magnitude of the internal voltage source. Referring to *Figure 12*, the initial voltage wave is derived as follows.

$$v_i(1) = (V_{0+} - V_{0-}) \bullet \frac{R_0}{R_0 + R_S} \tag{36}$$

while the voltage at the source at t = 0+ is

$$v_S(0+) = v_S(0-) + v_i(1) = V_{0-} \bullet \frac{R_L}{R_L + R_S} + v_i(1) \tag{37}$$

If the receiver switching point is at the mean of the driver voltage swing, the initial wave always has sufficient magnitude to indicate the correct logic state as it passes the receiver site. This maximizes the noise margins of the receiver.

Since $R_S < R_0$, the source voltage reflection coefficient ρ_S is less than zero. Any voltage waves, then, arriving back at the source are changed in sign, reduced in amplitude (assuming $R_S > 0\Omega$), and sent back toward the load. If the load resistance equals the characteristic line resistance ($R_L = R_0$), the voltage reflection coefficient of the load is

$$\rho_L = \frac{R_L - R_0}{R_L + R_0} = \frac{0}{2R_0} = 0$$

No reflections, therefore, are generated at the load. The voltage wave produced at the source is reproduced at the load after a time delay of $\tau = \ell\delta$, and the line assumes a steady state condition. *Figure 16* illustrates the source and load voltage waveforms for this case.

If R_L is greater than R_0, ρ_L is positive. Waves arriving at the load generate the same polarity reflections as the arriving waves. ρ_S and ρ_L are of opposite signs, so a dampened oscillatory behavior of the load voltage is expected. The oscillation period or *ringing* is 4τ. The overshoot of v_L from $t = \tau$ to 3τ may cause breakdown of the input circuitry of a receiver, depending on the receiver voltage rating. The undershoot at $t = 3\tau$ or 5τ can reduce the noise immunity of a receiver or even cause a logic level misinterpretation — an error in the data. These waveforms are shown in *Figure 16*.

If R_L is less than R_0, then ρ_L is negative and a wave arriving at the load generates a reflection opposite in polarity to the incident wave. This causes the voltage at the source to overshoot steady state voltage at t = 0. Each reflection returning from the load causes the source voltage to continually step down toward the steady state voltage V_{SS}. These steps last for 2τ, or one round trip delay. Load voltage starts an increasing step-up waveform towards V_{SS} at time $t = \tau$, with steps again taking one round trip delay, 2τ. A line receiver placed in the middle of the line sees an entirely different waveform — dampened oscillations much like the load voltage in *Figure 16*. This is caused by the negative signs of both source and load voltage reflection coefficients. Each time an incident wave arrives at either source or load, the reflected wave generated at that time has a sign opposite to the sign of the incident voltage wave. The voltage at a distance half way down the line is composed of these forward and reverse traveling waves arriving at that point commencing at time $t = 0.5\tau$, and with each new wave passing that point after one line delay (τ). These waveforms are shown in *Figure 16*.

The optimum load resistance for voltage signal communications on transmission lines driven by a low impedance source ($R_S < R_0$) is equal to the characteristic line resistance. Large signal line voltages are produced and there are no reflection effects complicating the waveforms *Figure 14*.

However, a matched load ($R_L = R_0$) is a dc load on the driver, thus it increases system power dissipation. But, it does preserve signal fidelity and amplitude allowing use of multiple bridging receivers ($R_{in} \gg R_0$) along the line.

The unterminated case ($R_L > R_0$) reduces dc driver loading and also reduces system power dissipation over the matched load case. The unterminated case does, however, allow the load signal to exhibit pronounced overshoot and undershoot around the steady state voltage. If the load signal undershoot places the receiver in its threshold uncertainty region, data errors result. There is a way to "civilize" the voltage waveform of the unterminated line load by trading off signal rise time versus line time delay. This is discussed later.

The final case of $R_S < R_0$ and $R_L < R_0$ is not generally useful in terms of voltage signals produced (*Figure 16*). Systems using this case consume more power than the previous two cases and have no particular advantage for voltage mode communications.

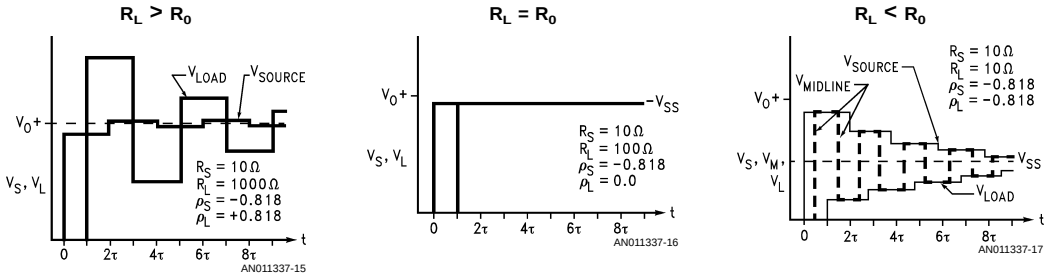


FIGURE 13. $R_S < R_0$

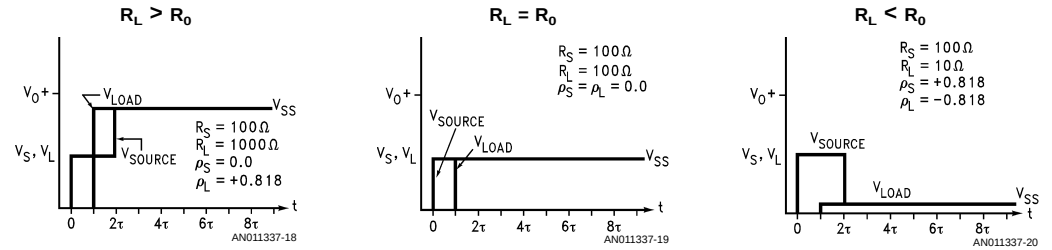


FIGURE 14. $R_S = R_0$

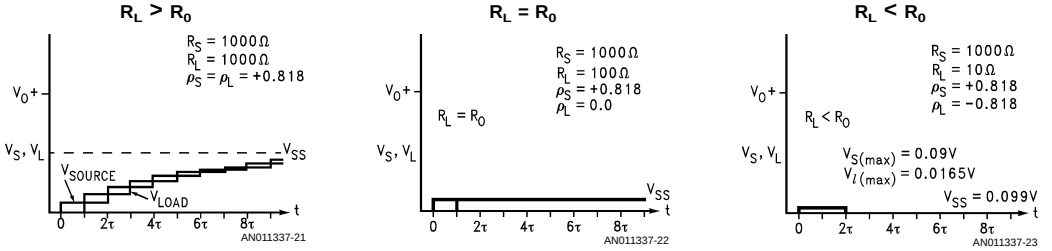


FIGURE 15. $R_S > R_0$

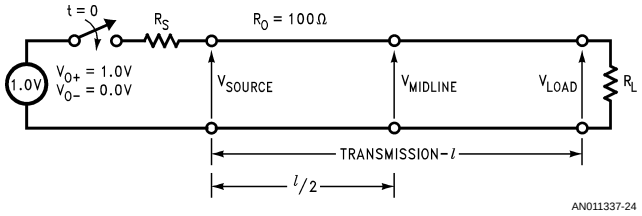


FIGURE 16. Source and Load Voltage Waveforms for Various R_S and R_L

REFLECTION EFFECTS FOR MATCHED-SOURCE DRIVERS

In all three cases under discussion here, the initial voltage produced by the driver onto the line is

$$v_i(1) = (V_{0+} - V_{0-}) \frac{R_0}{R_0 + R_S} = \frac{1}{2}(V_{0+} + V_{0-}) \quad (38)$$

since $R_S = R_0$. The voltage at the source at time t = 0+ is

$$v_S(0+) = v_S(0-) + v_i(1) = V_{0-} \bullet \frac{R_L}{R_L + R_S} + v_i(1) \quad (39)$$

Assume, for clarity, that initial voltage (V_{0-}) is zero, thus *Equation (39)* simplifies to

$$v_S(0+) = \frac{V_{0+}}{2} \quad (40)$$

Since $R_S = R_0$, $\rho_S$is equal to zero. This means that load-generated reflections due to load mismatch are absorbed at the source when, at time $t = 2\tau$, the reflected wave arrives back at the source. The line then assumes a steady state throughout. This back match or series termination effect of a matched source allows a wide latitude in choice of load resistance without sacrificing the signal fidelity of the load voltage waveform.

If the load resistance equals the characteristic line resistance $R_L = R_0$, then ρ_L equals zero and no load site reflections are generated. The initial voltage wave arrives at the load at time $t = \tau$ (one line delay) and voltages (and currents) on the line immediately assume steady state conditions (see *Figure 16*). The optimum receiver threshold here is one-half the steady state voltage or $V_{0+}/4$. The main advantage over the voltage source type driver with matched load case ($R_S < R_0$, $R_L = R_0$) is that $R_S$and R_L resistance tolerances may be relaxed without incurring much signal *ringing*. This effect is due primarily to the termination provided by both line ends, rather than just one line end. Any reflected voltage wave on either system is attenuated by the product of ρ_S and ρ_L for each round trip line delay time. Since the $\rho_S\rho_L$ product for the fully matched case is smaller than the $\rho_S\rho_L$product for the single matched case, the reflections are attenuated and die out in fewer round trips. For example, if 20% tolerance resistors are used in both cases, ρ_S and ρ_L values for the fully matched case become 0.0 ±0.0909, which is a $\rho_S\rho_L$ product of ±0.0033. This means that after one round trip (2τ), the reflection amplitude starting back toward the load would be less than 0.33% of the initial wave.

Using $R_S = 10\Omega$, $R_L = 100\Omega$, and $R_0 = 100\Omega$ as for *Figure 16*, shows the same 20% tolerances applied to the single matched case

$$-0.8519 \le \rho_S \le -0.7857$$

$$-0.0909 \le \rho_L \le +0.0909$$

and

$$|\rho_S \le \rho_L| \le 0.0909$$

The voltage reflection amplitude after one round trip is a maximum of 7.7% of the initial wave.

The choice between using the single and fully matched system should be carefully considered because the fully matched system does sacrifice signal voltage magnitude to get a decreased dependence on absolute resistor values.

If the load resistance for a matched driver circuit is made much greater than the line resistance, the initial wave arriving at the load at time $t = \tau$ will be almost double since ρ_L will be close to +1.0. Because source resistance is set equal to line resistance, ρ_S becomes zero, the reflected voltage wave from the load is absorbed by the source at time $t = 2\tau$, and steady state conditions prevail. Waveforms for this case are shown in *Figure 16*. This is called *back matching* or *series termination*.

The main advantage of series termination is a great reduction in steady state power consumption when compared with the parallel terminated case ($R_S \ll R_0$, $R_L = R_0$). At the same time, series termination provides the same signal fidelity to a receiver placed at the line end. Compare the load voltage waveforms for the two cases in and *Figure 16*. The main disadvantage to series termination is that receivers placed along the line see a waveform similar to that shown for the source in *Figure 16*. That is, receivers along the line see the $V_{0+}/2$ initial wave as it passes that point on the line, and do not see a full signal swing until the load end reflection passes that point. Consequently, receivers along the line do not see a signal sufficient to produce the valid logic state output until the load reflection returns. Depending on actual line length and receiver characteristics, the receiver may even oscillate, having been placed in its linear operation region. With the benefit, then, of reducing system power, the series termination method has a constraint of allowing only one line receiver located at the line load end. The parallel termination method should be used if other receivers along the line are required.

The final case of matched source drivers is with the use of a load resistance less than the characteristic line resistance. The waveforms for this case are shown in *Figure 16*. A line receiver with a threshold of $V_0/4$ placed at the source responds like a positive, edge triggered one-shot and produces a pulse in response to a +V/2 initial wave of 2τ duration. Aside from its use as a one-shot, this circuit doesn't seem to offer any advantages for voltage mode communications.

REFLECTION EFFECTS FOR CURRENT-SOURCE DRIVERS

The name *current source drivers* is somewhat of a misnomer, and might be more properly called *current-limited voltage source drivers*. True *current source* drivers such as the DS75110A are normally used in conjunction with parallel termination resistors to create a matched source.

The *current source* drivers ($R_S > R_0$) discussed resemble true current sources in the respect that their output resistance is usually much greater than the characteristic line resistance. The initial voltage step produced on the line is thus usually small $v_i(1) = (i_S(1)R_0)$. This is due to the voltage divider action of the driver source resistance and the characteristic line resistance.

Voltage waveforms for a current source type driver either step up to V_{SS}, reach steady state after 2τ, or execute a dampened oscillation around V_{SS}, depending on whether the load resistance R_L is greater, equal, or less than R_0, respectively. The second case $R_L = R_0$ provides signals much the same as the other two cases where $R_L = R_0$, that is, the source voltage steps immediately to V_{SS}, with the load voltage following after one line time delay. Here the amplitude of the signal is much smaller than previous matched load cases. Since the current source type drivers (DS75110A) have high off-state impedances, they allow multiple drivers on the line to produce data bus or party line. Waveforms for the matched load case are shown in *Figure 16*.

The case $R_L < R_0$ really provides no useful advantage for voltage mode communications. The negative sign for ρ_L and the positive sign for ρ_S lead to dampened oscillatory behavior, or ringing. The maximum perturbation takes place at the source end of the line. Waveforms for this case are similar to those shown in *Figure 16*, and are shown to scale in *Figure 16*. With the given values used to produce the figure, the maximum amplitude ringing appears at the source line end.

The $R_L > R_0$ case is of interest because it is representative of DTL driving a transmission line with the output going from LOW to HIGH. DTL has a high value R_S, (2 kΩ or 6 kΩ) in the HIGH logic state. Since both R_S and R_L are greater than R_0, both ρ_S and ρ_L are positive. A small voltage step starts from the source at t = 0+; its magnitude is

$$v_i(1) = V\frac{R_0}{R_0 + R_S}$$

Note: Since the input diode is not represented, the representation of DTL input as a single resistor to ground is not strictly correct. For purposes of approximation, this simple representation is used. Treatment of non-linear current/voltage sources and loads is covered by Metzger & Vabre. (op. cit.)

Upon arrival at the load at time $t = \tau$, this initial wave generates a positive voltage reflection since $\rho_L > 0$. The voltage reflection arrives back at the source site at time $t = 2\tau$. Since ρ_S is also positive, another positive voltage reflection is launched back toward the load. The process repeats, and the source and load voltages both execute a step-up approach toward steady state voltage V_{SS}. These waveforms are shown in *Figure 16*.

In examining voltage at the line midpoint ($x = \ell/2$), a step-up type waveform is seen which is the sum of all the incident voltage waves passing the line midpoint up to the time of examination. The midpoint voltage is expressed as follows.

$$v_m(t) = V_{SS}(1 - \exp[-(t + 0.5\tau)/T]) \quad (41)$$

Note: This equation is presented without derivation, but a procedure similar to that used by Matick (Ref. 2, AN-806) can be used.

for $t = n + 0.5\tau$ with n = 0, 1, 2, 3, etc. V_{SS} in *Equation (41)* is the steady state line voltage

$$V_{SS} = V_{0+} \bullet \frac{R_L}{R_S + R_L}$$

and T is a time constant given by

$$T = -\frac{2\tau}{\ell\, n(\rho_S \rho_L)} \quad (42)$$

with τ being one line delay ($\tau = \ell\delta$).

Note: This equation is presented without derivation, but a procedure similar to that used by Matick (Ref. 2, AN-806) can be used.

Equation (41) provides an exact solution for odd multiples of n (n = 1, 3, 5…, so $t = 1.5\tau, 3.5\tau, 5.5\tau$…), while it approximates $v_m(t)$ for even multiples of n (n = 0, 2, 4…, so $t = 0.5\tau$, 2.5τ, 4.5τ…). The closer the $\rho_S\rho_L$ product is to 1, the better *Equation (41)* predicts $v_m(t)$, particularly for even multiples of n. To illustrate the fitting, *Table 1* and *Table 2* are generated by the BASIC language computer program *Table 3* and their data is plotted in *Figure 18*.

Designers familiar with DTL circuits should quickly recognize that the waveforms shown in *Figure 18* are very similar to the rising edge waveforms found when a DTL gate output goes from the LOW to HIGH state. This characteristic waveform has usually been attributed to the series RC circuit (a gate output resistance driving a lumped transmission line capacitance). The time constant for this approach, based on the C(dv/dt) = i rule from simple circuit theory, provides only an approximation. The actual cause of the waveform shape, however, is due to reflection effects. Unfortunately, the only way to speed up the rising edge is to reduce source resistance, (providing an initial step greater than the receiving threshold) and terminate the line to eliminate the load reflections.

DTL inability to drive transmission lines at high repetition rates is the direct result of the signal rise time limitation caused by positive reflection coefficients for both the source and load. A transmitted positive pulse may be missed if its duration is less than the time required for the load signal to reach the receiver threshold.

The $R_S > R_o$ and $R_L > R_o$ case provides no definite advantages as voltage mode communication is concerned. This case, in fact, poses a definite hazard to high speed data communications because the reflections cause, in effect, a slow, exponential signal transition. Because line delay is a factor, longer lines will only increase the effect.

TABLE 1. (R_S = 2000Ω, R_0 = 100Ω, R_L = 4000Ω)

RHOS = 0.904762 RHOL = 0.951220
TAU = −13.3250 V1(1) = 4.76190H-C2
V_{SS} = 0.666667

TIME	VM(T)	VAPPX	%DIFF
0.5	0.04762	0.04820	+1.220%
1.5	0.09292	0.09292	+0.000%
2.5	0.13390	0.13440	+0.373%
3.5	0.17288	0.17288	+0.000%
4.5	0.20815	0.20858	+0.207%
5.5	0.24170	0.24170	+0.000%
6.5	0.27206	0.27243	+0.136%
7.5	0.30093	0.30093	+0.000%
8.5	0.32705	0.32737	+0.097%
9.5	0.35190	0.35190	+0.000%
10.5	0.37439	0.37466	+0.073%
11.5	0.39577	0.39577	+0.000%
12.5	0.41512	0.41536	+0.057%
13.5	0.43353	0.43353	+0.000%
14.5	0.45018	0.45038	+0.045%
15.5	0.46602	0.46602	+0.000%
16.5	0.48035	0.48053	+0.036%
17.5	0.49399	0.49399	+0.000%
18.5	0.50632	0.50647	+0.030%
19.5	0.51805	0.51805	+0.000%
20.5	0.52867	0.52880	+0.024%
21.5	0.53877	0.53877	+0.000%

TABLE 2. (R_S = 500Ω, R_0 = 75Ω, R_L = 10 kΩ)

RHOS = 0.739130 RHOL = 0.985112
TAU = −6.30356 V1(1) = 1.30435
V_{SS} = 0.952381

TIME	VM(T)	VAPPX	%DIFF
0.5	0.13043	0.13971	+7.112%
1.5	0.25893	0.25893	+0.000%
2.5	0.35390	0.36066	+1.909%
3.5	0.44746	0.44746	+0.000%
4.5	0.51661	0.52153	+0.952%
5.5	0.58473	0.58473	+0.000%
6.5	0.63509	0.63867	+0.564%
7.5	0.68469	0.68469	+0.000%
8.5	0.72135	0.72396	+0.361%
9.5	0.75747	0.75747	+0.000%
10.5	0.78416	0.78606	+0.242%
11.5	0.81046	0.81046	+0.000%
12.5	0.82990	0.83128	+0.167%
13.5	0.84904	0.84904	+0.000%
14.5	0.86320	0.86420	+0.117%
15.5	0.87714	0.87714	+0.000%
16.5	0.88744	0.88818	+0.083%
17.5	0.89759	0.89759	+0.000%
18.5	0.90510	0.90563	+0.059%
19.5	0.91249	0.91249	+0.000%
20.5	0.91795	0.91834	+0.042%
21.5	0.92334	0.92334	+0.000%

TABLE 3. BASIC Program Listing

```
100   PRINT'ENTER RS, R0, RL'1
110   INPUT R1, R0, R2
120   P1=(R1-R0)/R1+R0)
130   P2=(R2-R0)/R2+R0)
140   V1=R0/R1+R0)
150   K1=2./LOG(P1*P2)
160   V9=R2/(R1+R2)
170   PRINT'RHOS='; P1;'RHOL=';PS;'TAU=';K1
180   PRINT 'V1(1)=';V1;'VSS=';V9
190   V=V1
200   PRINT'TIME VM(T) VAPPX
      DIFF'
210   FOR T=0.5 TO 20.5 STEP 2.
220   V2=V9*(1.-EXP((T+.5)/KL))
230   P=100.*(V2-V)/V
240   PRINT USING 250,T,V,V2,P
250   :##.# -#.##### -#.##### +###.###

260   V1=V1*P2
270   V=V+V1
280   REM SOURCE END
290   V2=V9*(1.-EXP( (T+1.5)/k1 ) )
300   P=100.*(V2-V)/V
310   PRINT USING 250,T+1.,V,V2,P
320   V1=P1*V1
330   V=V+V1
340   NEXT T
350   PRINT
360   PRINT
370   PRINT
380   GOTO 100
390   END
```

FIGURE 17. Comparison of v_m Formula to Computed Midline Voltage

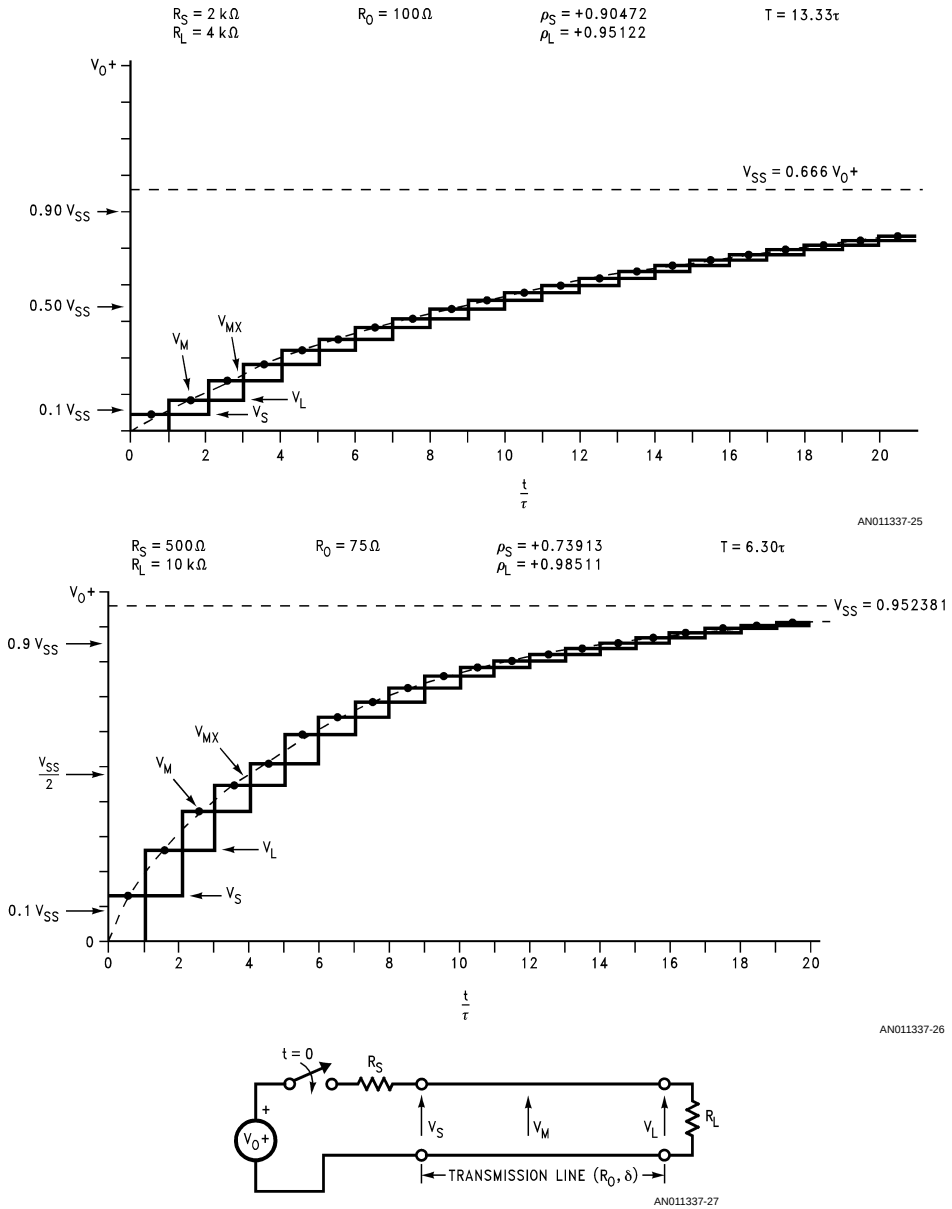


FIGURE 18. Approximation of Midline Voltage with $R_S > R_0$ and $R_L > R_0$

$$v_{MX}(t) = V_{SS}\left(1 - \exp[-(t + 0.5\tau)/T]\right)$$

$$t = \frac{-2\tau}{\ell n\,(\rho_S\,\rho_L)}$$

SUMMARY — Which are the Advantageous Combinations?

In examining the basic combinations of source, line and load resistances, and typical waveforms characteristic of each case, advantageous combinations can be determined. The primary results are tabulated in *Figure 19*. those combinations generally used in voltage mode communications circuits are as follows.

1. Unterminated case ($R_S \ll R_0$, $R_L \gg R_0$). This situation provides low steady state power dissipation and large signal levels, but also shows pronounced “ringing” effects. The “ringing” can be reduced by controlling signal rise/fall time versus τ, or by clamping diodes to limit load signal excursions. This case is representative of TTL circuits and is thus widely employed.

2. The parallel terminated case ($R_S \ll R_0$, $R_L = R_0$) provides large signal levels, and excellent signal fidelity. However, it is power consuming with most of that power dissipated in the load resistor. This case is useful for cleaning up the reflection effects of Case 1 but, at the same time, does require a driver circuit to have its internal current limits set at greater values than those required to produce the desired signal level into the minimum line resistance used. Thus, this case requires specific line driver devices such as the DS75114/ DS9614. Ordinary TTL, except for the above mentioned circuits, has too low a current limit point to adequately drive 50Ω lines.
3. The series terminated or backmatched driver case $R_S = R_0$, $R_L \gg R_0$ provides a low steady state power dissipation system for use with one receiver located at the load end of the line. The positive reflection coefficient of the load is used to approximately double the initial wave arriving at the load. Setting $R_S = R_0$ terminates the reflected wave when it arrives back at the source site after two line delays, and the line then assumes steady state conditions. The use of other receivers located along the line is not recommended, because they will not see the full driver signal swing until the reflection from the load passes their particular bridging points Such receivers could malfunction, as they would see a voltage very close to their threshold, and perhaps even place the line receiver in its linear operating region. This could make the line receiver sensitive to oscillatory, parasitic feedback. If these constraints are acceptable, the series termination method can be used to good advantage in providing the same signal fidelity and signal amplitude as with the parallel termination method, while at the same time, contributing a significant savings in steady state power consumption.
4. The fully matched case $R_S = R_0$, $R_L = R_0$ not only provides excellent signal fidelity all along the line, but also has reduced signal amplitude over that of the parallel terminated case. Additionally, the power consumption is somewhat less than the parallel termination case and the power is divided equally by the source and load. The primary advantage of the fully matched system is that termination resistor tolerances can be relaxed somewhat without incurring large amounts of ringing. This is because both the source and load act as line terminations.

Configuration Name (if any)	(Driver) Source Resistance	(Receiver) Load Resistance	Signal Characteristics	Optimum Receiver Threshold	Line Receivers Allowed at Other Than Load End of Line?	Comments
Unterminated	$\ll R_0$	$\gg R_0$	Ringing Pronounced	0.5 V_{SS}	Yes	Undershoot May Cause Errors
Parallel Terminated	$\ll R_0$	$= R_0$	Excellent Fidelity	0.5 V_{SS}	Yes	Load Resistor Consumes Power $P_L = \frac{(V_{SS})^2}{R_L}$
	$\ll R_0$	$\ll R_0$	Awful — Different Signals at Each Point on the Line	NA	No	Not Generally Useful
Series Terminated or Backmatched Driver	$= R_0$	$\gg R_0$	Load Signal Excellent	0.5 V_{SS}	No	Reduced Power Consumption Over Parallel Termination
Fully Matched	$= R_0$	$= R_0$	Excellent Fidelity	0.25 V_{SS}	Yes	Greater Tolerances on Resistors Allowed for Same Fidelity as Parallel Termination
	$= R_0$	$< R_0$	Load Signal Like a One-Shot	NA	NA	Not Generally Useful for Data, is Useful as Pulse Generator
	$\gg R_0$	$\gg R_0$	Exponential Like Signal Waveforms	0.5 V_{SS}	Yes	Low Power Consumption. Increased Delay due to Signal "Rise" Times.
	$\gg R_0$	$= R_0$	Small Signal Amplitude and Excellent Fidelity	0.5 V_{SS}	Yes	Produces Only Small Signal Voltages Compared with Other Methods. Uses Current Sinking Drivers such as the 75110A.
	$\gg R_0$	$< R_0$	Very Small Signal Amplitudes, also Ringing	NA	NA	Not Generally Useful

FIGURE 19. Summary of Effects

EFFECT OF SOURCE RISE TIME ON WAVEFORMS

Previously, it was assumed that the source-produced signal rise time was always much less than the line time delay (τ). Because the waveforms for the source and load voltage were the superposition of incident and reflected waves occurring at their proper times, and because the shape of each wave was a square edged step function, the resultant source and load waveforms were thus also square edged, or *ideal* in nature. In many practical cases, particularly when line length is short, the source excitation possesses a finite, and non-negligible, rise time. Therefore, depending on the ratio of rise time to line delay, it is possible to have a new wave start arriving at the point of interest *before* the previous wave can reach its final value. The net waveform for voltage or current at that point, then, would consist of the superposition of two or more waves during their time of overlap. To study the superposition effect on signal waveforms, the source excitation is represented as a simple linear ramp rise to its final value of V_{o+}, so

$e(t) = 0$ for $t < 0$

$e(t) = V_{o+} \cdot t/t_r$ for $0 \le t \le t_r$

$e(t) = V_{o+}$ for $t > t_r$

and where t_r represents the 0-to-100% source rise time. The circuit model and its lattice diagram are shown in *Figure 20*. The values of R_S, R_0 and R_L were chosen to equal those of

an actual circuit on hand, allowing the theoretical waveforms, obtained by graphical superposition, to be compared with the measured response of an actual circuit.

Figure 21 shows the load voltage v_L, source voltage v_S and source current i_S waveforms versus time for a circuit with a source rise time very much less than τ. The actual waveforms for v_L, v_S and i_S are composed of the superposition of both incident and reflected waves in their proper time sequence. In the figures, these waves are shown as dotted lines. Each wave represents the sum of the incident wave plus its reflection. The resultant v_L, v_S and i_S waveforms (shown as solid lines) are the superposition of the waves represented by the dotted lines. With the exception of a slight rounding of the edges, the actual waveforms for the circuit, shown in the oscilloscope photograph in *Figure 21*, closely approximate the waveforms predicted by theory.

Source					**Load**				
t in (τ)	**$v_i + v_r$ (V)**	**$i_i + i_r$ (mA)**	**v_S (V)**	**i_S (mA)**	**t in (τ)**	**$v_i + v_r$ (V)**	**$i_i + i_r$ (mA)**	**v_L (V)**	**i_L (mA)**
0	0.9400	12.53	0.9400	12.53	1	1.8500	0.40	1.8500	0.40
2	0.1224	−22.64	1.0624	−10.10	3	−1.5500	−0.34	0.3000	0.06
4	−0.1026	18.97	0.9599	8.87	5	1.2986	0.28	1.5986	0.35
6	0.0859	−15.90	1.0458	−7.03	7	− 1.0881	−0.24	0.5106	0.11
8	−0.0720	13.32	0.9738	6.29	9	0.9116	0.20	1.4222	0.31
10	0.0603	−11.17	1.0341	−4.87	11	−0.7638	−0.17	0.6584	0.14
12	−0.0505	9.36	0.9836	4.48	13	0.6399	0.14	1.2983	0.28
14	0.0424	−7.84	1.0259	−3.36	15	−0.5362	−0.12	0.7622	0.16
16	0.0355	6.57	0.9904	3.21	17	0.4492	0.10	1.2114	0.26

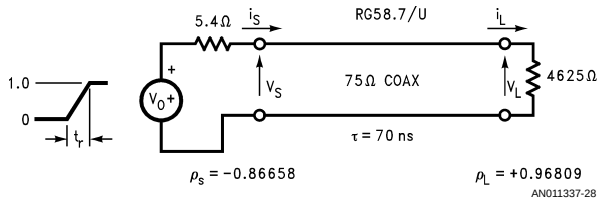


FIGURE 20. Transmission Line Model and Its Lattice Diagram

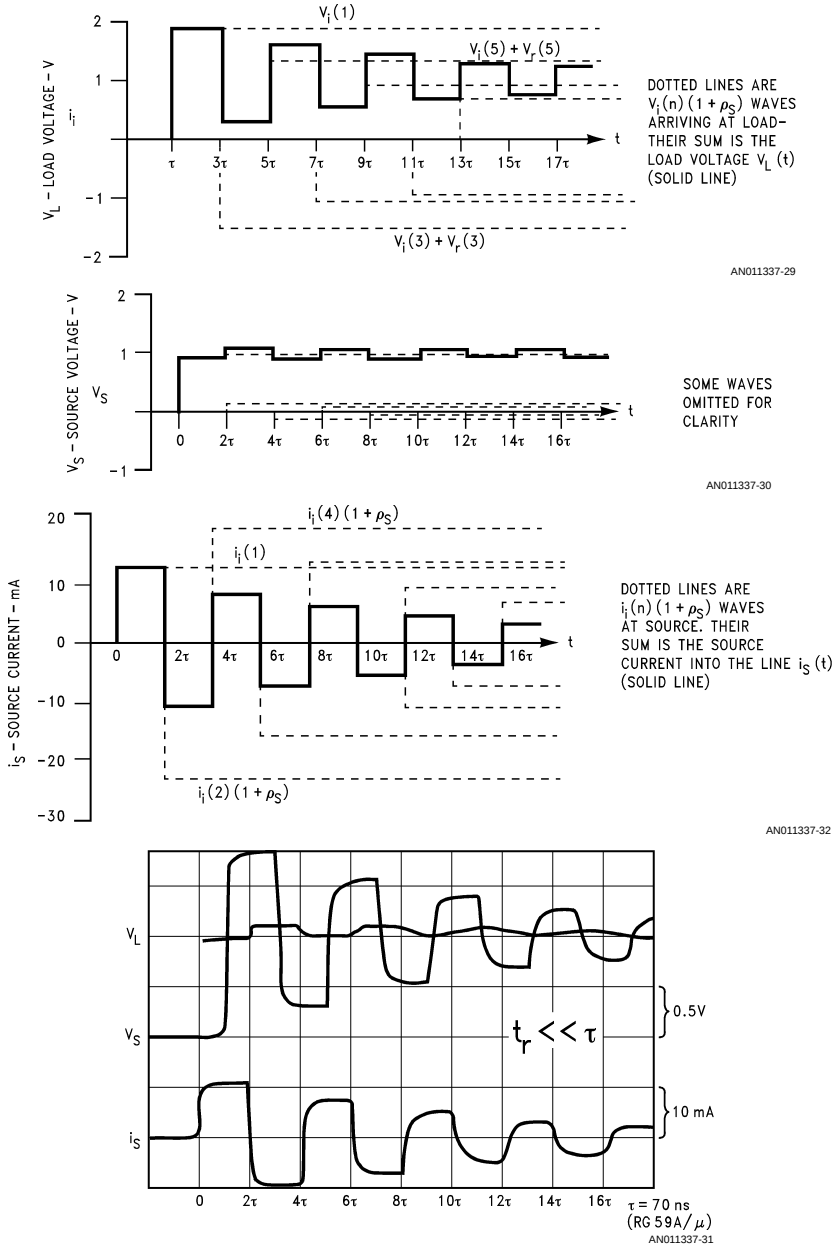


FIGURE 21. Waveforms for $t_r = 2 \ll \tau$

If the source excitation is adjusted so that its 0-to-100% rise time t_r is equal to 2τ, each of the $v_i + v_r$ and $i_i + i_r$ waveforms must be modified to include this rise time. The waves will have the same final value as predicted by the lattice diagram, but they now require two line time delays to reach this final value. The v_L, v_S and i_S waveforms consist of the superposition of these linear ramps. Because each wave reaches its final value just as a new wave arrives, their superposition converts the square edged v_L, v_S and i_S waveforms into triangular waveforms. This is shown in *Figure 22*. The accompanying oscilloscope plot shows the close correspondence between the actual and theoretical waveforms whereas an additional oscilloscope photograph in *Figure 22* shows the actual waveforms for the case where $t_r = \tau$. Not surprisingly, the $t_r = \tau$ case changes the v_L, v_S and i_S waveforms of the

$t_r \ll \tau$ case into trapeziodal forms because each arriving wave reaches its final value well before a new wave arrives.

If the source excitation is adjusted such that its rise time equals three line delays $t_r = 3\tau$, the $v_i + v_r$ and $i_i + i_r$ waves overlap for a period of time equal to τ. That is, each wave reaches only ⅔ of its final value when a new wave starts arriving. Considering the waveform, the load voltage from time τ to 3τ is

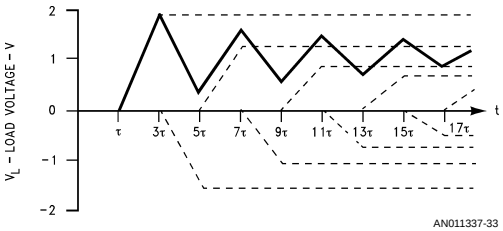
$$v_i(1)\ (1 + \rho_L)\ e\ (t - \tau)$$

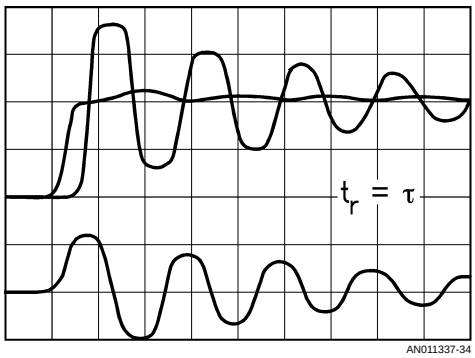
Starting at $t = 3\tau$, the wave

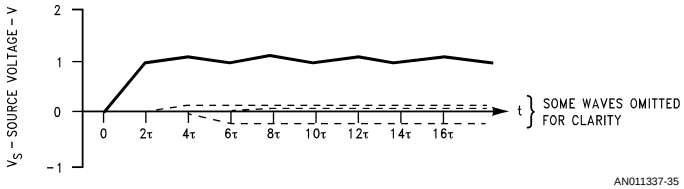
$$v_i(3) = v_i(1)\rho_S\rho_L\ e(t - 3\tau).$$

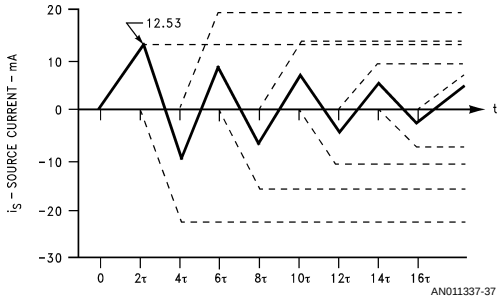
begins arriving from the source, and the load voltage then is the superposition of these two waves. Because $v_i(3)$ is a negative wave ($\rho_S < 0$), the algebraic sum of the last third of the first wave and the first third of the second wave $v_i(3)$ arriving at the load causes the load voltage to reduce in amplitude from the ($t_r \ll \tau$) case. Likewise, the source voltage and source current show reduced amplitudes over the ideal case, due to the overlap period of the waves arriving at the source.

Theoretical and actual waveforms for the $t_r = 3\tau$ case are shown in *Figure 23*. Notice that load voltage perturbations and source current i_S requirements are reduced from those of the $t_r \ll \tau$ case. Similarly, the ratio of t_r to τ can be successively increased. This results in reduced ringing on the load voltage and reduced source current due to the overlapping of more and more $v_i + v_r$ (or $i_i + i_r$) waves. Actual and theoretical waveforms for t_r equal to 4τ, 6τ, and 8τ are shown in *Figure 24*, *Figure 25* and *Figure 26*, respectively. In each case, as the t_r to τ ratio is increased, the instantaneous source and load voltages become more equal. The source current is also reduced so that the circuit exhibits fewer reflection effects and the transmission line itself can be considered as a simple interconnection from dc circuit theory.









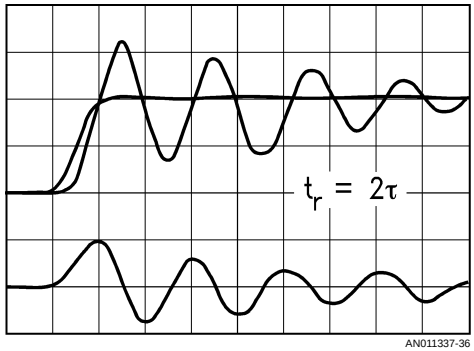


FIGURE 22. Waveforms for $t_r = 2\tau$

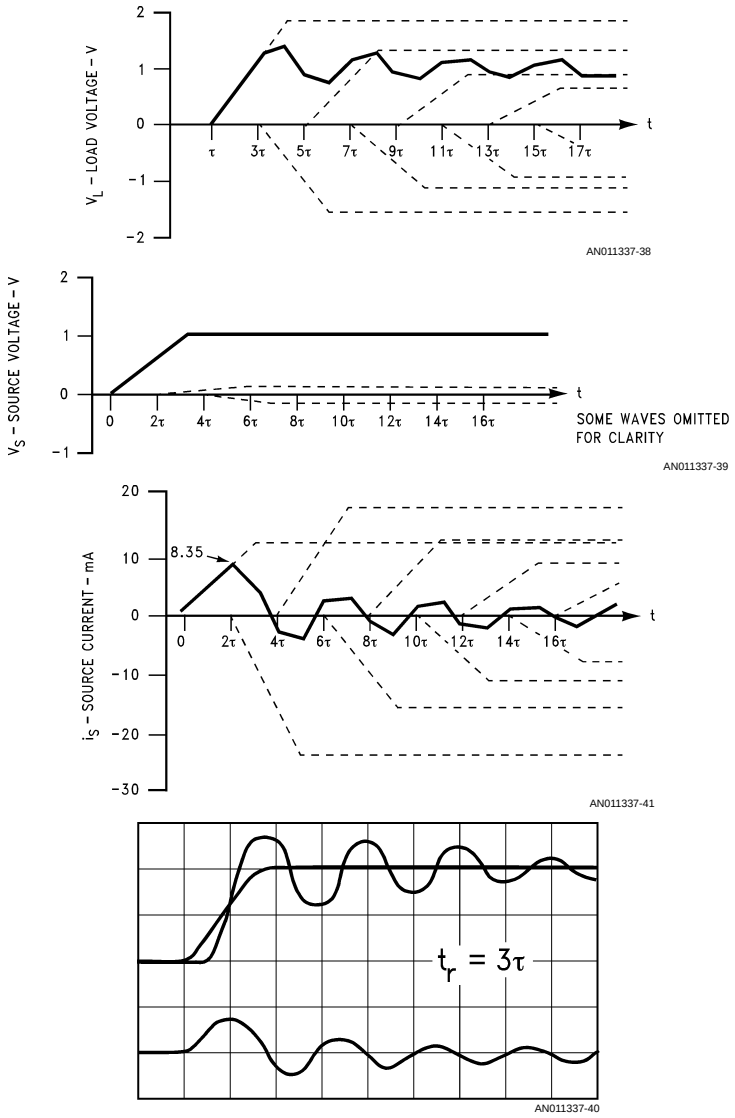
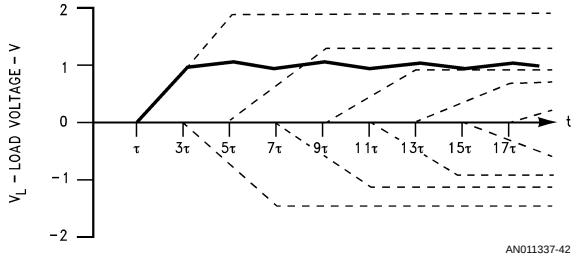
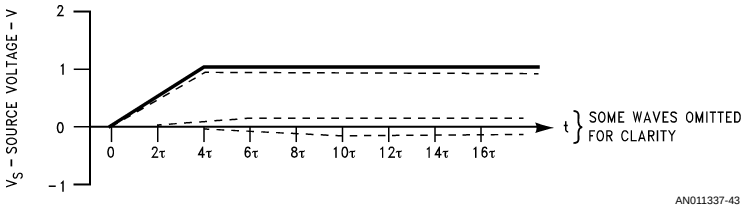
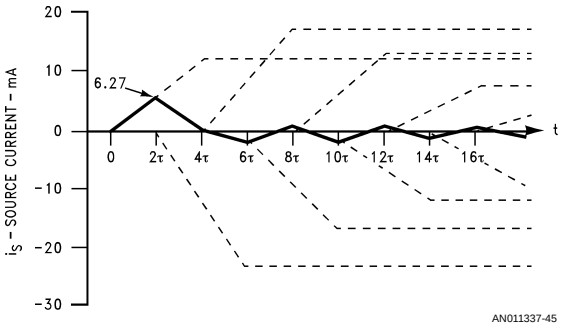


FIGURE 23. Waveforms for $t_r = 3\tau$







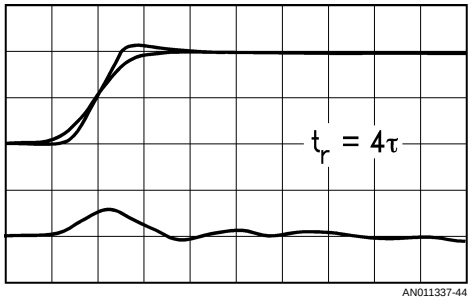


FIGURE 24. Waveforms for $t_r = 4\tau$

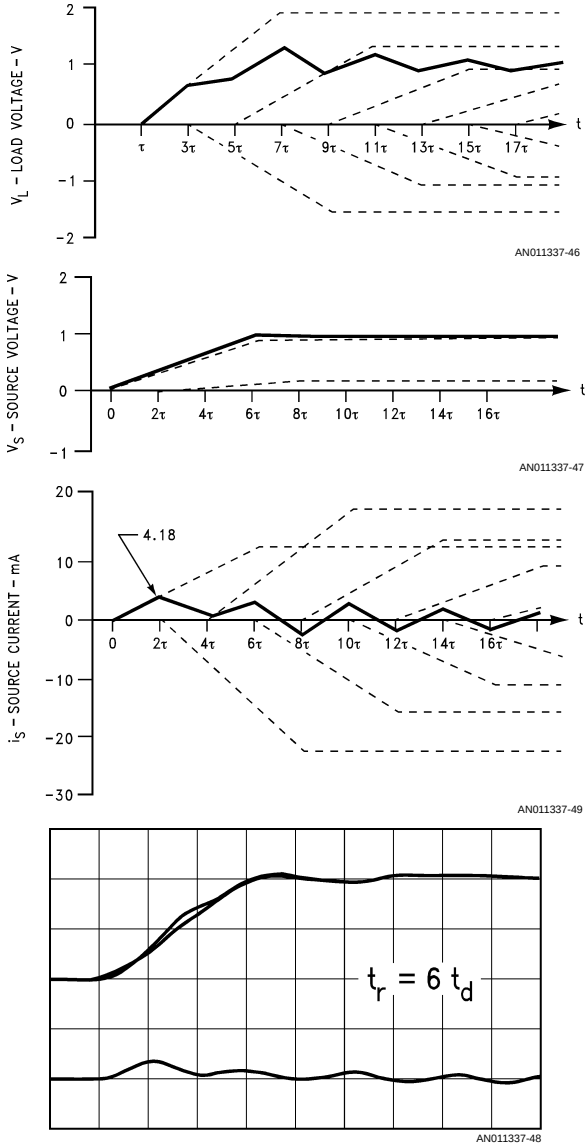


FIGURE 25. Waveforms for $t_r = 6\tau$

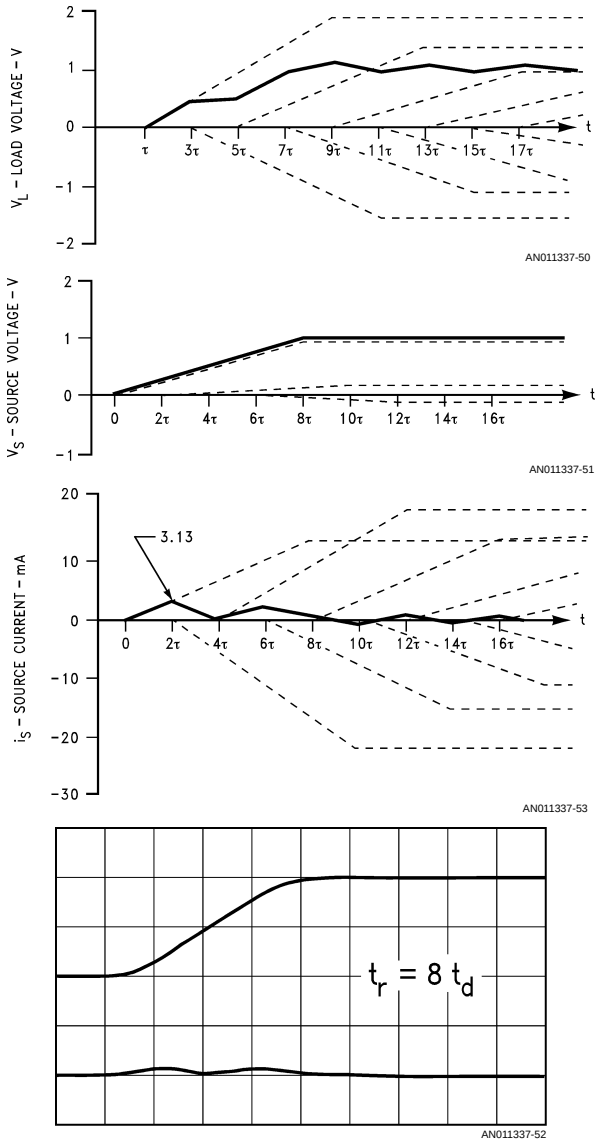


FIGURE 26. Waveforms for $t_r = 8\tau$

Using the t_r to τ ratio to reduce reflection effects has many practical advantages in digital design. The low source and high input resistance of TTL or ECL circuits allows one gate to drive many receiving gates. The reflection effects of this unterminated combination, however, can cause data errors or at least lead to reduced noise immunity due to the pronounced load voltage undershoot. Since the rise and fall times of these devices are easily measured, a maximum line length can be set such that the resulting t_r to τ ratio provides the desired reduction in ringing. This is the primary basis for the wiring rules of each logic family and, usually, the t_r to τ ratio is chosen somewhere between 3:1 and 4:1. As an example, the rise and fall time for normal TTL is $t_{10\%-90\%}$ = 6 ns. When this is converted to an equivalent linear 0% to 100% time, t_r = 8 ns. A common propagation delay of 1.7 ns/ft, in combination with the requirement that $t_r = 3\tau$, gives the maximum line length of approximately 18 inches. This corresponds with the published recommendation of the various manufacturers for the 74 series TTL circuits. A similar computation of the rise and fall times for other logic families yields their respective line length recommendations. The faster families require shorter line lengths for the same $t_r$to τ ratio, and slower logic families allow relatively longer line length. This ratio can also be used to make stubs or taps on lines “disappear”. In other words, if the stub’s time delay is made very short when compared to the t_r of the sig-

nal at the stub line location, the stub reflections will have a minimal effect on the line signals. A stub length to generate a t_r to τ ratio of greater than 8:1 is usually considered adequate to negate the stub reflections.

The third primary application of the t_r to τ ratio for controlling reflection effects is that used in some standard data communications interfaces such as EIA/TIA-232-E (RS-232). Here, driver slew rate is explicitly controlled. This, along with the implied maximum interconnect cable length serves to produce a t_r to τ ratio of 3:1 or greater. This, in turn, reduces the reflection effects inherent in a voltage source driver, unterminated line system. The main disadvantage of using the t_r to τ ratio to control reflection effects is in the overall time for the signal representing the data to rise above the receiver threshold level. With the parallel terminated method, the minimum time delay was τ or one line delay. When the t_r to τ ratio is used, an additional delay time of approximately 0.5 $t_r$is added to the line delay yielding, therefore, a greater effective signal propagation delay. This increased delay may or may not be acceptable in the desired system so the trade-off between ease of usage of the unterminated case must be weighed against the increased effective signal delay over that delay obtainable with the terminated case.

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See AN-806 and AN-808

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