

Simple Byte Parity Applications Featuring the FAST® 74F899

National Semiconductor
Application Note 753

J. Chapin
G. Connolly
J. Davis
February 1991



Simple Byte Parity Applications Featuring the FAST 74F899

Maintaining data integrity during transmission and retrieval from storage devices is a constant challenge for computer designers. Meeting this challenge is increasingly important for the ongoing evolution of higher-performance high-density memory systems, ranging from low-end PCs to high-end work stations and mainframes. Of the various methods used to improve data integrity in the transmission, storage, and retrieval of data/address words in computer systems, two of the most common are: (1) Error Detection and Correction (EDAC) and (2) Simple Byte Parity (SBP).

EDAC is generally found in higher-end systems. This technique uses modified Hamming code to detect and correct single-bit errors in whole data words. For example, the FAST 74F632 EDAC device is typically used to insure data integrity from storage devices. The 74F632 generates a 7-bit check word from an incoming 32-bit data word. The check word is then stored in memory along with the data word during the memory write cycle. During the memory read cycle, the EDAC processes the 39 bit word to determine if errors exist. Only single-bit errors in the 32-bit data word are flagged and corrected by the EDAC. Single-bit errors in the check word and 2-bit errors in any of the 39-bit positions of the word are flagged but cannot be corrected. Three or more simultaneous-bit errors can cause EDAC to perceive no error, correctable error, or uncorrectable error and will produce erroneous results in all three cases. Gross errors of all 39 bits low or high will be recognized and flagged.

SBP implementations can be found in a broad spectrum of computer systems. Typically a parity tree circuit initially evaluates the byte and adds a parity status bit based on the odd/even bit content of the byte. If subsequent evaluation of the byte indicates a parity status bit change, then an error condition is flagged. SBP is effective at flagging single-bit errors within each byte plus parity word, but cannot determine the error location or correct the bit error within the 9-bit word. Some multiple-bit errors within each byte plus parity word will also be flagged, i.e., 3-, 5-, 7-, and 9-bit errors. SBP is commonly used to improve data integrity during transmission on the buses and across backplanes. SBP is also easily used in lieu of EDAC in managing the integrity of data flowing to and from storage devices. System response to detection of parity error typically will be a resend of data or an initiation of diagnostics.

The data word width used in a system can influence the designer's choice of SBP or EDAC for the application. For systems with data word width up to 64 bits, SBP can be

more attractive versus EDAC in terms of the memory and board routing overhead. For example, 32-bit data systems need to route four extra parity bits for SBP versus 7 bits extra for EDAC. The system memory will be similarly burdened by having to store the wider EDAC words. For 64-bit data words, EDAC achieves parity on the overhead to support eight extra bits of EDAC versus the eight extra SBP Bits. Another factor influencing the designer's choice is the effectiveness of error detection. In the 32-bit 74F632 EDAC example discussed earlier, we noted that single- and dual-bit errors in the whole 39-bit word were accurately flagged but that three or more bit errors will be processed incorrectly. With the 32-bit SBP system, 1-, 3-, 5-, 7-, and 9-bit errors in each data byte plus parity bit will be accurately flagged.

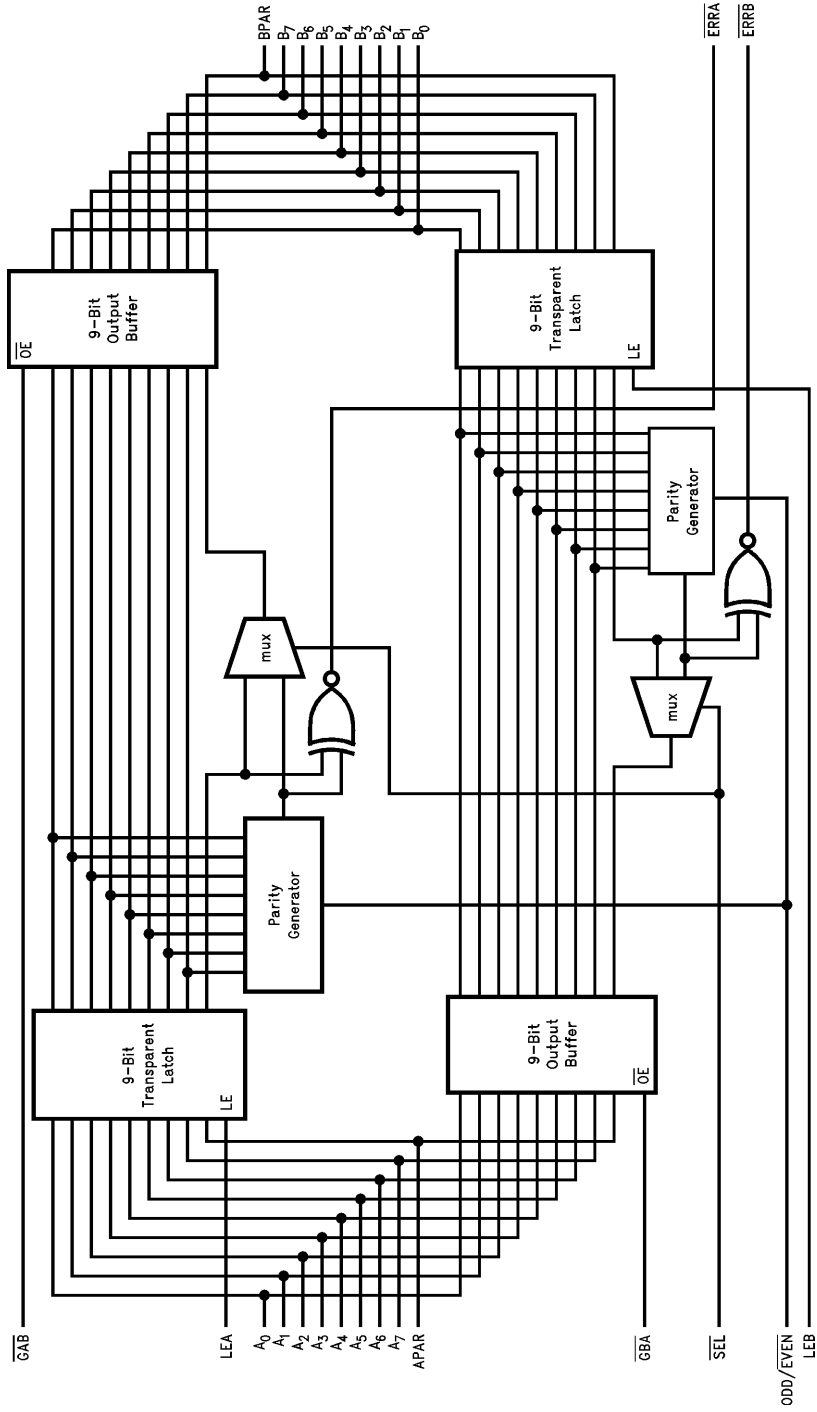
For a SBP system, parity is traditionally generated and transmitted without simultaneously checking for correct parity generation. Upon receipt of the word, data plus parity, the receiver will re-generate parity and check against the original transmitted parity bit. Logic devices are typically used in various combinations to implement these systems, i.e., 74F373/573, 74F280, and 74F541 or 74F573 and 74F657 or equivalent devices or PLD's. The 74F657 is particularly useful in that it will generate and transmit parity and will perform a parity check upon a direction reversal, i.e., read-back mode. However, SBP systems using the 74F657 tend to be awkward in checking parity. After parity generation, system buses need to be TRI-STATE®, device direction reversed and the system buses re-enabled prior to doing the parity check. This is time consuming, inefficient, and degrades the system performance.

The desire for enhanced byte parity system performance has led to development of National Semiconductor's 74F899. This single device incorporates latches and dual-parity generators onto a single die, eliminating the need for unnecessary bus direction reversal to check parity.

THE 74F899 IN BYTE PARITY SYSTEMS

The 74F899 is a 9-bit latchable transceiver with parity generation and simultaneous check capability. The 74F899 is packaged in the 28-pin PLCC. Owing to its functional complexity and flexibility of use, it can be efficiently applied in high-performance SBP systems. *Figure 1* illustrates the function blocks comprising the 74F899. Note that this single chip contains the approximate functional complexity of eight discrete IC's; two 74F843's, two 74F820's, two 74F827's, a 74F157, and a 74F86. The various modes of operation for the 74F899 are shown in Table I.

FAST® and TRI-STATE® are registered trademarks of National Semiconductor Corporation.



TL/F/10905-1

FIGURE 1. Functional Block Diagram

TABLE I. Function Table									
Inputs					Operation				
$\overline{\text{GAB}}$	$\overline{\text{GBA}}$	SEL	LEA	LEB					
H	H	X	X	X	Busses A and B are TRI-STATE.				
H	L	L	L	H	Generates parity from B[0–7] based on $\text{O}/\overline{\text{E}}$ (Note 1). Generated parity $\rightarrow$ APAR. Generated parity checked against BPAR and output as $\overline{\text{ERRB}}$.				
H	L	L	H	H	Generates parity from B[0–7] based on $\text{O}/\overline{\text{E}}$. Generated parity $\rightarrow$ APAR. Generated parity checked against BPAR and output as $\overline{\text{ERRB}}$. Generated parity also fed back through the A latch for generate/check as $\overline{\text{ERRA}}$.				
H	L	L	X	L	Generates parity from B latch data based on $\text{O}/\overline{\text{E}}$. Generated parity $\rightarrow$ APAR. Generated parity checked against latched BPAR and output as $\overline{\text{ERRB}}$.				
H	L	H	X	H	BPAR/B[0–7] $\rightarrow$ APAR/A[0–7] Feed-through mode. Generated parity checked against BPAR and output as $\overline{\text{ERRB}}$.				
H	L	H	H	H	BPAR/B[0–7] $\rightarrow$ APAR/A[0–7] Feed-through mode. Generated parity checked against BPAR and output as $\overline{\text{ERRB}}$. Generated parity also fed back through the A latch for generate/check as $\overline{\text{ERRA}}$.				
L	H	L	H	L	Generates parity for A[0–7] based on $\text{O}/\overline{\text{E}}$. Generated parity $\rightarrow$ BPAR. Generated parity checked against APAR and output as $\overline{\text{ERRA}}$.				
L	H	L	H	H	Generates parity from A[0–7] based on $\text{O}/\overline{\text{E}}$. Generated parity $\rightarrow$ BPAR. Generated parity checked against APAR and output as $\overline{\text{ERRA}}$. Generated parity also fed back through the B latch for generate/check as $\overline{\text{ERRB}}$.				
L	H	L	L	X	Generates parity from A latch data based on $\text{O}/\overline{\text{E}}$. Generated parity $\rightarrow$ BPAR. Generated parity checked against latched APAR and output as $\overline{\text{ERRA}}$.				
L	H	H	H	L	APAR/A[0–7] $\rightarrow$ BPAR/B[0–7] Feed-through mode. Generated parity checked against APAR and output as $\overline{\text{ERRA}}$.				
L	H	H	H	H	APAR/A[0–7] $\rightarrow$ BPAR/B[0–7] Feed-through mode. Generated parity checked against APAR and output as $\overline{\text{ERRA}}$. Generated parity also fed back through the B latch for generate/check as $\overline{\text{ERRB}}$.				

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
Note 1: $\text{O}/\overline{\text{E}}$ = ODD/EVEN

FUNCTIONALITY DISCUSSION

Referring to *Figure 1*, note that use of two parity generators is key to the 74F899's enhanced functional flexibility. With both latches transparent, the 74F899 performs bidirectional, realtime checking of the incoming byte and its parity bit. For example, when transferring data from A side to B side, parity is regenerated for the byte at A_{0-7} , compared against APAR, and flagged at $\overline{\text{ERRA}}$. The A_{0-7} byte and its original parity bit APAR is output to B_{0-7} and BPAR respectively. This is known at the feedthrough mode when $\text{SEL} = \text{high}$. The regenerated parity bit is output at BPAR in generate mode when $\text{SEL} = \text{low}$. The byte and parity bit at B side are fed through the transparent B side latch. Parity is regenerat-

ed for the B_{0-7} byte, compared against BPAR, and flagged at $\overline{\text{ERRB}}$. In this example, realtime parity checking was performed on both sides during data transmission without having to TRI-STATE the B side bus. In feedthrough mode, APAR feeds through to BPAR and vice versa, and the device behaves as a 9-bit latchable transceiver with optional bidirectional parity checking. The parity checking is termed "optional" since if the APAR/BPAR bit is actual parity relevant to bytes $\text{A}_{0-7}/\text{B}_{0-7}$, only then will the response at $\overline{\text{ERRA}}/\overline{\text{ERRB}}$ be relevant. In the generate mode (internally-generated parity bit is output), the device essentially behaves as a 8-bit latchable transceiver with bidirectional parity generate and optional bidirectional parity check capability. Again, the term "optional" applies as mentioned above.

The device can be configured for use in systems with odd or even parity. The I_{OH}/I_{OL} drive capability is $-3/24$ mA for the A_{0-7} and APAR outputs. The B_{0-7} and BPAR outputs, being designed to drive the system backplane, will drive $-15/64$ mA. The error outputs, $ERRA$ and $ERRB$ are active low with standard FAST bi-state drive for greatest flexibility. (Refer to Table I for more details on the 74F899's functional operation.)

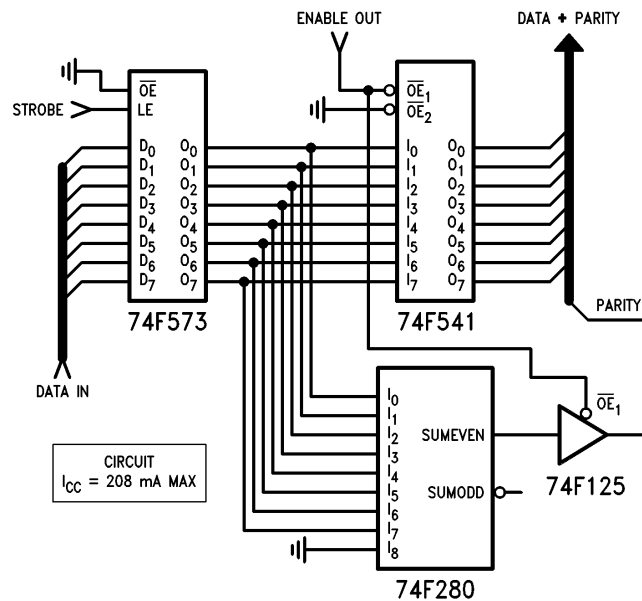
An additional feature of the 74F899 is an ability to be configured for system diagnostics by identifying parity generation errors. Diagnostics can be performed via manipulation of the ODD/EVEN and/or APAR (BPAR) signals when in the feedthrough configuration and with the respective latches transparent. The ability to read-back via the latches also assists software programmers in debugging a system.

Some noteworthy performance features of the 74F899 include:

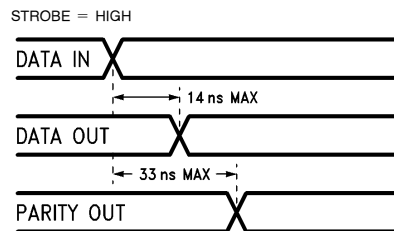
- Data to Latch Enable $t_S/t_H = 5/0$ ns (min),
- Data to Generated Parity/Error = 18 ns (max),
- Data In to Data Out (transparent) = 14 ns (max),
- I_{CC} max = 210 mA, and ESD protection = 4000V min.

COMPARISON OF 74F899 PERFORMANCE WITH DISCRETE LOGIC IMPLEMENTATION

The 74F899's enhanced functional flexibility and superior performance are best illustrated by direct comparison with various discrete logic SBP implementations for parity generation and checking. The basic assumption is made that all practical discrete applications will necessitate an input data latch capability and TRI-STATE outputs in consideration of CPU efficiency and bus-interface compatibility.

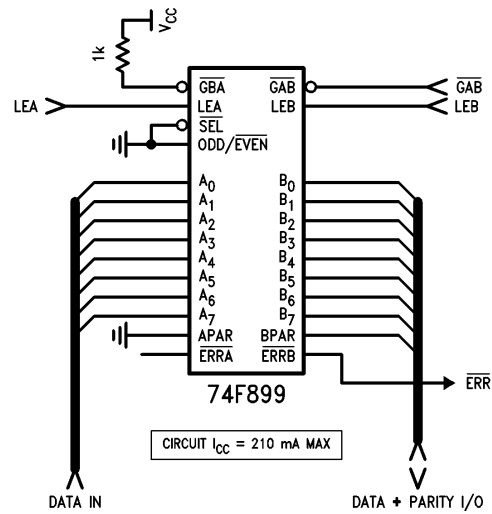


TL/F/10905-2

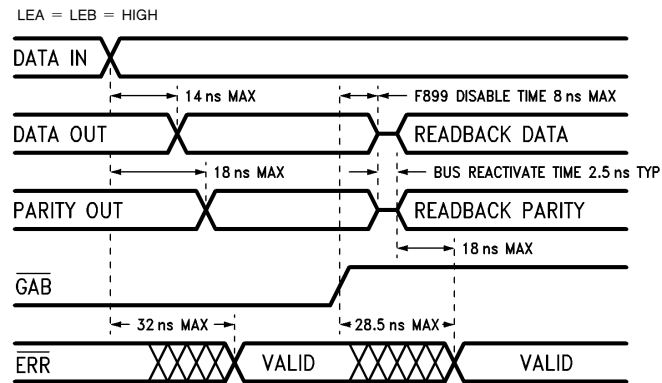


TL/F/10905-3

FIGURE 2a. Simple Byte Parity Generate Discrete IC Circuit



TL/F/10905-4

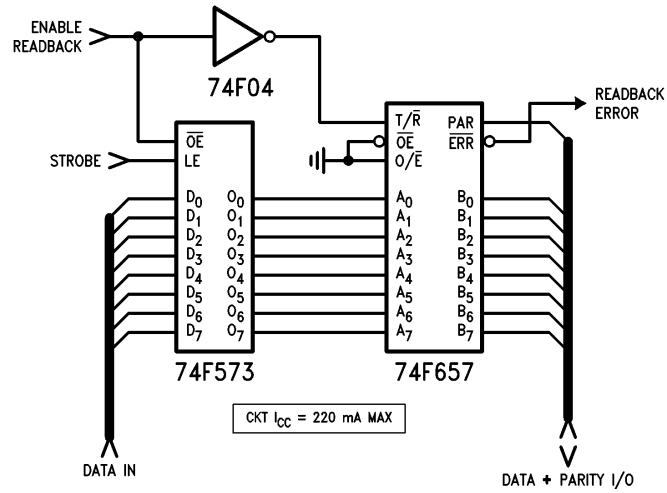


TL/F/10905-5

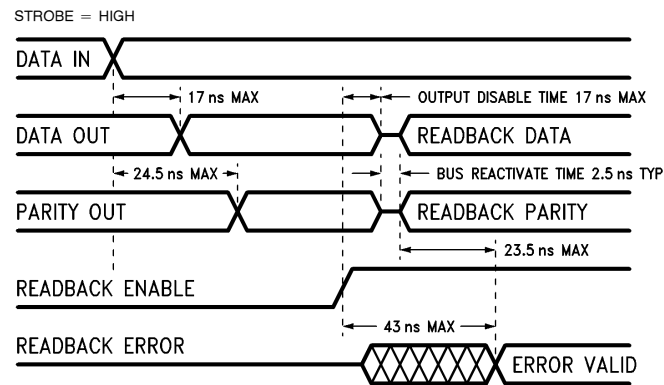
Figure 2b. Simple Byte Parity Generate 74F899 Circuit

Figure 2a illustrates the use of standard logic devices to generate—but not check parity—in a parity generate/transmit application where checking is done separately at the receiver. Compare this circuit's performance with the equivalent function performed by the 74F899 shown in Figure 2b. Note that despite Figure 2a circuit's functional simplicity, the 74F899 implementation is closely matched in power con-

sumption (I_{CC}). Both implementations propagate the data byte in 14 ns, but the 74F899 is considerably quicker in outputting the parity bit onto the bus at 18 ns versus the 35 ns of Figure 2a. As shown in the timing diagrams, the 74F899's generate mode inherently provides realtime parity transmission check capability through the transparent B side latch and also provides the classic readback parity check capability.

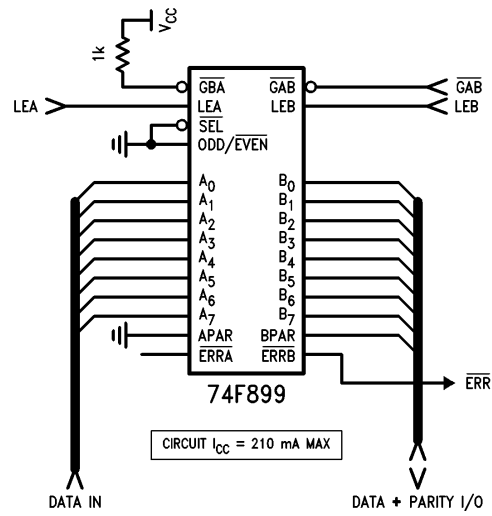


TL/F/10905-6

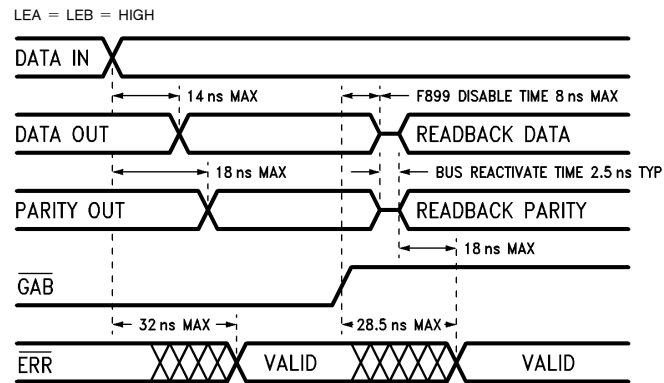


TL/F/10905-7

Figure 3a. Simple Byte Parity Generate with Readback Check Discrete IC Circuit



TL/F/10905-8

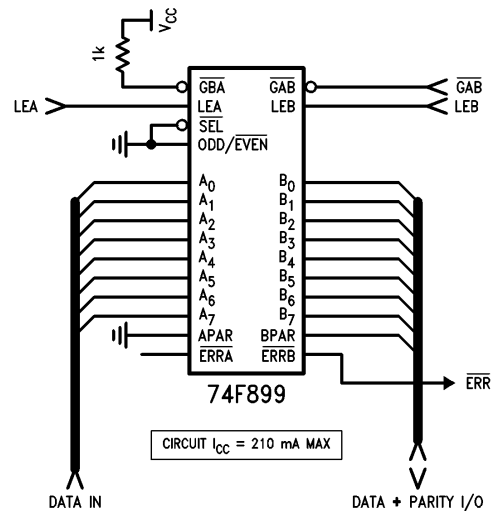


TL/F/10905-9

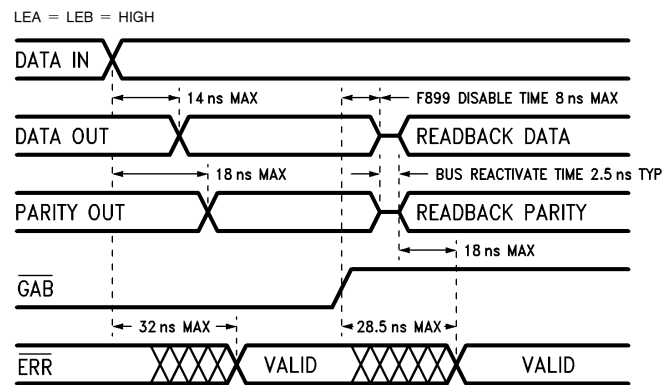
Figure 3b. Simple Byte Parity Generate with Readback Check 74F899 Circuit

Figure 3a illustrates the classical use of the 74F657 in the parity generate with readback check mode. Comparison with the 74F899's implementation of Figure 3b shows the 74F899 to be superior in all performance aspects. Again the

74F899 provides an inherent bonus of realtime parity transmission check capability over that of the discrete IC implementation.



TL/F/10905-12

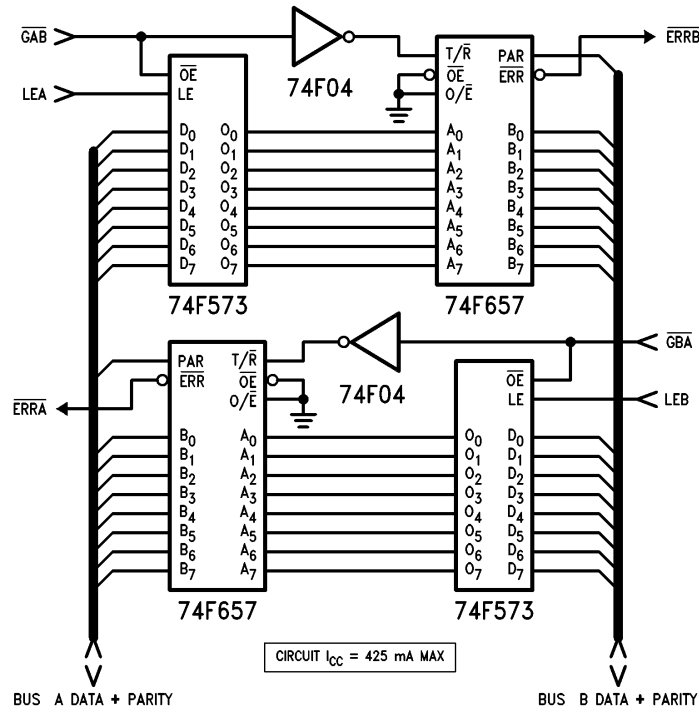


TL/F/10905-13

Figure 4b. Simple Byte Parity Generate and Realtime/Readback Check 74F899 Circuit

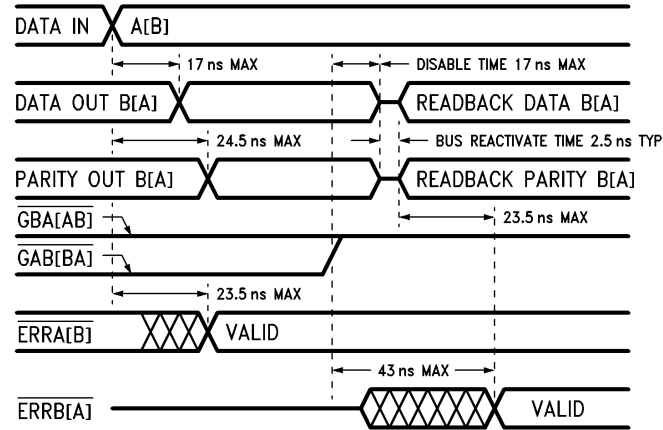
Figure 4a illustrates the addition of a second 74F280 to the Figure 2a circuit to add realtime and readback parity check capability. The comparison to the 74F899's implementation in Figure 4b shows the 74F899 is again the performance leader in all areas except time-to-readback parity check.

The circuit in Figure 4a has a slight speed advantage since the parity checker is tied directly to the bus. It is at a functional disadvantage to the 74F899 since the readback data must be held stable on the bus significantly longer due to absence of latching capability.



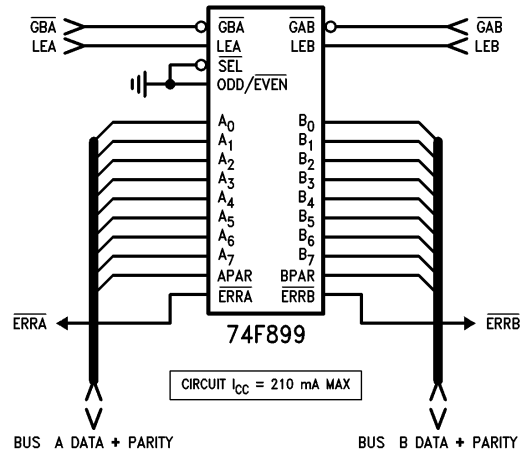
TL/F/10905-14

LEA = LEB = HIGH

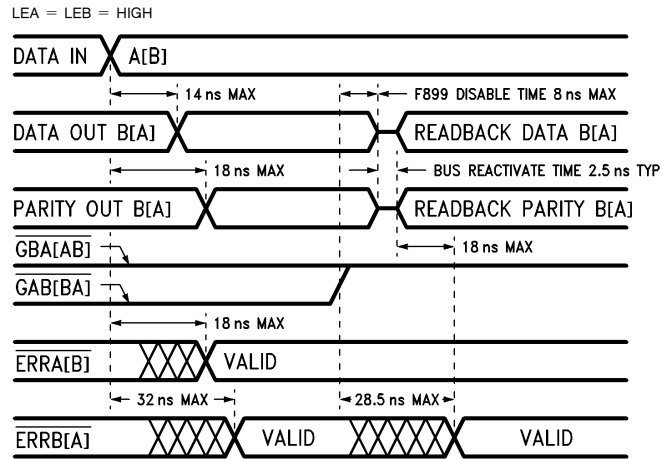


TL/F/10905-15

Figure 5a. Bidirectional Byte Parity Generate and Check Discrete IC Circuit



TL/F/10905-16



TL/F/10905-17

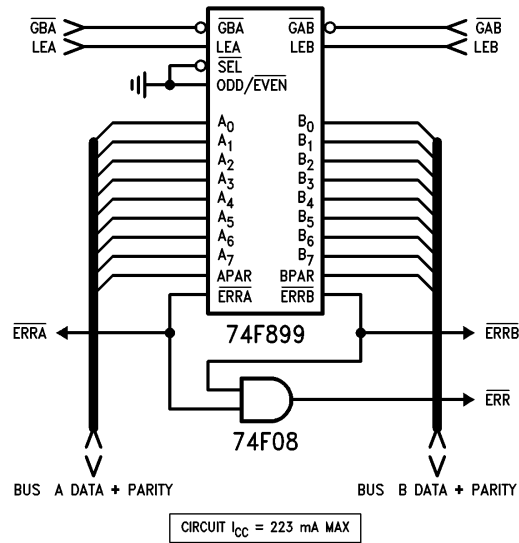
Figure 5b. Bidirectional Byte Parity Generate and Check 74F899 Circuit

Figure 5a illustrates the use of 74F657s in a manner which begins to approximate the functional capabilities of the 74F899, i.e., bidirectional parity generate with check. Comparison to the 74F899 implementation in Figure 5b shows the 74F899 to again be the superior performer in all areas. Although both implementations perform realtime incoming parity checks and readback checks, only the 74F899 is capable of the realtime check of outgoing transmitted data/parity.

THE 74F899 CONFIGURED FOR DIAGNOSTICS

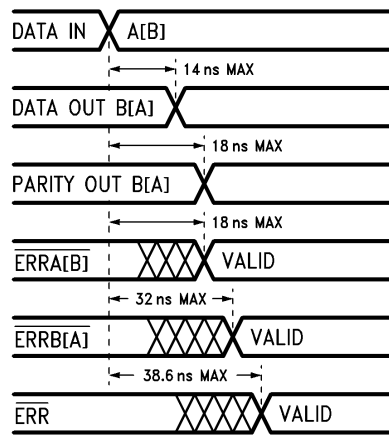
Figure 6a illustrates the 74F899 configured for diagnostics in parity generate mode. Parity is regenerated from the in-

coming data byte A_0-7 . Incoming parity $APAR$ is checked against the regenerated bit and any error is flagged at $\overline{ERRA}$. The data byte and its regenerated parity bit is passed to the B-bus. With LEB HIGH, the data on the B-bus is fed back into the device and a second generation/check is performed with error flagged at $\overline{ERRB}$. ANDing of the $\overline{ERRA}$ and $\overline{ERRB}$ signals provides a single error flag ($\overline{ERR}$) for parity discrepancies on both buses. This configuration is useful for detecting and diagnosing bus shorts/open circuits and/or parity generation errors internal or external to the 74F899. The ANDing of $\overline{ERRA}/\overline{ERRB}$ could also initiate a readback operation for comparison against the original data word transmitted.



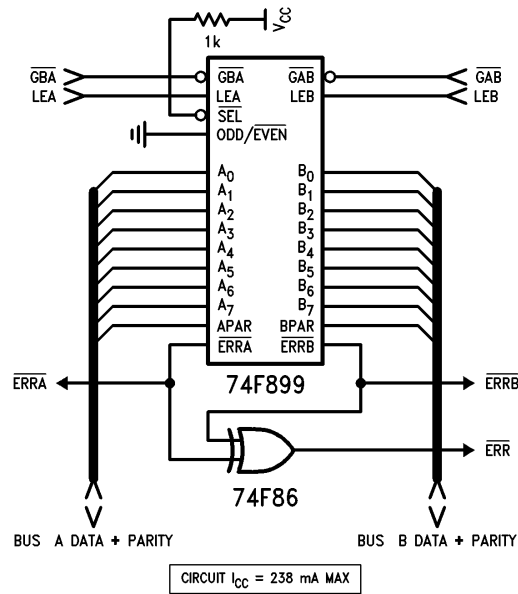
TL/F/10905-18

LEA = LEB = HIGH $\overline{\text{GAB}}(\text{GBA}) = \text{LOW } \overline{\text{GBA}}(\text{GAB}) = \text{HIGH}$

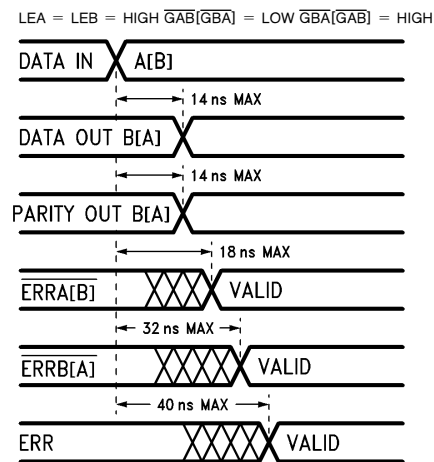


TL/F/10905-19

Figure 6a. 74F899 Generate Mode Diagnostics



TL/F/10905-20



TL/F/10905-21

Figure 6b. 74F899 Feedthrough Mode Diagnostics

Figure 6b illustrates the 74F899 uniquely configured for diagnostics in feedthrough mode. In this configuration, transmission errors will be flagged even if parity is not input. For example, with the 74F899 configured for even parity, if the A_{0-7} input byte is evaluated for parity and found to be odd, and if the APAR (9th) bit is intentionally not a parity bit and it is a valid low (even), then $\overline{\text{ERRA}}$ will go low indicating the 74F899's perception of a parity error. A_{0-7} is passed to B_{0-7} and APAR is passed to BPAR while the transparent B

side latch permits re-evaluation and corresponding perception of a parity error at $\overline{\text{ERRB}}$. The Exclusive-OR sees that $\overline{\text{ERRA}} = \overline{\text{ERRB}}$ and therefore no transmission error has occurred. Conversely, had a single 3-, 5-, 7-, or 9-bit change on the B side (any combination of B_{0-7} and BPAR bits) occurred in transmission, then $\overline{\text{ERRA}}$ would not equal $\overline{\text{ERRB}}$ and the XOR comparison would flag the error(s). This configuration is also useful for diagnosing a bus short/open on the receive side of the device or internal 74F899 parity generation errors.

SUMMARY AND CONCLUSIONS

Simple Byte Parity implementations using the 74F899 should be considered where enhancements to data transmission integrity are needed and should include applications where EDAC is traditionally used.

The principal enhancements offered by the 74F899 in SBP applications over a discrete implementation include:

- Replacement of up to eight logic devices with a single 28-pin PLCC package.
- Significantly lower power consumption than discrete implementations having functional similarity to the 74F899, i.e., bidirectional parity generate and check.
- Superior throughput in a system environment: Real-time error checking versus the readback method common with other implementations.
- Superior diagnostic capability within a system.
- Capability for functional configuration as a 9-bit 74F245 or 74F543, i.e., feedthrough mode.

Lit. # 100753

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



National Semiconductor Corporation
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090
Tel: (408) 272-9959
TWX: (910) 339-9240

National Semiconductor GmbH
Livny-Gargan-Str. 10
D-82256 Fürstenfeldbruck
Germany
Tel: (81-41) 35-0
Telex: 527849
Fax: (81-41) 35-1

National Semiconductor Japan Ltd.
Sumitomo Chemical
Engineering Center
Bldg. 7F
1-7-1, Nakase, Mihama-Ku
Chiba-City,
Chiba Prefecture 261
Tel: (043) 299-2300
Fax: (043) 299-2500

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semicondutores Do Brazil Ltda.
Rue Deputado Lacorda Franco
120-3A
Sao Paulo-SP
Brazil 05418-000
Tel: (55-11) 212-5066
Telex: 391-1131931 NSBR BR
Fax: (55-11) 212-1181

National Semiconductor (Australia) Pty. Ltd.
Building 16
Business Park Drive
Monash Business Park
Nottingham, Melbourne
Victoria 3168 Australia
Tel: (3) 558-9999
Fax: (3) 558-9998