Description of the NS32GX320 Bus Fairness Mechanism

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INTRODUCTION

This application note describes the Bus Fairness Mechanism in the NS32GX320 High-Performance 32-bit Embedded System Processor. The NS32GX320 is composed of a 32-bit CPU, 2-channel Direct Memory Access Controller (DMAC), an interrupt control unit (ICU) and three 16-bit timers. The Bus Fairness Mechanism is a programmable feature designed to enable the NS32GX320 user to control the bus arbitration between the CPU and the DMAC.

The note is divided into 3 sections. Section 1 presents a general description of the DMAC, including the bus arbitration and bus fairness mechanisms.

Section 2 presents a complete description of the bus fairness mechanism and its parameters.

Section 3 presents examples of different bus fairness parameters and their effect on NS32GX320 behavior.

BACKGROUND

The DMAC supports two channels for transferring blocks of data between memory and I/O devices with minimal CPU intervention. Each channel can be programmed to perform FLYBY (Direct) or Memory-To-Memory (Indirect) data transfers. In FLYBY mode at least one end of the channel is an I/O device.

Bus fairness between the CPU and the DMAC gives a low priority device the chance to gain control of the bus even though a higher priority device is requesting control at the same time. The bus fairness mechanism is user programmable.

The DMAC enters the bus aquisition state (to obtain control of the bus) when it detects a channel request signal on the corresponding DMA channel REQUEST ($\overline{DRQ}$) pin. The subsquent bus arbitration is done using a fixed priority scheme. The priority scheme is ordered as follows: $\overline{HOLD}$ request has the highest priority, followed by channel 0, then channel 1. The CPU has the lowest priority.

Once the bus is granted in response to a DMA channel request and no higher priority request is pending, the selected channel can use the bus for a certain number of back-to-back transfers before it is forced to relinquish the bus. The determination of when to relinquish the bus is controlled by the bus fairness mechanism. This mechanism prevents a DMAC channel from monopolizing the bus. The maximum number of back-to-back transfers can be programmed through the Block Transfer Length (BLT) field in the Mode Control register. The channel relinquishes the bus for at least one cycle after the programmed number of transfers is complete. This frees the bus for a lower priority request.

Note: The CPU has priority over the second channel during the cycle when the bus is released because of the bus fairness mechanism. Note that except for this instance the DMAC channels always have priority over the CPU.

DESCRIPTION

The bus fairness mechanism is controlled by the Mode Control register BLT field (bits [10:14]) *(Figure 1)*. Since each channel has its own MODE register each channel can have different parameters for bus fairness.

The fields for these parameters are:

BWA—Device A bus width bits [7:8] of MODE register.
- 00 - 8 bits bus width
- 01 - 16 bits bus width
- 10 - 32 bits bus width
- 11 - (reserved)

BWB—Device B bus width bits [4:5] of MODE register.
- 00 - 8 bits bus width
- 01 - 16 bits bus width
- 10 - 32 bits bus width
- 11 - (reserved)

BLT—Block Length Transfer bits [10:14] of MODE register.

The Bus Width related to a certain transfer is determined according to the following criteria:

1. In FLYBY mode bus width is determined according to BWA field in Mode Control Register.
2. In Memory-To-Memory mode bus width is determined according to the smallest bus width of the two nodes (Minimum between BWA and BWB fields in Mode Control Register).

Table I presents a functional description of each combination within the BLT field and describes the maximum number of back-to-back transfers for different values of BLT field in MODE register.

Refer to the NS32GX320 Data Sheet for DMAC registers' description.

31 15	14 10	9	8 7	6	5 4	3	2	1	0
RESERVED	////// BLT //////	ABA	////// BWA //////	ADB	////// BWB //////	DIR	FBY	RES	OT

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FIGURE 1

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TABLE I

BLT in MODE Control Reg bits [10:14]	Functional Description	Maximum Numbers of DMAC Transfers		
		BYTE Transfers	WORD Transfers	DOUBLE__WORD Transfers
0 0 0 0 0	DMAC will not relinquish the bus unless the respective $\overline{DRQ}$ pin is deasserted, or the block transfer is completed.	Unlimited	Unlimited	Unlimited
0 0 0 0 1	DMAC will relinquish the bus after each transfer.	1	1	1
0 0 0 1 0	DMAC will relinquish the bus whenever the least significant bit of Transfer Complete Counter (TCC) equals 0 [e.g., after transferring 16 bits (WORD)]. The TCC counts the number of bytes transferred.	2	1	1
0 0 1 0 0	DMAC will relinquish the bus whenever the two least significant bits of the TCC equal 00 [e.g., after transferring 32 bits (DOUBLE WORD)].	4	2	1
0 1 0 0 0	DMAC will relinquish the bus whenever the three least significant bits of the TCC equal 000 [e.g., after transferring 64 bits (QUAD WORD)].	8	4	2
1 0 0 0 0	DMAC will relinquish the bus whenever the four least significant bits of the TCC equal 0000 [e.g., after transferring 128 bits (TWO QUAD WORDS)].	16	8	4

EXAMPLES

This section contains a number of examples of how to use the bus fairness mechanism. A table at the beginning of each example describes the parameters to be programmed and their meaning. Each table is followed by a timing diagram that describes the behavior of the NS32GX320 under those circumstances.

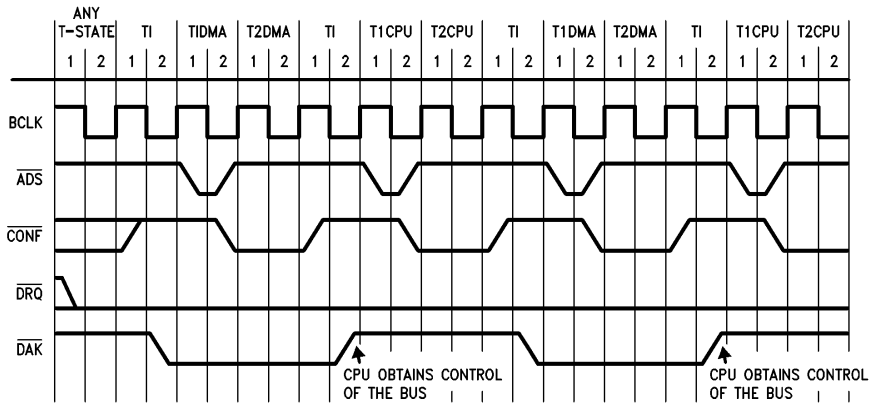
Example 1

The DMAC relinquishes the bus after each transfer. Each transfer is 1 byte because the bus width is 1 byte (Diagram 1). The CPU obtains control of the bus as soon as the DMAC relinquishes it (Table II).

TABLE II. Parameters for programming the DMAC to relinquish the bus after each byte transfer.

Bus Fairness Parameters	Values	Description
Bus Width	0 0	Bus Width is 8 bits (BYTE)
BLT Field	0 0 0 0 1	DMAC relinquishes the bus after each transfer.
MODE CONTROL REGISTER	H'608	OT = 0; auto-initialize off FLYBY = 0; flyby mode DIR = 1; write cycle in flyby BWB = 00; device B bw is 8 bits ADB = 1; address increment BWA = 00; device A bw is 8 bits ADA = 0; address unchanged BLT = see above.

Diagram 1



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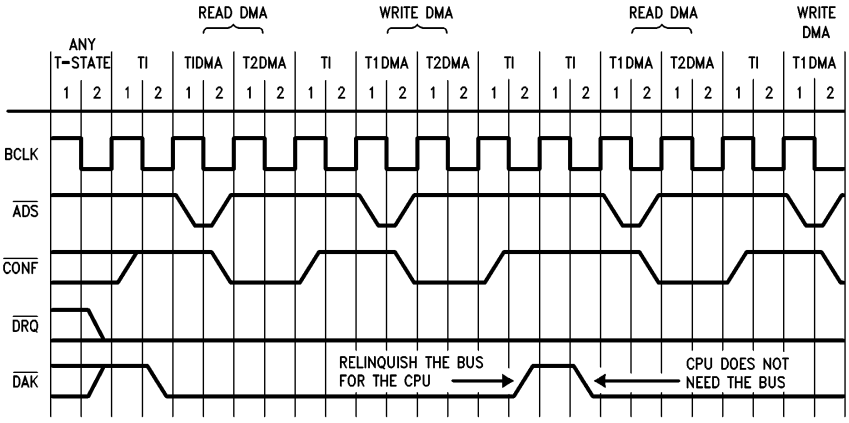
Example 2

Example 2 presents the case in which the DMAC relinquishes the bus, but the CPU does not obtain control of the bus, because it doesn't need the bus. This may occur when the CPU is in the middle of executing a long instruction or in idle state at the time that the DMAC relinquishes the bus. In Diagram 2, the CPU does not apply for the bus after the DMAC relinquishes it. After the idle bus cycle the DMAC is granted the bus for another transfer.

TABLE III. Parameters for programming the DMAC to relinquish the bus after each transfer (Bus Width is of one byte) therefore the bus is relinquished after each byte transfer.

Bus Fairness Parameters	Values	Description
Bus Width	0 0	Bus Width is 8 bits (BYTE)
BLT Field	0 0 0 0 1	DMAC relinquishes the bus after each transfer.
MODE CONTROL REGISTER	H'60C	OT = 0; auto-initialize off FLYBY = 1; memory to memory DIR = 1; write cycle in flyby BWB = 00; device B bw is 8 bits ADB = 1; address increment BWA = 00; device A bw is 8 bits ADA = 0; address unchanged BLT = see above.

Diagram 2



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Example 3

Example 3 uses the same parameters as in example 2. The difference between the two examples is that in example 3 the CPU obtains control of the bus. Diagram 3 shows that the CPU obtains control of the bus as soon as the DMAC relinquishes it.

Example 4

Example 4 presents the case in which the DMAC is programmed to unlimited number of back-to-back DMAC transfers. In this case, the DMAC does not relinquish the bus until the corresponding $\overline{DRQ}$ pin is deasserted or block transfer is completed.

TABLE IV. Parameters for programming the DMAC not to relinquish the bus.

Bus Fairness Parameters	Values	Description
Bus Width	0 0	Bus Width is 8 bits (BYTE)
BLT Field	0 0 0 0 0	DMAC will not relinquish the bus until the corresponding DRQ is deasserted, or EOT occurs, or block transfer is complete.
MODE CONTROL REGISTER	H'24C	OT = 0; auto-initialize off FLYBY = 1; memory to memory DIR = 1; write cycle in flyby BWB = 00; device B bw is 8 bits ADB = 1; address increment BWA = 00; device A bw is 8 bits ADA = 0; address unchanged BLT = see above.

Diagram 3

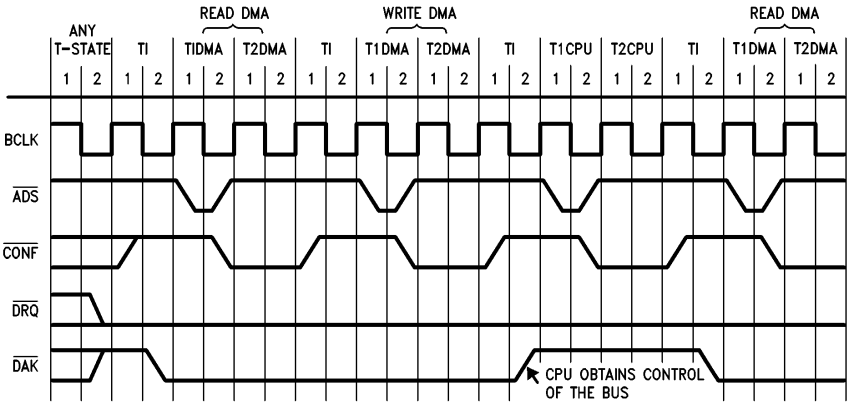

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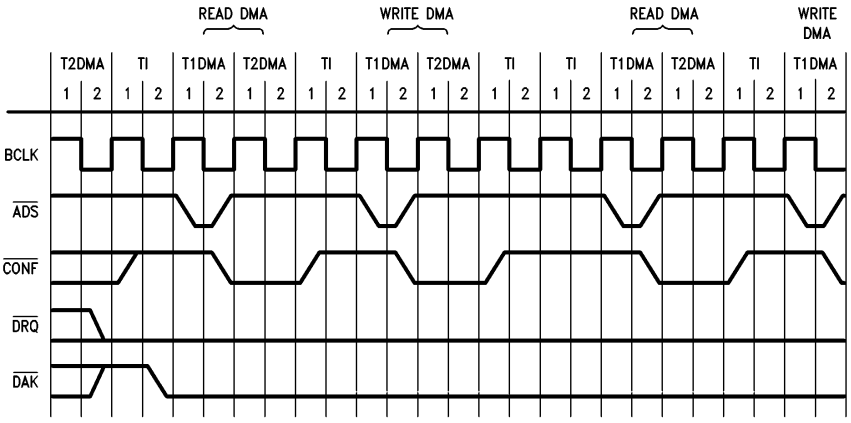
Diagram 4



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