Using the F100181 ALU and F100179 Carry-Lookahead

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INTRODUCTION

Speed is of paramount importance in the arithmetic unit of a system design. The National F100181 Arithmetic Logic Unit (ALU) in conjunction with the F100179 Carry-Lookahead offer a high-performance and efficient design solution. Besides the obvious performance benefits, they offer both temperature and voltage compensation which leads to better performance stabilization throughout the guaranteed ranges. Better noise immunity over TTL devices and more efficient designs by using wired-OR logic and complementary outputs are also benefits offered by these devices. This application note describes the function of the F100181 and F100179, offers configurations for their use, and gives a detailed timing analysis of the function settling times.

F100181 FUNCTIONAL DESCRIPTION

The F100181 is an ALU capable of performing sixteen arithmetic and logic operations on two 4-bit words. The operating mode is selected by four function-select lines (S_3–S_0). Arithmetic operations are selected when S_3 is LOW, and logic operations are selected when S_3 is HIGH. When S_3 is LOW, the arithmetic mode can be selected between binary and binary coded decimal (BCD) with the S_2 input [S_2 is LOW (BCD); S_2 is HIGH (binary)]. The remaining function-select inputs S_1, S_0 select between addition, subtraction, and the basic logical operations (refer to Table I).

Provision for simple ripple-carry cascading is available with the carry output ($\overline{C_n + 4}$). A carry unit ($\overline{C_n}$) is provided for use with arithmetic operations. In BCD mode, it can be used to perform a ten's complement result in subtraction. Likewise, in binary mode, it can be used to perform a two's complement result in subtraction.

A full carry-lookahead scheme is implemented for fast, simultaneous group carry generation by means of propagate ($\overline{P}$) and generate ($\overline{G}$) carries. When used in conjunction with the F100179 carry-lookahead generator, high-speed arithmetic operations can be performed. Table II presents the equations for internal carry-lookahead and $\overline{C_n + 4}$, $\overline{P}$, $\overline{G}$ for the F100181. Refer to the data sheet on the F100181.

F100179 FUNCTIONAL DESCRIPTION

The F100179 is a high-speed, carry-lookahead generator capable of anticipating a carry across eight 4-bit adders/ALU's. Carry, generate carry, and propagate carry functions are provided to perform full carry-lookahead across n-bit words. Table III presents the four carry output equations. For detailed AC/DC specifications, refer to the F100179 data sheet.

TABLE I. F100181 Carry Output Equations

S_3	S_2	S_1	S_0	F_n Function	G_n (n = 0 to 3)	P_n (n = 0 to 3)	Outputs		
					Internal Signals		$\overline{C_n + 4}$	$\overline{G}$	$\overline{P}$
L	L	L	L	$F_n = A$ Plus B Plus C_n (BCD)	A_nD_n	$A_n + D_n$	$\overline{C}_n + 4$	$\overline{G}$	$\overline{P}$
L	L	L	H	$F_n = A$ Minus B Plus C_n (BCD)	$A_n\overline{B}_n$	$A_n + \overline{B}_n$	$\overline{C}_n + 4$	$\overline{G}$	$\overline{P}$
L	L	H	L	$F_n = B$ Minus A Plus C_n (BCD)	$\overline{A}_nB_n$	$\overline{A}_n + B_n$	$\overline{C}_n + 4$	$\overline{G}$	$\overline{P}$
L	L	H	H	$F_n = 0$ Minus B Plus C_n (BCD)	L	$\overline{B}_n$	$\overline{C}_n + 4$	H	$\overline{P}$
L	H	L	L	$F_n = A$ Plus B Plus C_n (Binary)	A_nB_n	$A_n + B_n$	$\overline{C}_n + 4$	$\overline{G}$	$\overline{P}$
L	H	L	H	$F_n = A$ Minus B Plus C_n (Binary)	$A_n\overline{B}_n$	$A_n + \overline{B}_n$	$\overline{C}_n + 4$	$\overline{G}$	$\overline{P}$
L	H	H	L	$F_n = B$ Minus A Plus C_n (Binary)	$\overline{A}_nB_n$	$\overline{A}_n + B_n$	$\overline{C}_n + 4$	$\overline{G}$	$\overline{P}$
L	H	H	H	$F_n = 0$ Minus B Plus C_n (Binary)	L	$\overline{B}_n$	$\overline{C}_n + 4$	H	$\overline{P}$
H	L	L	L	$F_n = A_nB_n + \overline{A}_n\overline{B}_n$	A_nB_n	$A_n + B_n$	$\overline{C}_n + 4$	$\overline{G}$	$\overline{P}$
H	L	L	H	$F_n = A_n\overline{B}_n + \overline{A}_nB_n$	$A_n\overline{B}_n$	$A_n + \overline{B}_n$	$\overline{C}_n + 4$	$\overline{G}$	$\overline{P}$
H	L	H	L	$F_n = A_n + B_n$	A_n	$\overline{B}_n$	$\overline{C}_n + 4$	$\overline{G}_x$	$\overline{P}$
H	L	H	H	$F_n = A_n$	A_n	H	$\overline{C}_n + 4$	$\overline{G}$	L
H	H	L	L	$F_n = \overline{B}_n$	L	B_n	L	H	$\overline{P}$
H	H	L	H	$F_n = B_n$	L	$\overline{B}_n$	L	H	$\overline{P}$
H	H	H	L	$F_n = A_nB_n$	L	$\overline{A}_n + \overline{B}_n$	L	H	$\overline{P}$
H	H	H	H	$F_n =$ LOW	L	H	L	H	L

H = HIGH Voltage Level
L = LOW Voltage Level

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APPLICATIONS

Logic symbol representations of the F100179 and F100181 are shown in *Figure 1* with propagation delay paths. The times shown are maximum values at nominal room temperature (25°C) and power supply voltage ($V_{EE} = -4.5V$) for a flatpak package. The propagation delays from the select inputs (F100181) are ignored since it is assumed that the mode of operation is set prior to application of the input word operands.

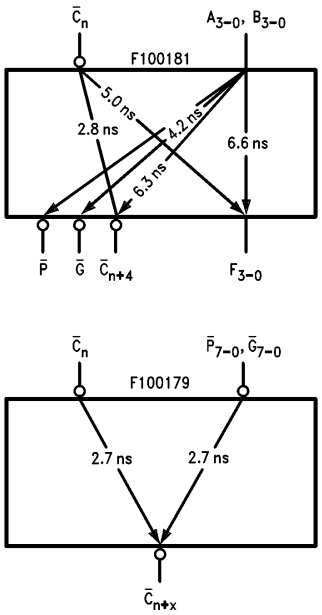

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FIGURE 1. F100179/F100181 Propagation Delays

TABLE II. F100181 Carry Output Equations

$$\overline{P} = \overline{P}_0 + \overline{P}_1 + \overline{P}_2 + \overline{P}_3$$

$$\overline{G} = \overline{G}_3 + P_3G_2 + P_3P_2P_1 + P_3P_2P_1G_0$$

$$\overline{C}_{n+4} = \overline{G} \bullet (\overline{P} + \overline{C}_n)$$

Internal Equations for Carry-Lookahead

(i = 0, 1, 2, 3)

$$C_0 = C_n + S_3$$

$$C_1 = G_0 + P_0C_n + S_3$$

$$C_2 = G_1 + P_1G_0 + P_1P_0C_n + S_3$$

$$C_3 = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n + S_3$$

RIPPLE CARRY CALCULATION

Figure 2 shows the schematic for simple n-stage cascading, incorporating ripple carry. Regardless of the width of the adder, all stages have a sum and carry from the A, B inputs in 6.6 ns. However, this represents the true sum and carry for stage one. For each succeeding stage, the $\overline{C_n}$-to-$\overline{C_{n+4}}$ and $\overline{C_n}$-to-F propagation delays must be considered. Therefore, for n-stages the total settling time for the function outputs during addition is:

$$t_{sum} = t_{[A,\,B,\text{-to-}F]} + (n\text{-}2)\, t_{[\overline{C_n}\text{-to-}\overline{C_{n+4}}]} + t_{[\overline{C_n}\text{-to-}F]}$$

A 32-bit wide adder requires eight stages (n = 8). The propagation time of the operand inputs (A, B) to the function outputs (F) of the first stage is 6.6 ns. The propagation time of the carry input ($\overline{C_n}$) to the function outputs of the last stage is 5.0 ns. Each middle stage has a propagation delay, $\overline{C_n}$ to the carry output ($\overline{C_{n+4}}$), of 2.8 ns. The total settling time of the function outputs is then:

$$t_{sum} = 6.6 + (8\text{-}2)\,(2.8) + 5.0 = 28.4 \text{ ns}$$

Figure 3 shows graphically the settling times of each of the eight stages.

TABLE III. F100179 Carry Output Equations

$$\overline{C}_{n+2} = \overline{G}_1 \bullet (\overline{P}_1 + \overline{G}_0) \bullet (\overline{P}_1 + \overline{P}_0 + \overline{C}_n)$$

$$\overline{C}_{n+4} = \overline{G}_3 \bullet (\overline{P}_3 + \overline{G}_2) \bullet (\overline{P}_3 + \overline{P}_2 + \overline{G}_1) \bullet (\overline{P}_3 + \overline{P}_2 + \overline{P}_1 + \overline{G}_0) \bullet (\overline{P}_3 + \overline{P}_2 + \overline{P}_1 + \overline{P}_0 + \overline{C}_n)$$

$$\overline{C}_{n+6} = \overline{G}_5 \bullet (\overline{P}_5 + \overline{G}_4) \bullet (\overline{P}_5 + \overline{P}_4 + \overline{G}_3) \bullet (\overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{G}_2) \bullet (\overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{P}_2 + \overline{G}_1) \bullet (\overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{P}_2 + \overline{P}_1 + \overline{G}_0) \bullet (\overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{P}_2 + \overline{P}_1 + \overline{P}_0 + \overline{C}_n)$$

$$\overline{C}_{n+8} = \overline{G}_7 \bullet (\overline{P}_7 + \overline{G}_6) \bullet (\overline{P}_7 + \overline{P}_6 + \overline{G}_5) \bullet (\overline{P}_7 + \overline{P}_6 + \overline{P}_5 + \overline{G}_4) \bullet (\overline{P}_7 + \overline{P}_6 + \overline{P}_5 + \overline{P}_4 + \overline{G}_3) \bullet (\overline{P}_7 + \overline{P}_6 + \overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{G}_2) \bullet (\overline{P}_7 + \overline{P}_6 + \overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{P}_2 + \overline{G}_1) \bullet (\overline{P}_7 + \overline{P}_6 + \overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{P}_2 + \overline{P}_1 + \overline{G}_0) \bullet (\overline{P}_7 + \overline{P}_6 + \overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{P}_2 + \overline{P}_1 + \overline{P}_0 + \overline{C}_n)$$

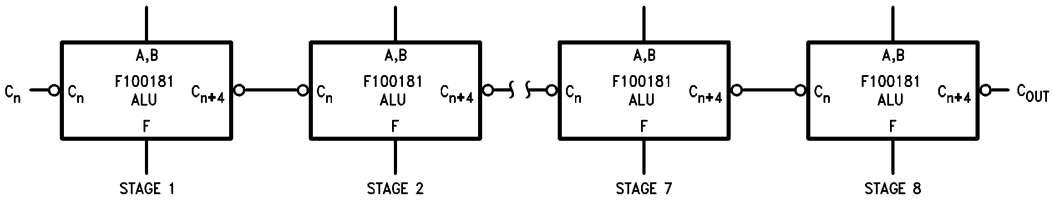

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FIGURE 2. Ripple Carry

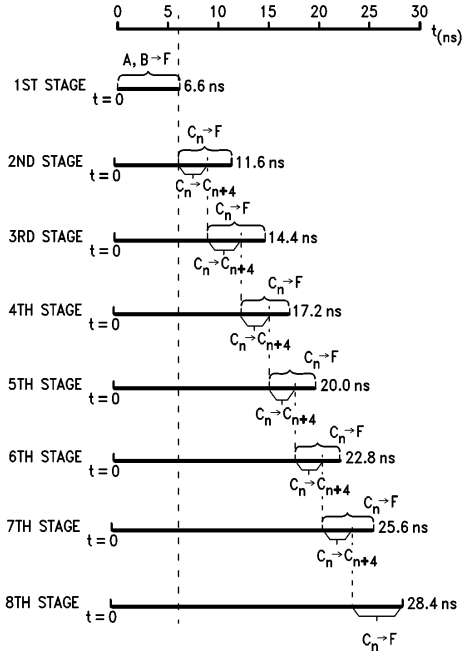

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FIGURE 3. Timing Line Diagram for 32-Bit ALU

1-LEVEL CARRY-LOOKAHEAD CALCULATION

Figure 4 shows a 16-bit adder using one level of carry-lookahead for every two ALU's. The reason for this arrangement is that the F100179 does not provide every $\overline{C_{n+x}}$, but instead provides $\overline{C_{n+2}}$, $\overline{C_{n+4}}$, $\overline{C_{n+6}}$, and $\overline{C_{n+8}}$. One F100179 is capable of providing carry-lookahead for 32 bits. The timing line diagram for the 16-bit ALU with one level of carry-lookahead is given in *Figure 5*. The equation which describes each 32-bit stage is given by:

$$t_{sum} = t_{[A,B\text{-to-}P,G]} + t_{[\overline{C_n}\text{-to-}F]} + t_{[\overline{C_n}\text{-to-}\overline{C_{n+4}}]} + t_{[P,G\text{-to-}\overline{C_{n+2}}]}$$

To expand this scheme past 32 bits (eight ALU's) requires that the adder be broken into 32-bit groups connected with ripple carries since group generate and propagate are not available from the F100179. Each 32-bit group past the first one adds one F100179 P, G-to-$\overline{C_{n+x}}$ time to establish the carry into the next 32-bit group. *Figure 6* shows this method of interconnection.

FAST 16-Bit 1-Level Carry-Lookahead

Another method for implementing a 16-bit adder with faster carry propagation is shown in *Figure 7*. In this example, the full capability of the F100179 is used by forcing carry propagation through the odd-order stages. The carry outputs, $\overline{C_{n+x}}$, are then used to supply the appropriate carry bit to succeeding stages. The equation describing the critical path becomes:

$$t_{sum} = t_{[A,B\text{-to-}P,G]} + t_{[P,G\text{-to-}\overline{C_{n+x}}]} + t_{[\overline{C_n}\text{-to-}F]}.$$

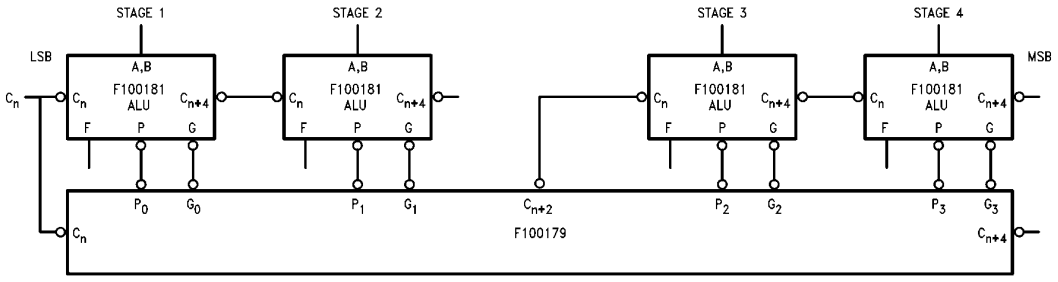

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FIGURE 4. 1-Level Carry-Lookahead

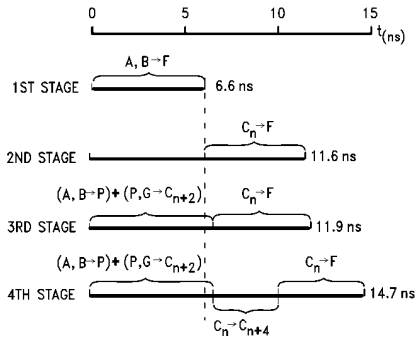

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FIGURE 5. Timing Line Diagram for 16-Bit ALU with 1-Level Carry-Lookahead

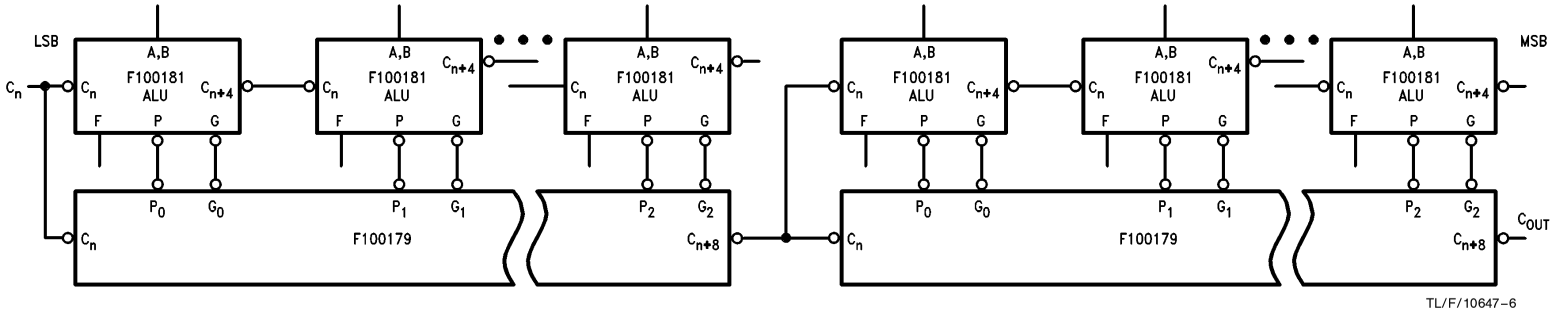

FIGURE 6. Expansion Past 32 Bits for 1-Level Carry-Lookahead

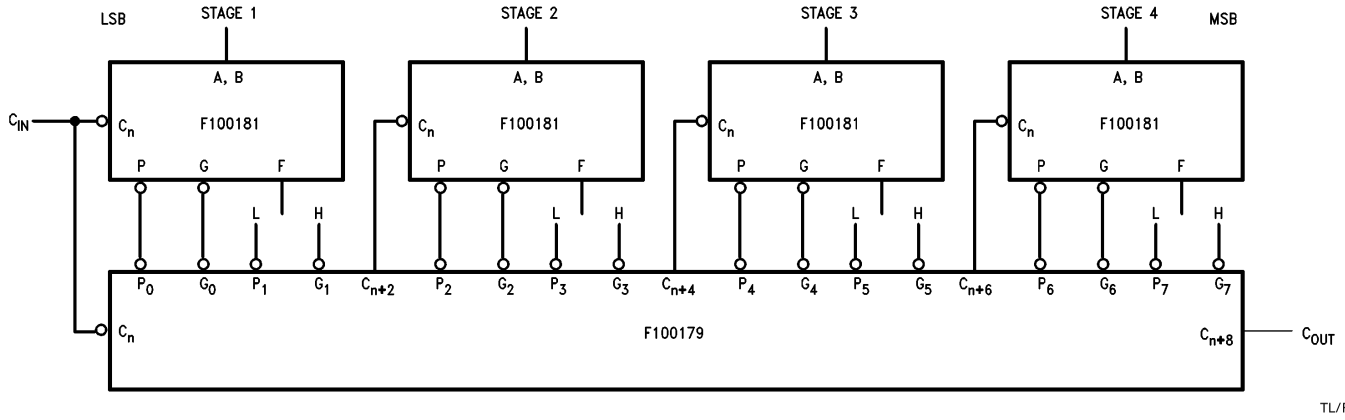

FIGURE 7. Fast 16-Bit 1-Level Carry-Lookahead

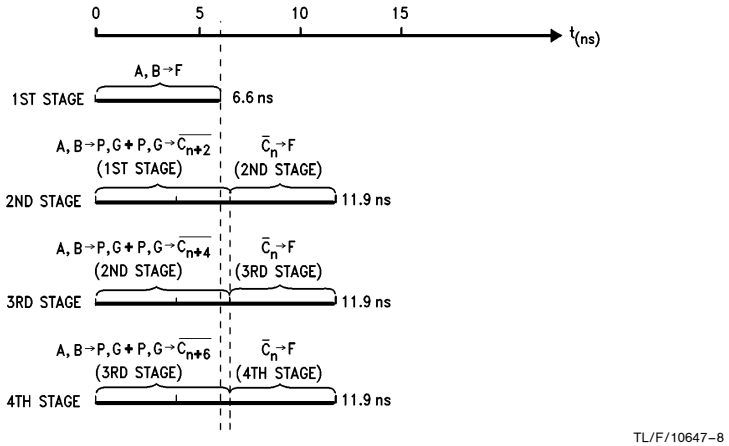

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FIGURE 8. Timing Line Diagram For Fast 16-Bit 1-Level Carry-Lookahead

TWO-LEVEL CARRY-LOOKAHEAD CALCULATION

The word widths of 32 bits or more, a two-level carry-lookahead scheme like that shown in *Figure 9* is preferred. One of the two F100179's generates a carry for the even-numbered ALU's; the other generates a carry for the odd-numbered ALU's. The timing line diagram for this method is given in *Figure 10*. The equation describing the 32-bit summation is:

$$t_{sum} = t_{[A,B,\text{-to-}P,G]} + t_{[P,G\text{-to-}C_{n+x}]} + t_{[C_n\text{-to-}F]}$$

This scheme can be expanded past 32 bits as in the previous case by interconnecting 32 bit groups with ripple carries. Each 32-bit group past the first adds one $t_{[P,G\text{-to-}\overline{C_{n+x}}]}$ delay to the total add time. Table IV summarizes the add times for all three schemes discussed in this application note.

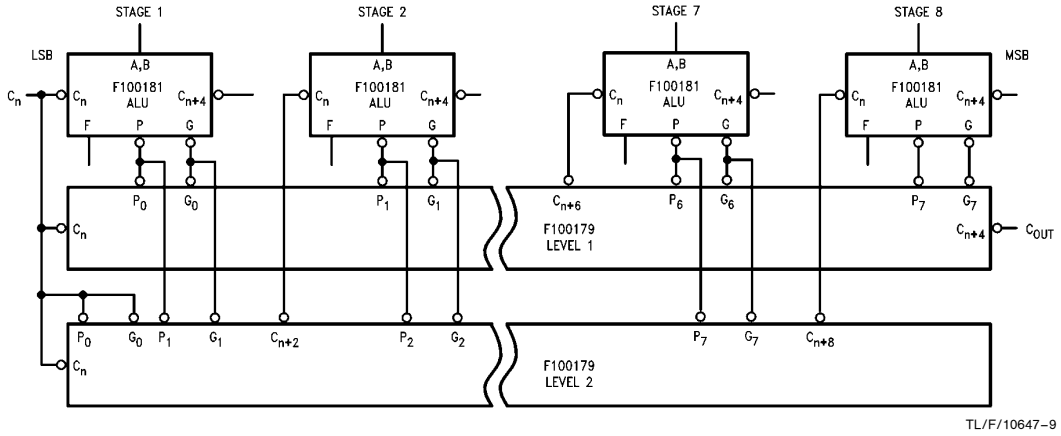

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FIGURE 9. 2-Level Carry-Lookahead

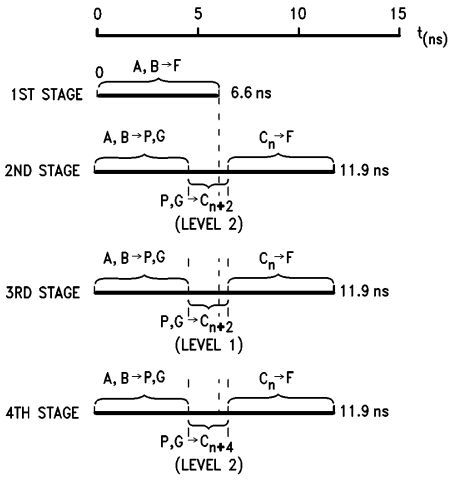

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FIGURE 10. Timing Line Diagram for 32-Bit ALU with 2-Level Carry-Lookahead

TABLE IV. Summary of Add Times

Bits	Stages	with Ripple Carry (ns)	with (1) F100179 (ns)	with (2) F100179 (ns)
8	2	11.6	n/a	n/a
16	4	17.2	14.7	11.9
32	8	28.4	14.7	11.9
64	16	50.8	17.4	14.6

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