

# The Super I/O Demo Board User's Guide

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## BACKGROUND

The PC87310 integrates two UARTs, a floppy disk controller with analog data separator, one parallel port, game port decode, hard disk controller decode, and standard PC-XT®/AT® address decode into one single chip. This chip can be used in the PC-XT or AT application which typically implements these functions separately. By using the PC87310, it significantly reduces the total chip count of the system and increases the overall reliability compared to implementing the same functions with multiple controller chips and glue logic.

## INTRODUCTION

This guide describes a design that uses the PC87310 (Super I/O) to implement the serial port, parallel port, floppy disk, game port, and hard disk interfaces in PC-AT environment. It includes an overview of the board, configuration information, schematics, a board floor plan and a listing of the available test software. For detailed information on the PC87310, refer to the data sheet.

## DEMO BOARD FEATURES

**1. IDE Hard Disk Interface:** The hard disk interface requires only a 20L8 PAL (U35), two buffers (74LS244 and

74LS125, U8 and U11), and two data transceivers (74LS245, U2 and U3). The PAL generates the read and write enable strobes for data bit 7 (D7) as well as the data transceiver gate controls for data bits D0–D6 and D8–D15. If the hard disk is an IDE (Integrated Drive Electronics) hard drive such as the Connor Peripherals CP3024, then no other circuitry is needed to interface the drive. (Table I lists the PAL equations.)

**2. Bidirectional Parallel Port Control:** The parallel port on the PC87310 is bidirectional and the control of data transfer direction is done by the  $\overline{POE}$  pin. In the PC application, the parallel port is usually configured as an output port which requires  $\overline{POE}$  to be tied low. Switch SWB-4 is used to configure the parallel port to function as either an input or an output port.

**3. PC-XT and PC-AT Game Port Support:** Although this board design mainly targets the PC-AT implementation of the game port, the PC87310 does provide the required game port interface signals (game port read and write strobes) for the PC-XT environment. Switches SWB-1, SWB-2, and SWB-3 determine how the read and write strobes are generated depending on which machine (XT or AT) this board is plugged into.

TABLE I. PAL Equations

Device: P20L8

### Inputs

$V_{CC}$ , GND	Pin 24, 12;
RESET, $\overline{IO16CS}$ , $\overline{HCS0}$ , $\overline{HCS1}$	Pin 1, 2, 3, 4;
$\overline{IOR}$ , $\overline{IOW}$ , A0	Pin 5, 6, 7;
A10, A11, A12	Pin 8, 9, 10;
A13, A14, A15, EN	Pin 11, 13, 14, 23;

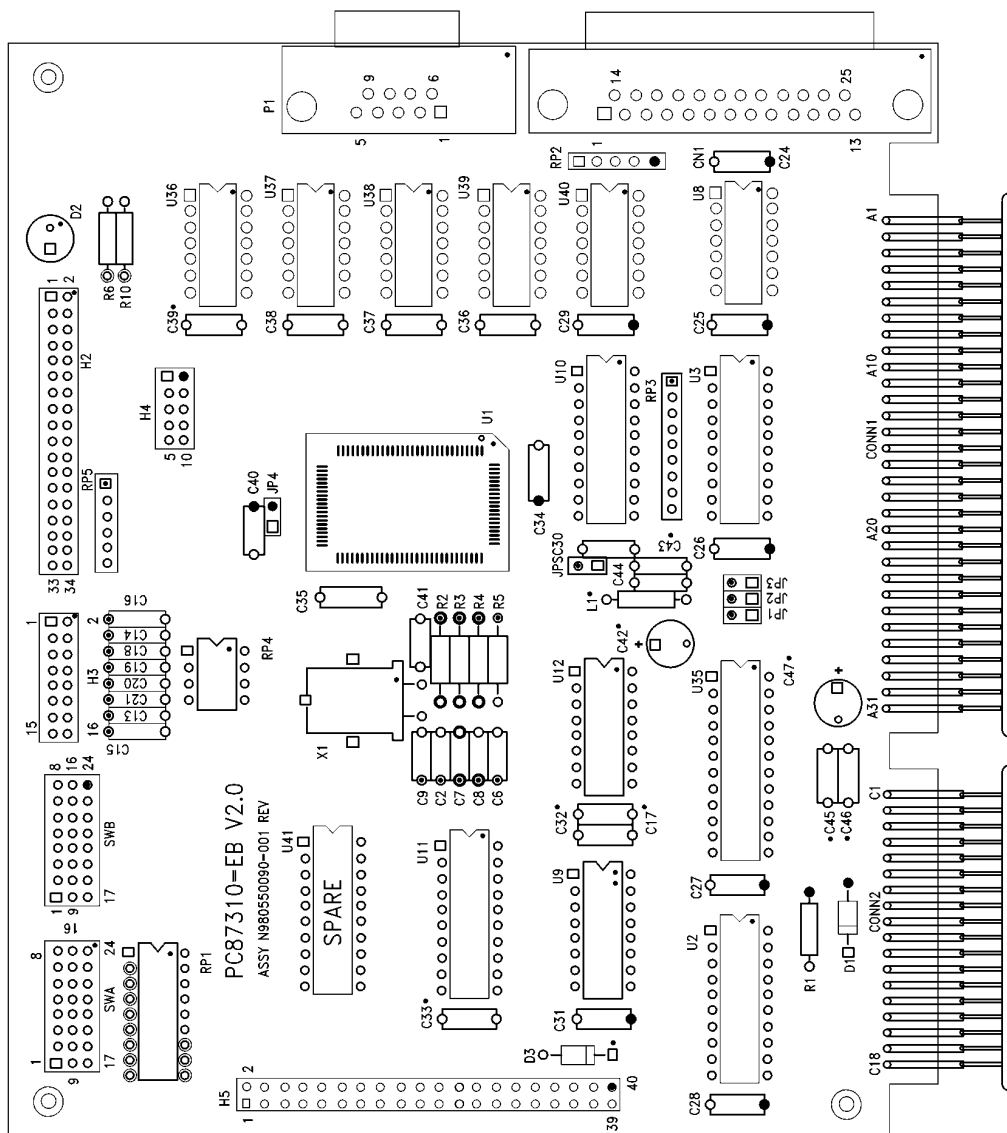
### Outputs

$\overline{RESET}$	Pin 15;
$\overline{D7WR}$ , $\overline{D7RD}$	Pin 18, 19;
$\overline{ENLO}$ , $\overline{ENHI}$	Pin 20, 21;
$\overline{IOL}$	Pin 22;

### Equations:

$\overline{RESET} = !(\text{RESET})$   
 $\overline{D7RD} = !(EN * (!\overline{IOR} * !\overline{HCS0}))$   
 $\overline{D7WR} = !(EN * (!\overline{IOW} * ((!\overline{HCS1} * !A0) + !\overline{HCS0})))$   
 $\overline{ENHI} = !(EN * ((!\overline{IO16CS} * !\overline{HCS0}) * (!\overline{IOR} + !\overline{IOW})))$   
 $\overline{ENLO} = !(EN * ((!\overline{HCS0} * (!\overline{IOR} + !\overline{IOW}) + (!\overline{HCS1} * ((A0 * !\overline{IOR}) + (!A0 * !\overline{IOW}))))))$   
 $\overline{IOL} = !(A10 * A11 * A12 * A13 * A14 * A15)$

# PC87310EB—Super I/O Evaluation Board Layout



## HARDWARE CONFIGURATION

The major functions of the PC87310 can be enabled/disabled via hardware or software. Each hardware Configuration pin is associated with a bit in the Configuration Register. The logic state on the  $\overline{\text{CRPE}}$  pin determines whether the default of the register will be 00 or a value latched in during reset from the hardware configuration pins. For hardware configuration, the  $\overline{\text{CRPE}}$  (SWA-8) is set to low. In addition, the complement of the logic states on  $\overline{\text{CRB0}}\text{--}\overline{\text{CRB7}}$  pins (SWA1–7) are latched into the Configuration Register upon system reset. Depending on the value loaded into the register, each function can then be disabled/enabled. Configuration Register bit 5 cannot be controlled via external hardware and always resets to the enabled (0) state.

## SOFTWARE CONFIGURATION

The Configuration Register on the PC87310 (U1) allows all or part of the functions to be enabled/disabled via software. When  $\overline{\text{CRPE}}$  pin is tied high (SWA-8), two consecutive

writes to the Configuration Register (I/O address 3F3 hex) are required to disable the desired functions after system reset. The second I/O write to the Configuration Register should be the correct bit pattern for programming the register and there should be no I/O write strobes between these two I/O writes to 3F3 hex. The best way to guarantee a correct bit pattern written to the Configuration Register is to disable the system interrupts before the two I/O writes and re-enable the interrupts right after performing I/O writes.

## SWITCHES AND JUMPERS

Switches SWA (8 positions) and SWB (8 positions), and Jumpers JP1–JP5 are used to configure the Super I/O for flexible testing purposes. Jumpers 1, 2, and 3 are for enabling or disabling IRQ 3, 4, and 7 respectively. Jumpers 4 and 5 are for the convenience of power consumption measurement. However, JP1–JP5 may not necessarily be required. Table II summarizes the functions of all switches and jumpers.

**TABLE II. PC87310EB—Switch and Jumper Selections**

**SWA—** Leftmost position is SWA-1, counting up to rightmost position SWA-8. The top switch position “+” connects a pull-up resistor to the pin, the bottom position “–” connects a pull-down resistor to the pin. Note: During a chip reset, the Configuration Register latches in the complement of the  $\overline{\text{CRBx}}$  when  $\overline{\text{CRPE}}$  is low. That is, the “+” position is a logical 0, and the “–” position is a logical 1 for each configuration bit. See the PC87310 data sheet for a complete description of each configuration bit.

Switch	Desc	+	–
SWA-1	$\overline{\text{CRB7}}$	Decoded FDC Drive Selects	Encoded FDC Drive Selects
SWA-2	$\overline{\text{CRB6}}$	FDC Enable	FDC Disable
SWA-3	$\overline{\text{CRB4}}$	0	1
SWA-4	$\overline{\text{CRB3}}$	0	1
SWA-5	$\overline{\text{CRB2}}$	0	1
SWA-6	$\overline{\text{CRB1}}$	0	1
SWA-7	$\overline{\text{CRB0}}$	0	1
SWA-8	$\overline{\text{CRBE}}$	Automatic Configuration	Hardware Configuration

**Note 1:**  $\overline{\text{CRB4}}\text{--}2$  are used to configure UART1 and UART2.

**Note 2:**  $\overline{\text{CRB1}}\text{--}0$  are used to configure Parallel Port.

**SWB—** Leftmost position is SWB-1, counting up to rightmost position SWB-8. The top switch position will be referenced as “+”, and the bottom switch position will be referenced as “–”.

Switch	Desc	+	–
SWB-1	$\overline{\text{XTSEL}}$	AT Mode	XT Mode
SWB-2	Game Read	AT Mode	XT Mode
SWB-3	Game Write	AT Mode	XT Mode
SWB-4	Parallel Write	High Z Inputs	Printer Port Outputs
SWB-5	Drive Type	High	Low
SWB-6	Precomp	Alternate	Normal
SWB-7	—	—	—
SWB-8	IDE ckt.	Enable	Disable

## JUMPERS

### JP1— IRQ3 Enable.

**ON—** IRQ3 interrupt signal connected to AT bus.

**OFF—** IRQ3 interrupt signal disconnected from AT bus.

### JP2— IRQ4 Enable.

**ON—** IRQ4 interrupt signal connected to AT bus.

**OFF—** IRQ4 interrupt signal disconnected from AT bus.

### JP3— IRQ7 Enable.

**ON—** IRQ7 interrupt signal connected to AT bus.

**OFF—** IRQ7 interrupt signal disconnected to AT bus.

### JP4— Digital $V_{CC}$ Enable.

**ON—** Digital  $V_{CC}$  inputs to PC87310 connected to AT bus +5V signal.

**OFF—** Digital  $V_{CC}$  inputs to PC87310 disconnected from AT bus +5V signal.

**JP5— Analog V<sub>CC</sub> Enable.**

**ON—** Analog V<sub>CC</sub> to FDC data separator section connected to output of +5V voltage regulator.

**OFF—** Analog V<sub>CC</sub> to FDC data separator section disconnected from output of +5V voltage regulator.

**CONNECTORS**

**P2—** DB25 Parallel Connector for Parallel Port (Printer).

**P1—** DB9 Serial Connector for UARTs.

**HEADERS**

**H2—** 34 pin Floppy Disk Drive Interface Connector. Connect pin 1 of cable to right side of header.

**H3—** 16 pin Game Port Connector. Connect pin1 of cable to right side of header.

**H4—** 10 pin UART Serial Connector. Tied to transceivers on the PC87310EB, which are connected to P1.

**H5—** 40 pin Enhanced Hard Disk Interface Connector. Connect pin 1 of cable to right side of header.

**TEST PROGRAMS**

Programs written in Assembly and C are available to carry out the functional evaluation of the PC87310. These programs have been tested successfully on the demo board. Some of the programs may require a loopback connector to continue the test. The configuration of those loopback connectors are detailed in Table III. (Table IV lists the available programs.) DP8473 demo program can also be used for diagnostic purposes.

**TABLE III. Loopback Connector Configuration**

Parallel Port Loopback Connector (25 Pins) Configuration			
Pin No.	Signal Name	Pin No.	Signal Name
14	AFD	15	ERROR
17	SLIN	13	SLCT
16	INIT	12	PE
1	STB	10	ACK
		11	BUSY

**Note:** Pin 1 is connected to pin 10 and pin 11.

**TABLE IV. Test Programs for the Super I/O PC87310**

Program	Description
451.EXE	Parallel Port Functionality Test
COMTEST.EXE	Serial Port Functionality Test
ACT.EXE	Full Duplex Asynchronous Test for Serial Port
120.EXE	Floppy Disk Controller Functionality Test for 1.2M Drive
360.EXE	Floppy Disk Controller Functionality Test for 360K Drive
FLOPPY.EXE	Floppy Disk Controller Demo Program

The test and demo programs mentioned in this user's guide, along with the appropriate C and assembly source code files, are available on National's Bulletin Board System. The Bulletin Board System is a service provided by the PC Peripherals Applications Group. It provides access to an automated information storage and retrieval system that may be accessed over standard dial-up telephone lines 24 hours a day.

The system's capabilities include a MESSAGE SECTION (electronic mail) for communicating to and from the PC Peripherals Applications Group and a FILE SECTION mode that can be used to search out and retrieve application data about NSC UARTs, Floppy Disk Controllers and High Integration Peripherals. The minimum system requirement: 1. A dumb terminal. 2. A 300 or 1200 baud modem. 3. A telephone. The modem is set up at 1200 baud, no parity, 8 data bits, 1 stop bit, and full duplex communication environment. With a communication package and a PC, the files mentioned in this design guide can be downloaded from the FILE SECTION to disk for later use.

The phone number for the PC Peripherals Apps BBS is (408) 245-0671.

**BOARD LAYOUT**

All of the circuitry can be implemented on a half size adapter. This demonstrates how the Super I/O can save in terms of the total board space and weight. (Table V lists components used in these demo boards.)

**TABLE V. The Super I/O PC87310EB Demo Board Part List**

Part ID	Part Description	Part ID	Part Description
C2, R2	Not Used	C6	1000 pF
C7	0.027 $\mu$ F	C8, 44	0.047 $\mu$ F
C9	15 pF	C13, 14, 15, 16	51 pF
C17–C21	0.01 $\mu$ F	C24–C39	0.01 $\mu$ F
C40	0.1 $\mu$ F	C41	10 pF
C42	22 $\mu$ F	C43, 46	0.1 $\mu$ F
C45	0.01 $\mu$ F	C47	10 $\mu$ F
P2	DB25 Female	P1	DB9 Male
D1, 3	1N914	D2	LED, RED
H2	Header 17 x 2	H3	Header 8 x 2
H4	Header 5 x 2	H5	Header 20 x 2
JP1–5	Jumper	L1	2.8 mH
R1	1K	R3, 4	560
R5	5.5K	R6	330
R10	10K	RP1	10K—DIP 16 Pins
RP2	4.7K—SIP 5 Pins	RP3	1K—SIP 9 Pins
RP4	2.2K—DIP 8 Pins	RP5	150—SIP 6 Pins
SWA	Jumper, 8 x 3	SWB	Jumper, 8 x 3
U1	PC87310	U2, 3	74LS245
U8	74LS125	U9	74LS32
U10, 11	74LS244	U12	NE558
U35	PAL, 20L8	U36, 40	1488
U37, 38, 39	1489	X1	24 MHz

## The Super I/O Demo Board Design Considerations

### I/O ADDRESS

Since the Super I/O incorporates the standard PC-XT and AT decode logic, this demo board supports the I/O addresses used in the PC-XT and AT for the serial port, parallel port, game port, floppy disk controller and hard disk. The PC-AT uses partially decoded address lines for accessing I/O ports (A10–A15 are not decoded), but the PS/2 systems fully decode all the address lines for the I/O ports. So, it is required to generate an active low signal to the  $\overline{\text{IOL}}$  input when A0–A15 are all low. When the  $\overline{\text{IOL}}$  is tied high, the on-board address decoder is being disabled. This function has been incorporated into the 20L8 PAL (U35). The AEN input is used to differentiate between a DMA access and a CPU access. (Table VI lists the I/O addresses the demo board supports.)

TABLE VI. I/O Address Decode

Address Range	Function
278–27F	Parallel Port 3
378–37F	Parallel Port 2
3BC–3BE	Parallel Port 1
3F8–3FF	Serial Port 1
2F8–2FF	Serial Port 2
320–324 (HCS0 Active)	Hard Disk Select for PC-XT
1F0–1F7 (HCS0 Active), (HCST Active)	Hard Disk Select for PC-AT
3F0–3F7	Floppy Disk
201	Game Port Select
3F3	Configuration Port

**Note 1:** 3F7H: Read D7 from FDC, D0–D6 from HDD; Write D0–D7 to FDC.

**Note 2:** Configuration Port is a Write-Only register that requires two writes to change the data.

### SERIAL AND PARALLEL INTERFACES

Since there is only one serial connector that can be physically located on the board, only one serial port can talk to another system via this connect. Serial channel 1 is chosen to communicate with the outside world via the serial connector. Additional RS232 line driver and receivers are provided for the second serial channel. This channel, presented at connector H4, can then directly drive an off-board DB9 connector. The RS-232 line driver and receivers, 1488 (U40) and 1489 (U38, U39), support the high speed transfer through the commercially available communication programs. The parallel port interface is straightforward. The only additional parts required are the 4.7 k $\Omega$  pull-up resistors on the printer control signals. This parallel port is a standard PC, PC-XT and PC-AT compatible parallel port. It can also be used as an input port and is therefore bidirectional.

### GAME PORT INTERFACE

The Super I/O supports two modes of operation (XT and AT modes) for interfacing with the game port. In the XT mode, two game port signals, GRD and GWR, are provided. In the AT mode, only  $\overline{\text{GPE}}N$  is provided. In order to generate the read and write strobe in the AT mode, the read and write strobes must be provided externally to the chip. A 74LS32 (U9) is used to gate  $\overline{\text{GPE}}N$  with CPU read and write strobes to generate game port read and write strobes. Switches SWB-1, SWB-2, and SWB-3 are used to select how the game port control signals are generated. To set it up in the AT mode, they are all connected to “+”, whereas in the XT mode they are all connected to “–”.

### FLOPPY DISK INTERFACE

The Super I/O provides all floppy disk control signals for the standard interface cable. The only additional circuit components needed are the pull-up resistors (150 $\Omega$ ) on the floppy disk interface input pins and the data separator filter components. The floppy disk controller is totally compatible with the  $\mu$ PD765A and the DP8473. It also includes enhanced features such as 1.0 Mb/s data rate support, extended track range to 4096, Implied Seeks, working Scan Commands, and standard IBM disk format as well as Sony ISO format support.

### HARD DISK INTERFACE

The PC87310 Super I/O controller is designed to provide a higher level of integration when interfacing to commonly used peripherals such as a floppy disk drives and communications ports. Another key interface design that is facilitated through use of the PC87310 is the **IDE** Hard Disk interface. The Super I/O provides the two hard disk chip selects required for this interface. Using the Super I/O, only five other chips (U2, U3, U8, U11, U35) are required to construct the IDE Hard Disk Interface circuit (See *PC87310EB Schematic*). The circuit shown provides the address decoding, buffers, and control and data signals for the hard disk IDE interface.

The IDE interface is essentially the AT bus ported to the hard drive. The hard disk controller resides on the hard drive itself. So the IDE interface circuit must provide the AT bus signals, including data bits D15–D0, address lines A3–A0, as well as the common control signals. These signals are contained on the 40-pin IDE interface header (See *Schematic*).

When in the PC-AT mode, the PC87310 Super I/O controller provides the two hard disk chip selects for the IDE interface. The  $\overline{\text{HCS}}0$  output is active low when the 1F0–1F7 (hex) I/O address space is chosen and corresponds to the 1FX signal on the IDE header. The  $\overline{\text{HCS}}1$  output is active low when the 3F6 or 3F7 I/O addresses are chosen, and corresponds to 3FX on the IDE header. These are the two address blocks used in the PC-AT hard disk controller. The table below summarizes the addresses used by the PC-AT hard disk controller.

Looking at the IDE interface circuit in more detail, the LS244 (U11) provides buffering of the control and address lines.

The 20L8 PAL (U35) provides the necessary control signals to enable the data lines for the correct addresses. These four control signals,  $\overline{\text{ENHI}}$ ,  $\overline{\text{ENLO}}$ ,  $\overline{\text{D7RD}}$ , and  $\overline{\text{D7WR}}$  are active low based on the PAL equations shown in Table I.

To summarize the function of these PAL control signals,  $\overline{\text{ENHI}}$  enables the LS245 (U2) octal bus transceiver for the upper data lines (D15–D8) for 16-bit read and write operations at addresses 1F0–1F7.  $\overline{\text{ENHI}}$  will activate the LS245 (U2) only if the  $\overline{\text{IOCS16}}$  output from the hard drive is active.

$\overline{\text{ENLO}}$  enables the other LS245 (U3) octal bus transceiver for the lower data lines (D6–D0) for 1F0–1F7 reads and writes, and for 3F6 writes and 3F7 reads. In addition, the  $\overline{\text{D7RD}}$  and  $\overline{\text{D7WR}}$  control lines from the PAL insure that the D7 data line is disabled for address 3F7 (this bit is used for the Disk Changed register on the floppy disk controller). The two LS245 chips are used to enable or tri-state these data signals. The LS125 (U8) is used to buffer or tri-state the D7 data line and the  $\overline{\text{HCS0}}$  chip select.

**PC-AT Hard Disk Controller Registers**

Address	Read Function	Write Function
1F0	Data Register	Data Register
1F1	Error Register	Write Precomp Register
1F2	Sector Count	Sector Count
1F3	Sector Number	Sector Number
1F4	Cylinder Low	Cylinder Low
1F5	Cylinder High	Cylinder High
1F6	SDH Register	SDH Register
1F7	Status Register	Command Register
3F6	Not Used. Data Bus TRI-STATE®	Digital Output Register
3F7	Drive Address Register (Note)	Not Used. Data Bus TRI-STATE

**Note:** Data bit D7 is used by the Floppy Disk Controller at address 3F7. D7 must be at TRI-STATE by the IDE interface circuit at this address.

#### CRYSTAL CIRCUIT DESIGN

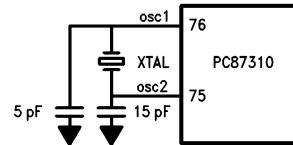
To assure proper operation, use the following recommendation to choose a crystal:

1. 24 MHz Fundamental mode, parallel resonant, HC/33 or HC/4x size crystal enclosure.
2. ESR (Effective Series Resistance) < 40Ω.
3. Shunt capacitance < 7 pF.
4. Avoid low-profile or surface mount XTAL with large “start-up” ESR values.

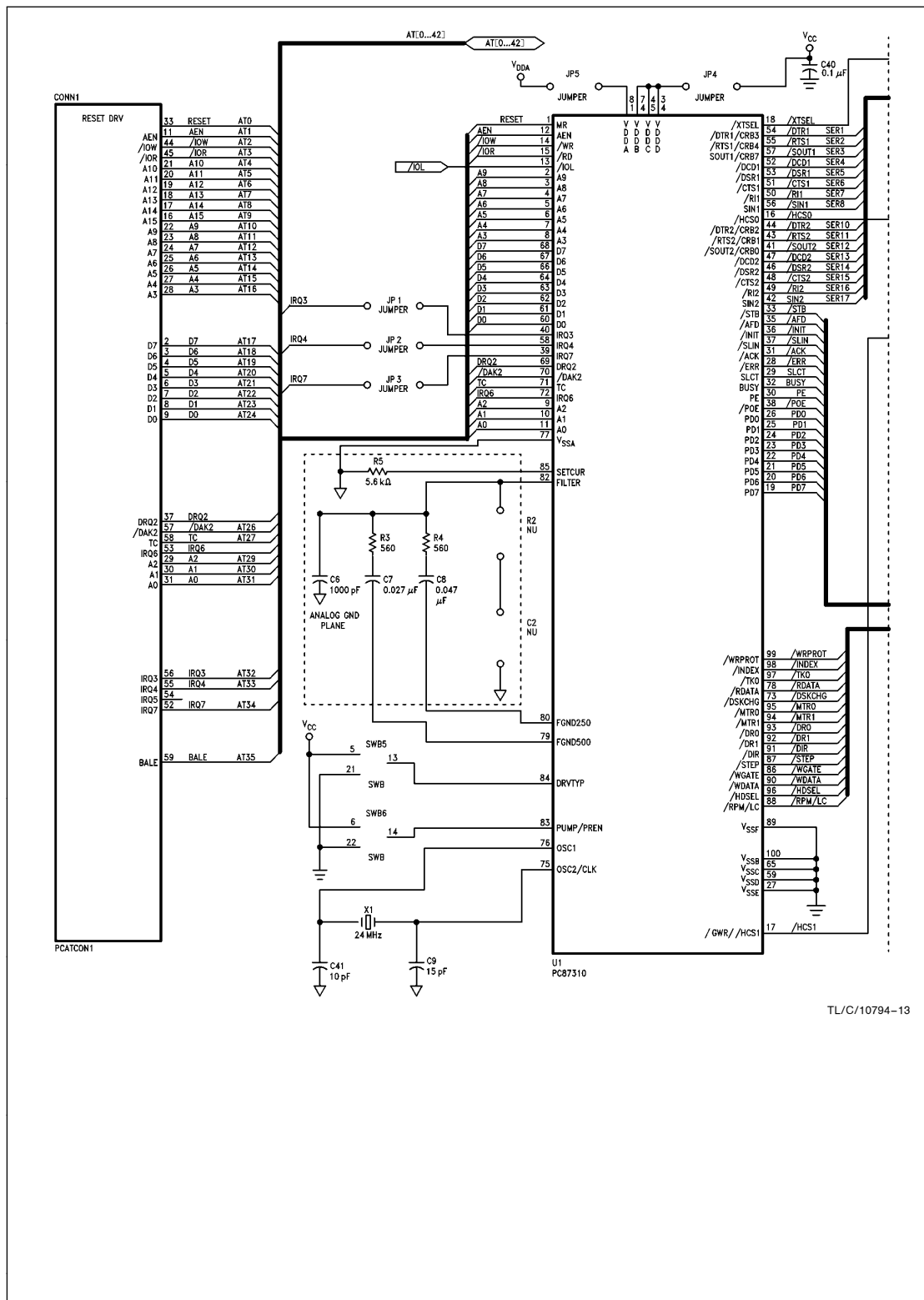
#### 5. Recommended XTAL part numbers:

Vendor	Part Number
Saronix	SRX3164
NEL	C2800N (NE-18A/24 MHz Type)
NEL	54024-2 (NE-18A/24 MHz Type)

#### 6. Recommended XTAL Circuit:

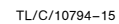


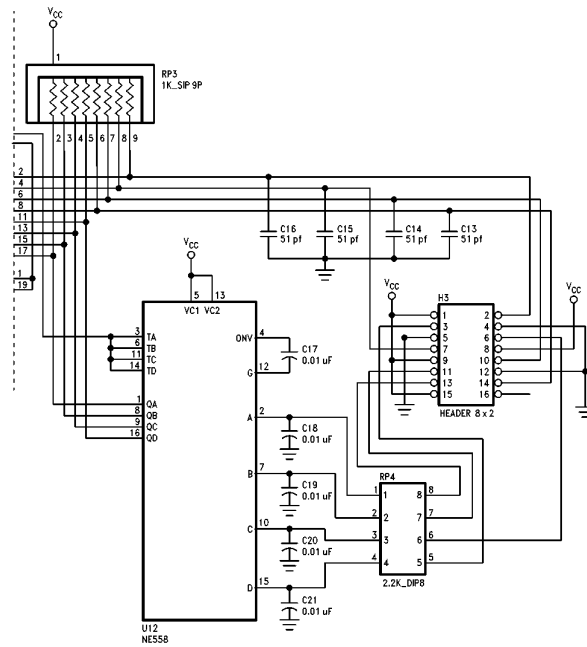
TL/C/10794–12



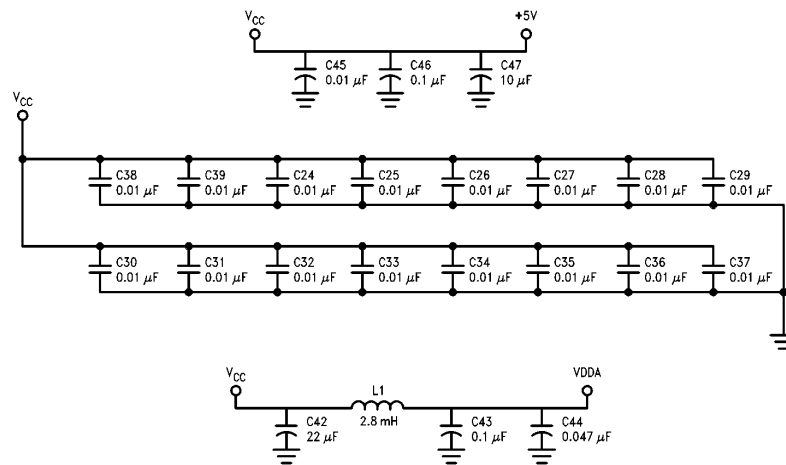
TL/C/10794-13



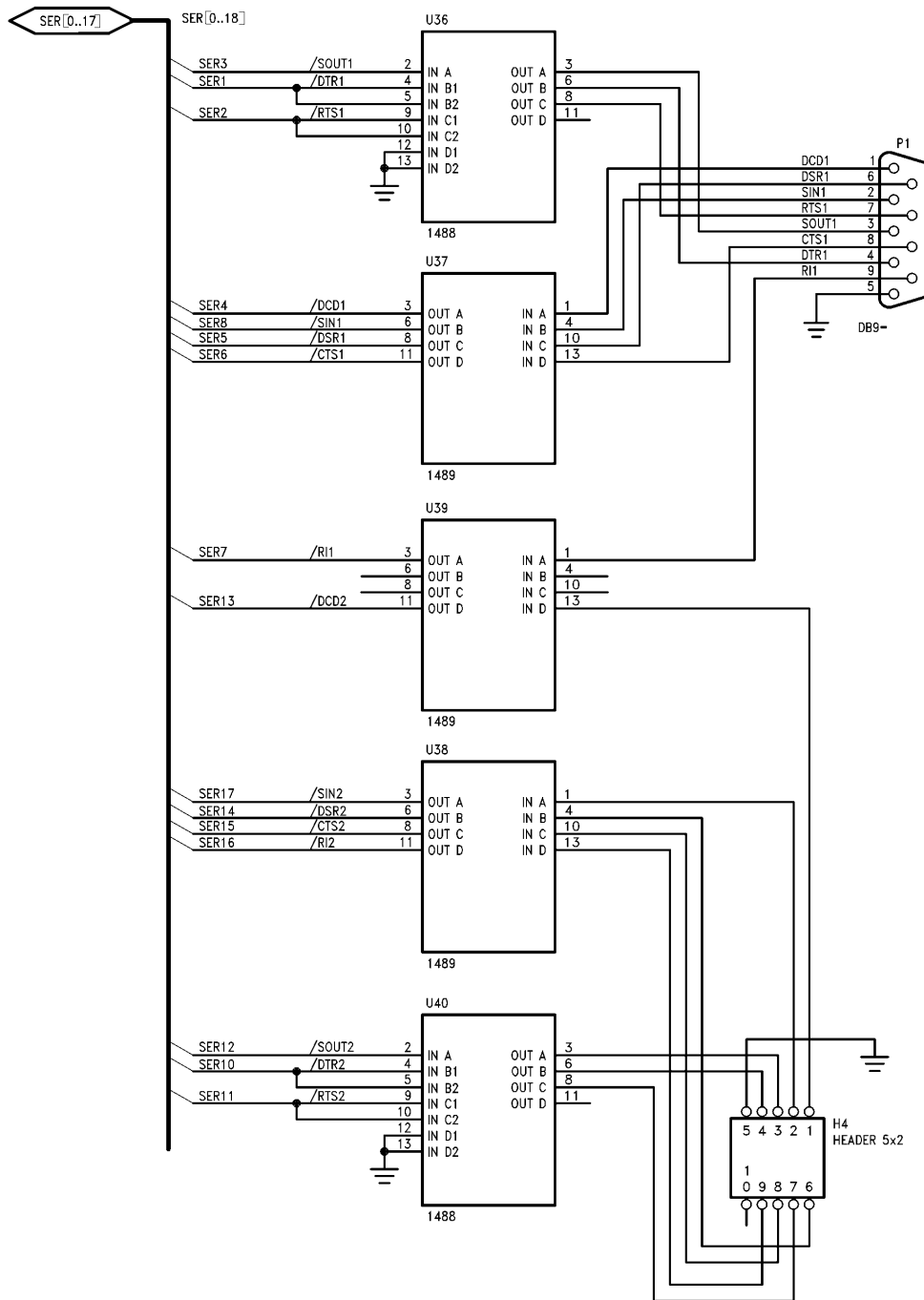




TL/C/10794-16



TL/C/10794-17



TL/C/10794-18

## Four Drive Support with the PC87310 Super I/O Controller

### INTRODUCTION

In most PC-AT systems, a configuration of two floppy disk drives is sufficient. A typical setup would enable the user to access 5.25" and 3.5" media, in either high or low density. In some situations however, it is necessary to support a combination of up to four floppy drives and floppy-compatible tape drives. An example of this situation would be a 1.2 Mb drive (5.25" high density), 360 kB drive (5.25" low density), and 1.44 Mb drive (3.5" dual density) in a system. Also, you could add a floppy-compatible tape drive for backup purposes, making a total of four floppy-compatible devices hooked up to one floppy disk controller. This setup would enable the user to transfer between high and low density media in both 5.25" and 3.5" disks, as well as back-up any hard disk files on tape.

This application note shows the PC87310 Super I/O controller supporting up to four floppy disk drives or floppy compatible tape drives in a system. The operation of the Super I/O when in this four drive support mode is explained. In addition, the circuit required to support four drives, as well as the extended BIOS needed for PC-AT systems will be discussed.

### SUPER I/O DRIVE CONTROL OPTIONS

The PC87310 Super I/O controller has fully decoded drive and motor select outputs that will support up to two floppy disk drives or floppy compatible tape drives. This configuration is fine for most applications, which do not require more than two floppy drives. In this case, the drive and motor select outputs from the Super I/O can be connected directly to the floppy disk interface cable.

The standard PC-AT BIOS will support a maximum of two floppy drives. So if you are designing a motherboard or adapter card using the Super I/O for a standard PC-AT application with two floppy drives, simply use the decoded drive and motor select outputs of the Super I/O. To select

the decoded drive control outputs of the Super I/O, see the description below.

In some cases however, it may be necessary to support up to four floppy disk or tape drives. The Super I/O is fully capable of supporting up to four floppy disk drives if it is configured for encoded drive and motor select outputs. The encoded drive and motor select signals are output on the DR1, DR0 and MTR1, MTR0 pins respectively.

### SELECTING ENCODED OR DECODED DRIVE CONTROL OUTPUTS

The encoded or decoded drive and motor select outputs can be configured with either hardware or software. During a hardware reset, the  $\overline{CRB7}$  signal (pin 57) of the PC87310 should be pulled high or low with a 10 k $\Omega$  resistor. The pull-up or pull-down on  $\overline{CRB7}$  will set up the drive control outputs as decoded or encoded drive and motor selects respectively as long as  $\overline{CRPE}$  (pin 17) is also pulled low. The software method of configuring the drive control outputs requires two successive writes to the Configuration Register at I/O address 3F3 hex. Writing a 0 to bit D7 will set up decoded outputs, and writing a 1 to bit D7 will set up the encoded outputs. See the PC87310 data sheet for more details about how to configure other features of the Super I/O via hardware or software.

Table I shows the states of the encoded drive and motor select outputs of the Super I/O, based on the bits programmed in the Drive Control Register. These outputs must then be decoded with external circuitry to produce four drive select and four motor select outputs. **Note:** *The encoded drive control outputs shown in Table I are valid only for the Drive Control Register Values shown. The user must ensure that the software will write only those values shown in the table to the Drive Control Register. Other values will result in non-unique drive control output states that could be falsely decoded by the external decoder circuit.*

TABLE I. Encoded Drive and Motor Select Outputs for PC87310

Drive Control Register Value (Hex)	Drive Control Output Pins				Description
	DR1	DR0	MTR1	MTR0	
0C	1	1	1	1	Turn Off All Drives
1C	1	1	1	0	Enable Drive A
2D	1	0	0	1	Enable Drive B
4E	0	1	1	1	Enable Drive C
8F	0	0	1	1	Enable Drive D

**Note 1:** For drive and motor select outputs, 0 = low and 1 = high (these are active low open-collector outputs).

**Note 2:** Bits 2 and 3 of the Drive Control Register are both set to 1, in order to keep the chip out of reset and enable the DRQ, INT, and  $\overline{DAK}$  signals.

## EXTERNAL DECODER CIRCUIT

Figure 1 shows the circuit required when supporting four drives with the Super I/O and its encoded drive control outputs. The circuit is relatively simple. All that is needed is a 16L8 PAL for the motor and drive select decode, and two 7406 inverting open collector drivers. The PAL will interpret the drive control signals as decoded if the CRB7 input is pulled high. If CRB7 is pulled low, the PAL will decode the drive control outputs according to the values in Table I. See the PAL equations for the decode of both drive control configurations.

The PAL outputs an active high signal for each drive/motor select pair when a particular drive and motor is selected via the Drive Control Register. Thus, only one drive select and one motor select line can be active at any one time, and there is no way to select a drive without also selecting its motor.

The active high outputs of the PAL are connected to the 7406 inverting buffers. This buffering is necessary because the PC87310 disk interface outputs are active low, open-collector outputs, capable of sinking up to 40 mA. The drive and motor select signals must also have this drive capability. Each drive enable output from the PAL is split into a drive select and motor select signal, so there is a total of four active low drive select lines (Drives A, B, C, and D), and four active low motor select lines.

In summary, the external decoder circuit will work for four drive access with encoded drive control outputs from the Super I/O. In addition, it will work for two drive access with decoded drive control outputs from the Super I/O.

## SOFTWARE THAT BYPASSES BIOS

There are many software programs that will bypass the BIOS driver routines and access the floppy controller directly, game programs being a good example. Diagnostic programs are another example of these kind of programs. As long as these programs know that there are four floppy drives in a system and access the floppy control directly, all that is required with the Super I/O for four drive support is the external decoder circuit.

Tape drives are devices that *require* their own software to access the floppy controller directly. Although these tape drives are floppy compatible, they cannot use the same software that is used to access a normal floppy drive because tape drives interpret floppy commands differently. For example, tape drive commands are sent to the drive in the form of step pulses. Since the software interface is different for tape drives, they must use their own software program to access the floppy controller directly. Many PC-AT systems

today will allow for a tape drive to be hooked up as logical drive 2. In this case, only the external decoder circuit is required with the Super I/O.

## EXTENDED BIOS ROM CIRCUIT

Most software for the PC-AT accesses the floppy drives via either BIOS or DOS function calls. Since DOS calls access the BOIS routines for floppy controller operations, it is the BIOS (via function call INT 13H that ultimately issues the commands to the floppy controller for a given operation. So if a particular piece of software is to take advantage of the existence of four floppy drives in a system, the BIOS must be able to access four drives.

The standard PC-AT BIOS is set up for a maximum of two floppy drives. Thus, a special BIOS must be written that will handle four drives. This BIOS must be part of the general expansion ROM BIOS address range (C800 to DFFF hex).

Figure 2 shows how to create an extended BIOS circuit for four drive support with the PC87310 Super I/O. National Semiconductor has developed a special floppy BIOS ROM for four drive support that uses this address range. National will provide a floppy ROM BIOS with object code upon request.

The expansion BIOS circuit consists of address decoding, the floppy BIOS ROM, and a drive setup register at address 3F0 hex, which is used to indicate the physical setup of floppy drives in the system.

The 74LS04 and 74LS32 are used to decode the floppy BIOS address range of C800h–CBFFh. The connections to the floppy BIOS are straightforward. Direct connections are made to the address, data and MEMR lines on the PC-AT bus. The Chip Enable (CE) input is taken from the address decode logic. Lastly, power and ground line connections are made.

The 74LS521, 74LS32, and 74LS245 make up the logic for the drive setup register at address 3F0. The LS521 and LS32 perform the address decode function, while the LS245 is used to enable the data bus during read operations at the 3F0 register address. The data for this register is derived from the jumper positions of JP1. See Table II for a description of the jumper positions and their configuration values. If the jumper is installed for a particular bit, then the bit is a logic 0, otherwise it is pulled high by RP2 and interpreted as a logic 1.

The hardware jumper JP1 replaces the configuration data for the floppy drives that is normally located in CMOS non-volatile memory in the PC-AT. The address of 3F0 hex was chosen for this drive setup register because it is unused and located within the normal floppy controller address range.

TABLE II. Floppy Configuration Register Bit Descriptions (Address 3F0 Hex)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Drive D1	Drive D0	Drive C1	Drive C0	Drive B1	Drive B0	Drive A1	Drive A0

**Note 3:** Jumper OPEN = 1  
Closed = 0

Drive X10 = 00–5.25" 360k Drive  
01–3.5" 720k Drive  
10–5.25" 1.2M Drive  
11–3.5" 1.44M Drive

**SUMMARY**

The method of implementing a four drive support circuit for the PC-AT with the Super I/O controller has been described. This circuit is comprised of two sections, the drive control decode circuit and the expansion ROM BIOS circuit. If the application is using software exclusively that accesses the floppy controller directly (bypassing BIOS calls), then only the decode circuit is needed.

If the application is for a PC-AT, there are many software programs, including DOS, that access the floppy controller via BIOS calls. In this case, the four drive support circuit must also include the expansion ROM BIOS interface. National Semiconductor has developed a floppy BIOS that can support four floppy or floppy compatible tape drives. A sample of this BIOS is available upon request in order to assist designers in developing their own four drive support circuit using the PC87310 Super I/O controller.

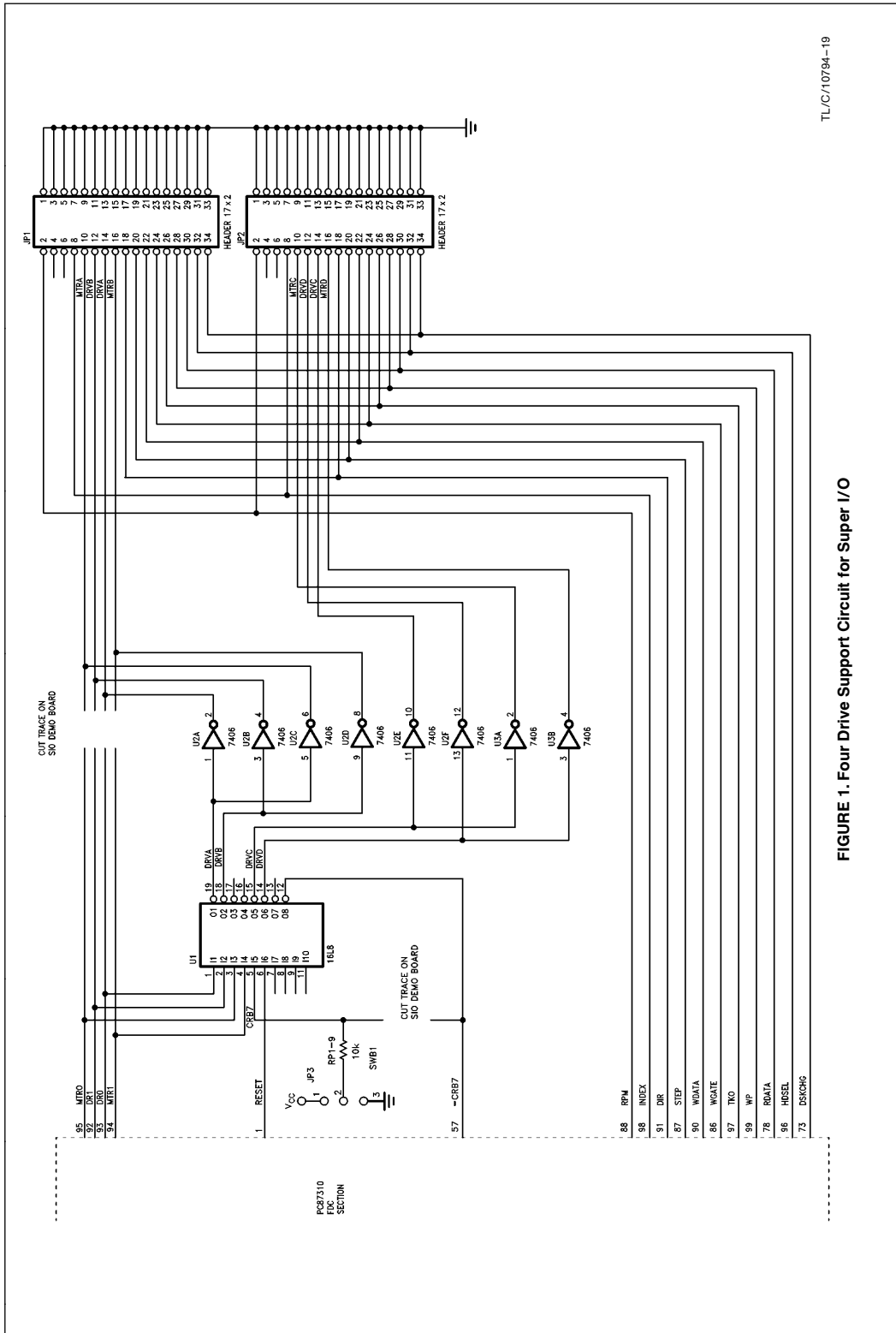
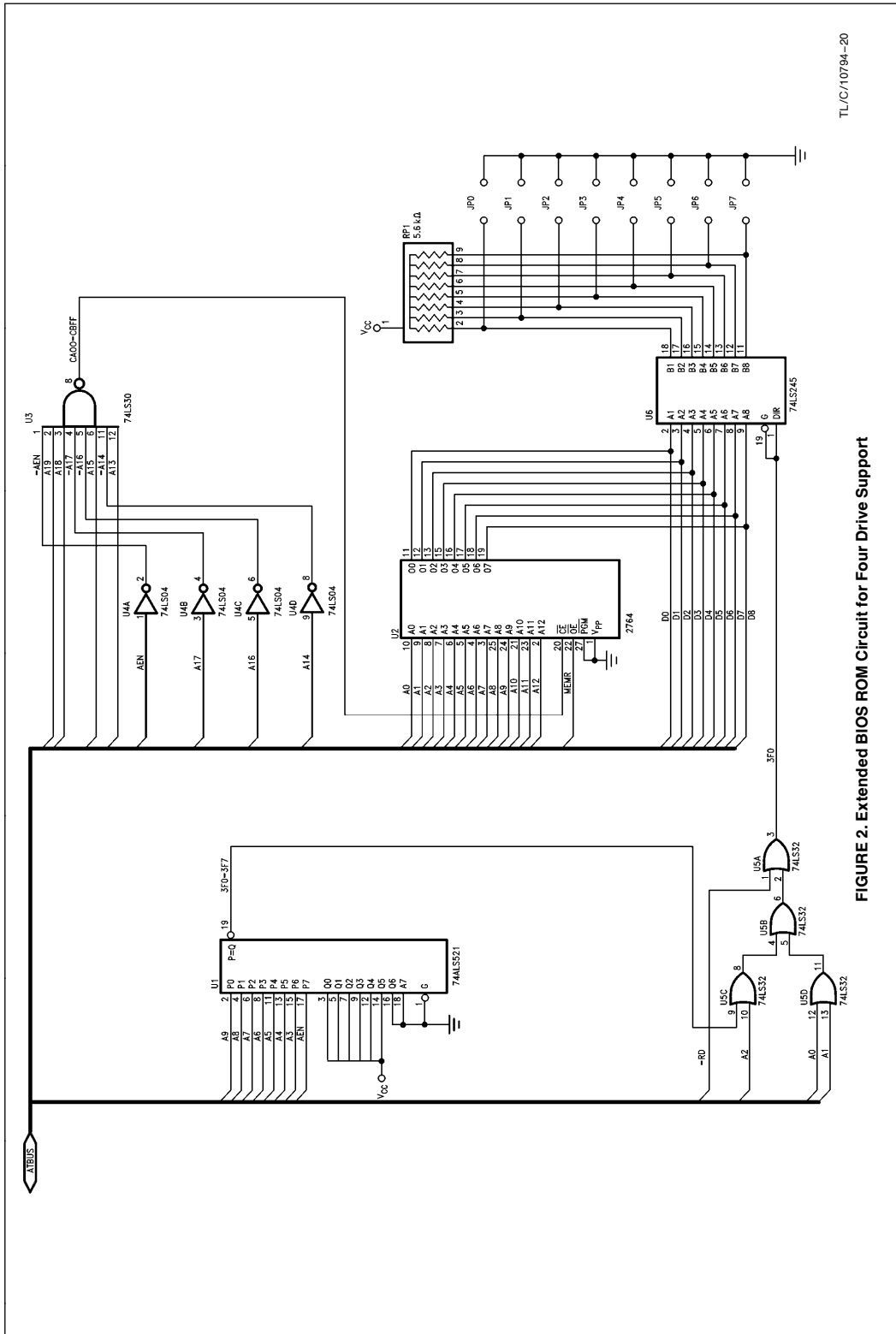


FIGURE 1. Four Drive Support Circuit for Super I/O

TL/C/10794-19



TL/G/10794-20

FIGURE 2. Extended BIOS ROM Circuit for Four Drive Support

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