

FAST®/FASTr™ Design Considerations

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FAST/FASTr Design Considerations

FAST and FASTr are high-speed logic families that achieve speeds typically 50% faster than the Schottky family with a corresponding power reduction of approximately 75%. They are fabricated with an advanced oxide isolation technique, Isoplanar II, which produces transistors with very high, well-controlled switching speeds, extremely small parasitic capacitances and f_T in excess of 5 GHz for FAST and 8 GHz for FASTr.

Since the family is designed to be pin-compatible with other TTL families existing designs can be easily upgraded. FAST logic offers significant improvement over the Schottky family in addition to improved speed and power specifications. Other key advantages are higher input threshold levels, reduced input loading, and increased output drive. The FAST family contains a complement of circuits for more efficient design capabilities.

Fairchild engineers had specific design objectives in mind when they developed the FAST/FASTr logic family. The primary objective was the improvement of the circuit speed-power performance versus earlier TTL families. Another important objective was increasing threshold levels to improve noise immunity. Other goals were maintaining or improving the output drive of Schottky for improved line driving capability, and reducing input loading for increasing the fan-out of the family. Output and input voltage levels, functions and pinouts were standardized to previous TTL families to maintain compatibility.

The primary design consideration was to improve speed while reducing power. The speed of any device is limited by the charge storage of the transistors. The time required to remove this charge is proportional to the capacitance and current available. Thus, to improve the speed, either the internal resistor values must be lowered to increase the available current and therefore remove the charge faster, such as in the Schottky family, or the capacitance must be reduced.

The speed-power curve shown in Figure 3-1a was used empirically to determine the optimum operating power level for the FAST family. Several internal gates programmed at a variety of power levels were produced on a wafer and the propagation delay of an internal gate for each power level was measured.

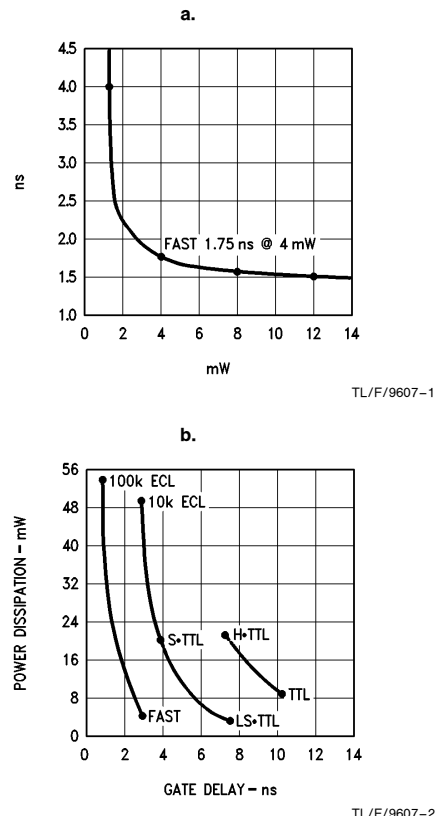


FIGURE 3-1. Speed-Power Product

As can be seen from the curves, power levels significantly below 4 mW per gate exhibit a dramatic degradation in performance. Power levels significantly above 4 mW, however, appear to have passed the point of diminishing returns with only minor improvements in propagation delay resulting from increased power. It was therefore concluded that the FAST family could be biased at 4 mW achieving a 1.75 ns propagation delay.

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Figure 3-1b compares the FAST logic family with previous TTL and ECL logic families. Each curve groups families with similar technologies. The first line, known as "gold doped," groups together the 7400 and the 74H families into one technology grouping. These saturating logic families can be seen to have a relatively poor speed-power curve.

The second curve notes the Schottky, Low Power Schottky and 10k ECL families. They use non-gold doped, soft saturated (Baker clamped) or current steering logic in order to achieve their speed-power performance; however, they still employ the planar technology. The last curve, which shows the FAST family with its ECL counterpart, the 100k ECL family, employs the Isoplanar technology. With FAST Isoplanar technology, 3 ns propagation delays at only 4 mW power dissipation are achieved with SSI devices.

THRESHOLD AND NOISE MARGINS

The noise margins most often cited for TTL obtained by subtracting the guaranteed maximum input HIGH level, V_{IH} , of a driven input from the guaranteed minimum output HIGH level, V_{OH} , of the driving source, and subtracting the guaranteed maximum output LOW level, V_{OL} , of the driver from

the guaranteed minimum input LOW level, V_{IL} , of a driven circuit. The guaranteed worst-case values of these parameters vary slightly among the various circuit families and are summarized in Table III-I. Note that although the 9000 Series V_{IH} and V_{IL} specifications have different limits at different temperatures, they are grouped with the 54/74 family in the table as a matter of convenience. Note also that the V_{OL} limit listed for 74LS is 0.5V, whereas these circuits are also specified at 0.4V at a lower level of I_{OL} . Noise margins calculated in this manner are quite conservative, since it is assumed that both the driver output characteristics are worst-case and that V_{CC} is on the low side for the driver and on the high side for the receiver.

Figure 3-2a shows how load capacitance affects the propagation delay of Low Power Schottky, Schottky and FAST gates, flip-flops, registers and decoders, etc. As would be expected, Low Power Schottky TTL shows greater sensitivity since LS output drive capability is not as great as either Schottky or FAST. Significantly, FAST is less affected than Schottky by load capacity. Figure 3-2b shows propagation delay versus load capacitance for buffers and line drivers since they are designed for greater output drive.

TABLE III-I. Parameter Limits

TTL Families		Military (-55°C to +125°C)				Commercial (0°C to +70°C)				Units
		V_{IL}	V_{IH}	V_{OL}	V_{OH}	V_{IL}	V_{IH}	V_{OL}	V_{OH}	
TTL	Standard TTL, 9000, 54/74	0.8	2.0	0.4	2.4	0.8	2.0	0.4	2.4	V
FAST/FASTr	54F/74F/74Fr	0.8	2.0	0.5	2.4	0.8	2.0	0.5	2.5	V
S-TTL	Schottky TTL, 54S/74S, 93S	0.8	2.0	0.5	2.5	0.8	2.0	0.5	2.7	V
LS-TTL	Low Power Schottky TTL, 54LS/74LS	0.7	2.0	0.4	2.5	0.8	2.0	0.5	2.7	V

V_{OL} and V_{OH} are the voltages generated at the output. V_{IL} and V_{IH} are the voltages required at the input to generate the appropriate levels. The numbers given above are guaranteed worst-case values for standard outputs.

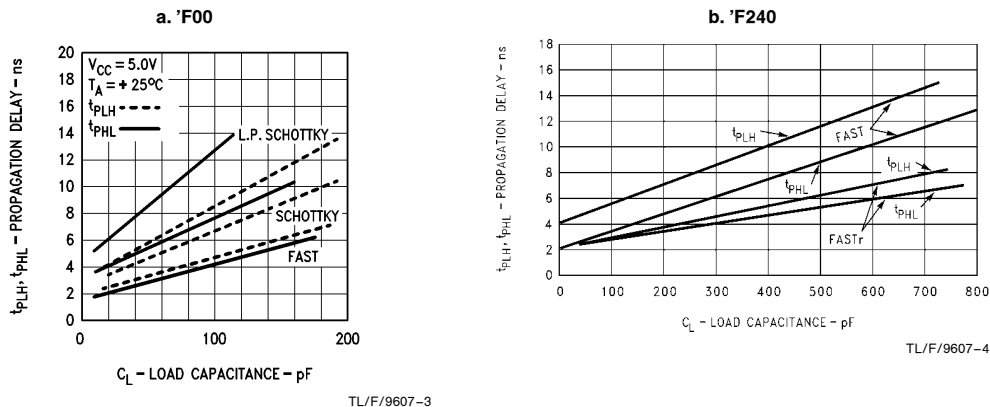


FIGURE 3-2. Propagation Delay vs Load Capacitance

Notice also in *Figure 3-2a* that for Schottky, the HIGH-to-LOW output transition is more affected than its LOW-to-HIGH transition, while for FAST both transitions are equally affected. This indicates a better balance in the design of the FAST output, and minimizes pulse stretching and compressing.

TEST AND SPECIFICATION IMPROVEMENTS

Because the circuitry and technological improvements (feedback and speedup diodes and the Miller Killer circuitry) yield well-controlled AC parameters, the FAST family can be specified over extremes of external influences. FAST is the first TTL logic family which does not require derating estimates for worst-case design. This has been accomplished by specifying minimum and maximum propagation delays over the operating temperature and supply voltage ranges with 50 pF loading for FAST and 250 pF/50 pF for FASTr. In addition, FASTr has extended specifications which include multiple output switching, propagation delays under 250 pF loading and guaranteed skew.

In order to achieve easier correlation with our customers' needs, a change in the actual AC test load was needed. Previously, most TTL families were measured with three serial diodes in parallel with the load capacitor. For the FAST/r logic family, a 50 pF/250 pF capacitance in parallel with a 500Ω resistor is employed. This facilitates fabrication of low capacitance test jigs. It also provides better correlation with customers' measurements of propagation delay. Passive 500Ω scope probes, which are less expensive and easier to use than the high impedance FET input scope probes, can be employed. This facilitates measurement of the AC performance on automatic test equipment and yields more conservative AC figures than are achieved with the previous AC load technique.

DESIGN CONSIDERATIONS

There are areas of concern which need to be addressed when designing with any high performance logic family. These topics include: transmission line concepts, printed circuit board layout, interfacing between technologies, open collector outputs, fanout, and unused inputs.

For additional information, please refer to National's FAST Applications Handbook.

TRANSMISSION LINES

Practical transmission lines, cables and strip lines used for TTL interconnections have a characteristic impedance between 30Ω and 150Ω. FAST is capable of driving a 50Ω line under worst-case conditions.

These considerations, applicable only when the round trip delay of the line is longer than the rise or fall time of the driving signal ($2t_d > t_r$), do not affect most TTL interconnections. Short interconnections do not behave like a resistive transmission line, but more like a capacitive load. Since the rise time of different TTL outputs is known, the longest interconnection that can be tolerated without causing transmission line effects can easily be calculated and is listed in Table III-II.

TABLE III-II. PC Board Interconnections

TTL Family	Rise Time	Fall Time	Max Interconnection Length
54/74, 54/74LS	6–9 ns	4–6 ns	18 in. (45 cm)
54S/74S	4–6 ns	2–3 ns	9 in. (22.5 cm)
FAST	1.8–2.8 ns	1.6–2.6 ns	7.5 in. (19 cm)
FASTr	1.2–2.3 ns	1.0–1.6 ns	5.0 in. (12.7 cm)

Assuming 1.7 ns/foot propagation speed, typical for epoxy fiberglass PC boards with $\epsilon_r = 4.7$.

Slightly longer interconnections show minimal transmission line effects; the longer the interconnections, the greater the chance that system performance may be degraded due to reflections and ringing.

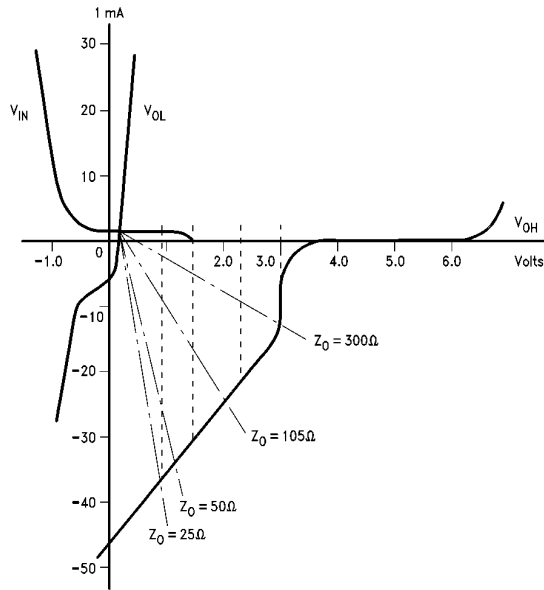
TRANSMISSION LINE EFFECTS

The fast rise and fall times of TTL outputs (2.0 ns to 6.0 ns) produce transmission line effects even with relatively short (<2 ft) interconnections. Consider one TTL device driving another and switching from the LOW to the HIGH state. If the propagation delay of the interconnection is long compared to the rise time of the signal, the arrangement behaves like a transmission line driven by a generator with a non-linear output impedance. Simple transmission line theory shows that the initial voltage step at the output just after the driver has switched is

$$V_{OUT} = V_E \frac{Z_O}{Z_O + R_O}$$

where Z_O is the characteristic impedance of the line, R_O is the output impedance of the driver, and V_E is the equivalent output voltage source in the driver, (i.e., V_{CC} minus the forward drop of the pull-up transistors).

Figure 3-3 shows how the initial voltage step can be determined graphically by superimposing lines of constant impedance of the static input and output characteristics of TTL elements. The constant impedance lines are drawn from the intersection of the V_{IN} and V_{OL} characteristics which is the quiescent condition preceding a LOW-to-HIGH transition. After this transition the V_{OH} characteristic applies, and the intersection of a particular impedance line with the V_{OH} characteristic determines the initial voltage step. The V_{OH} characteristic shown in *Figure 3-3* has an R_O of about 80Ω and V_E of approximately 4.0V, for calculation purposes.



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FIGURE 3-3. Initial Output Voltage of a 5400 TTL Driving Transmission Line

This initial voltage step propagates down the line and reflects at the end, assuming the typical case where the line is open-ended or terminated in an impedance greater than its characteristic impedance Z_0 . Arriving back at the source, this reflected wave increases V_{OUT} . If the total round-trip delay is larger than the rise time of the driving signal, there is a staircase response at the driver output and anywhere along the line. If one of the loads (gate inputs) is connected to the line close to the driver, the initial output voltage V_{OUT} might not exceed V_{IH} . This input is then undetermined until after the round trip of the system. Figure 3-4 shows the 'F00 driver output waveform for four different line impedances.

For Z_0 of 25Ω and 50Ω , the initial voltage step is in the threshold region of a TTL input and the output voltage only rises above the guaranteed $2.0V$ V_{IH} level after a reflection returns from the end of the line. If V_{OUT} is increased to $>2.0V$, by either increasing Z_0 or decreasing R_O , additional delay does not occur. R_O is characteristic of the driver output configuration, varying between the different TTL speed categories. Z_0 can be changed by varying the width of the conductor and its distance from ground. Table III-III lists the lowest transmission line impedance that can be driven by different TTL devices to insure an initial voltage step of $2.0V$.

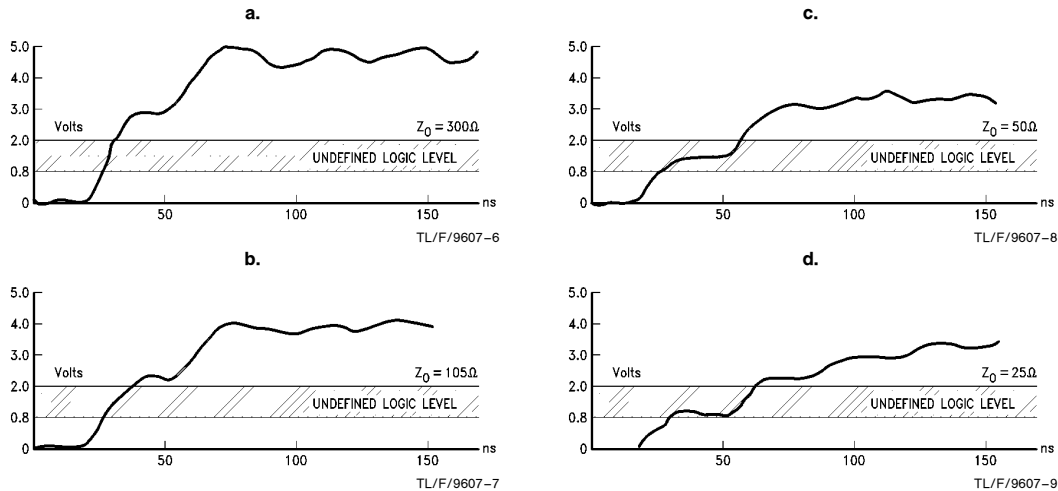


FIGURE 3-4. TTL Driving Transmission Line

Note that the worst-case value, assuming a $+30\%$ tolerance on the current limiting resistor and a -10% tolerance on V_{CC} , is 80% higher than the value for nominal conditions.

TABLE III-III. Transmission Line Driving Capability

TTL Family or Device	Collector Resistor R_{Ω}	Lowest Transmission Line Impedance Ω				
		Worst Case ($R + 30\%$)		Nominal	Best Case ($R - 30\%$)	
54/74	130	241.4	204.8	136.8	84.6	75.8
54S/74S	55	110.0	92.2	61.1	37.5	33.4
5440/7440	100	185.7	157.5	105.2	65.1	58.3
54S/74S40	25	50.0	41.9	27.7	17.0	15.2
54F/74F00	45	66.2	57.7	40.9	27.6	25.0
54F/74F258	25	36.76	32.0	22.7	15.3	13.9
54F/74F240/Fr240	15	22.0	19.2	13.6	9.2	8.3
Supply Voltage (V_{CC})		4.50	4.75	5.00	5.25	5.50

A graphical method provides excellent insight into the effects of high-speed digital circuits driving interconnections acting as transmission lines. A load line is drawn for each input and output situation. Each load line starts at the previous quiescent point, determined where the previous load line intersects the appropriate characteristic. The magnitude of the slope of the load lines is identical and equal to the characteristic impedance of the line, but alternate load lines have opposite signs representing the change in direction of current flow. The points where the load lines intersect the input and output characteristics represent the voltage and current value at the input or output, respectively, for that reflection. The results, *Figure 3-5*, are shown with and without the input diode and illustrate how the input diode on TTL elements assists in eliminating spurious switching due to reflection.

TRANSMISSION LINE CONCEPTS

The interactions between wiring and circuitry in high-speed systems are more easily determined by treating the interconnections as transmission lines. A brief review of basic concepts is presented and simplified methods of analysis

are used to examine situations commonly encountered in digital systems. Since the principles and methods apply to any type of logic circuit, normalized pulse amplitudes are used in sample waveforms and calculations.

SIMPLIFYING ASSUMPTIONS

For the great majority of interconnections in digital systems, the resistance of the conductors is much less than the input and output resistance of the circuits. Similarly, the insulating materials have very good dielectric properties. These circumstances allow such factors as attenuation, phase distortion and bandwidth limitations to be ignored. With these simplifications, interconnections can be dealt with in terms of characteristic impedance and propagation delay.

CHARACTERISTIC IMPEDANCE

The two conductors that interconnect a pair of circuits have distributed series inductance and distributed capacitance between them, and thus constitute a transmission line. For any length in which these distributed parameters are constant, the pair of conductors have a characteristic imped-

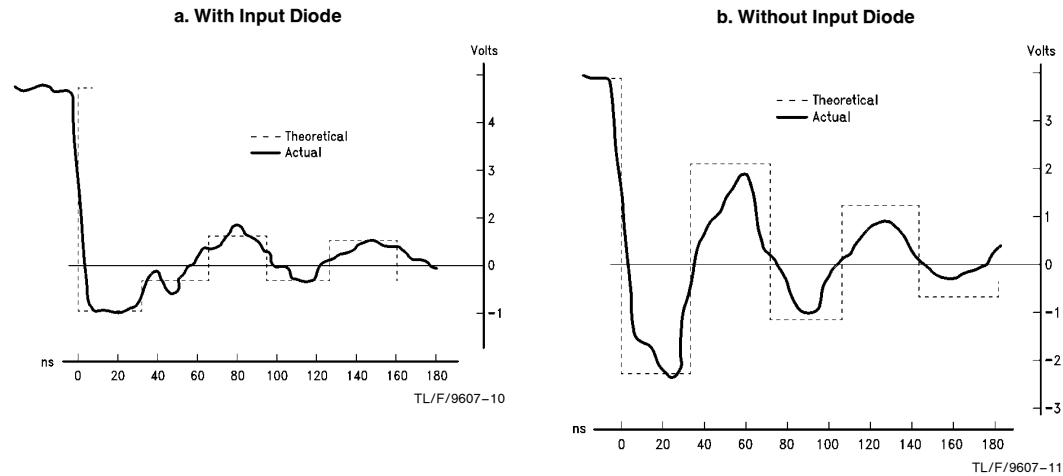


FIGURE 3-5. Ringing Caused by Reflections

ance Z_0 . Where quiescent conditions on the line are determined by the circuits and terminations, Z_0 is the ratio of transient voltage to transient current passing by a point on the line when a signal change or other electrical disturbance occurs. The relationship between transient voltage, transient current, characteristic impedance, and the distributed parameters is expressed as follows:

$$V/I = Z_0 = \sqrt{L_0/C_0}$$

where L_0 = inductance per unit length, and C_0 = capacitance per unit length. Z_0 is in ohms, L_0 in henries, and C_0 in farads.

PROPAGATION VELOCITY

Propagation velocity (v) and its reciprocal, delay per unit length δ , can also be expressed in terms of L_0 and C_0 . A consistent set of units is nanoseconds, microhenries and picofarads, with a common unit of length.

$$v = 1/\sqrt{L_0 C_0} \quad \delta = \sqrt{L_0 C_0}$$

These equations provide a convenient means of determining the L_0 and C_0 of a line when delay, length and impedance are known. For a length 1 and delay T , δ is the ratio $T/1$. To determine L_0 and C_0 , combine these equations.

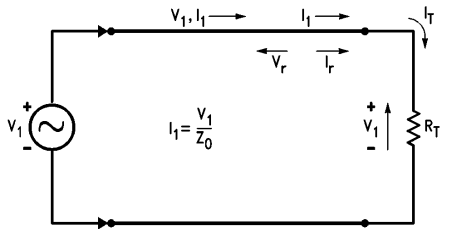
$$L_0 = \delta Z_0$$

$$C_0 = \delta/Z_0$$

More formal treatments of transmission line effects are available from many sources.

TERMINATION AND REFLECTION

A transmission line with a terminating resistor is shown in Figure 3-6. As indicated, a positive step function voltage travels from left to right. To keep track of reflection polarities, it is convenient to consider the lower conductor as the voltage reference and to think in terms of current flow in the top conductor only. The generator is assumed to have zero internal impedance. The initial current I_1 is determined by V_1 and Z_0 .



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LINE LENGTH = 1

DELAY = $T = 1 \delta$

FIGURE 3-6

If the terminating resistor matches the line impedance, the ratio of voltage to current traveling along the line is matched by the ratio of voltage to current which must, by Ohm's law, always prevail at R_T . From the viewpoint of the voltage step generator, no adjustment of output current is ever required; the situation is as though the transmission line never existed and R_T has been connected directly across the terminals of the generator.

From the R_T viewpoint, the only thing the line did was delay the arrival of the voltage step by the amount of time T .

When R_T is not equal to Z_0 , the initial current starting down the line is still determined by V_1 and Z_0 but the final steady

state current, after all reflections have died out, is determined by V_1 and R_T (ohmic resistance of the line is assumed to be negligible). The ratio of voltage to current in the initial wave is not equal to the ratio of voltage to current demanded by R_T . Therefore, at the instant the initial wave arrives at R_T , another voltage and current wave must be generated so that Ohm's law is satisfied at the line-load interface. This reflected wave, indicated by V_r and I_r in Figure 3-6, starts to return toward the generator. Applying Kirchoff's laws to the end of the line at the instant the initial wave arrives results in the following:

$$I_i + I_r = I_T = \text{current into } R_T$$

Since only one voltage can exist at the end of the line at this instant of time, the following is true:

$$V_1 + V_r = V_T$$

thus,

$$I_T = V_T/R_T = (V_1 + V_r)/R_T$$

also,

$$I_i = V_1/Z_0 \text{ and } I_r = -V_r/Z_0$$

with the minus sign indicating that V_r is moving toward the generator.

Combining the foregoing relationships algebraically and solving for V_r yields a simplified expression in terms of V_1 , Z_0 and R_T .

$$\begin{aligned} \frac{V_1}{Z_0} - \frac{V_r}{Z_0} &= \frac{V_1 + V_r}{R_T} = \frac{V_1}{R_T} + \frac{V_r}{R_T} \\ V_1 \left(\frac{1}{Z_0} - \frac{1}{R_T} \right) &= V_r \left(\frac{1}{R_T} + \frac{1}{Z_0} \right) \\ V_r &= V_1 \left(\frac{R_T - Z_0}{R_T + Z_0} \right) = \rho_L V_1 \end{aligned}$$

The term in parentheses is called the coefficient of reflection (ρ_L). With R_T ranging between zero (shorted line) and infinity (open line), the coefficient ranges between -1 and $+1$ respectively. The subscript L indicates that ρ_L refers to the coefficient at the load end of the line.

This last equation expresses the amount of voltage sent back down the line, and since

$$V_T = V_1 + V_r$$

then

$$V_T = V_1 (1 + \rho_L)$$

V_T can also be determined from an expression which does not require the preliminary step of calculating ρ_L . Manipulating $(1 + \rho_L)$ results in

$$\begin{aligned} 1 + \rho_L &= 1 + (R_T - Z_0)/(R_T + Z_0) \\ &= 2(R_T/(R_T + Z_0)) \end{aligned}$$

Substituting, this gives

$$V_T = 2(R_T/(R_T + Z_0)) V_1$$

The foregoing has the same form as a simple voltage divider involving a generator V_1 with internal impedance, Z_0 , driving a load R_T , except that the amplitude of V_T is doubled.

The arrow indicating the direction of V_r in Figure 3-6 correctly indicates the V_r direction of travel, but the direction of I_r flow depends on the V_r polarity. If V_r is positive, I_r flows toward the generator, opposing I_1 . This relationship between the polarity of V_r and the direction of I_r can be deduced by noting that if V_r is positive it is because R_T is greater than Z_0 . In turn, this means that the initial current I_r

is larger than the final quiescent current, dictated by V_1 and R_T . Hence I_r must oppose I_1 to reduce the line current to the final quiescent value. Similar reasoning shows that if V_r is negative, I_r flows in the same direction as I_1 .

It is somewhat easier to determine the effect of V_r on line conditions by thinking of it as an independent voltage generator in series with R_T . With this concept, the direction of I_r is immediately apparent; its magnitude, however, is the ratio of V_r to Z_0 , i.e., R_T is already accounted for in the magnitude of V_r . The relationships between incident and reflected signals are represented in *Figure 3-7* for both cases of mismatch between R_T and Z_0 .

The incident wave is shown in *Figure 3-7a*, before it has reached the end of the line. In *Figure 3-7b*, a positive V_r is returning to the generator. To the left of V_r the current is still I_1 , flowing to the right, while to the right of V_r the net current in the line is the difference between I_1 and I_r . In *Figure 3-7c*, the reflection coefficient is negative, producing a negative V_r . This, in turn, causes an increase in the amount of current flowing to the right behind the V_r wave.

SOURCE IMPEDANCE, MULTIPLE REFLECTIONS

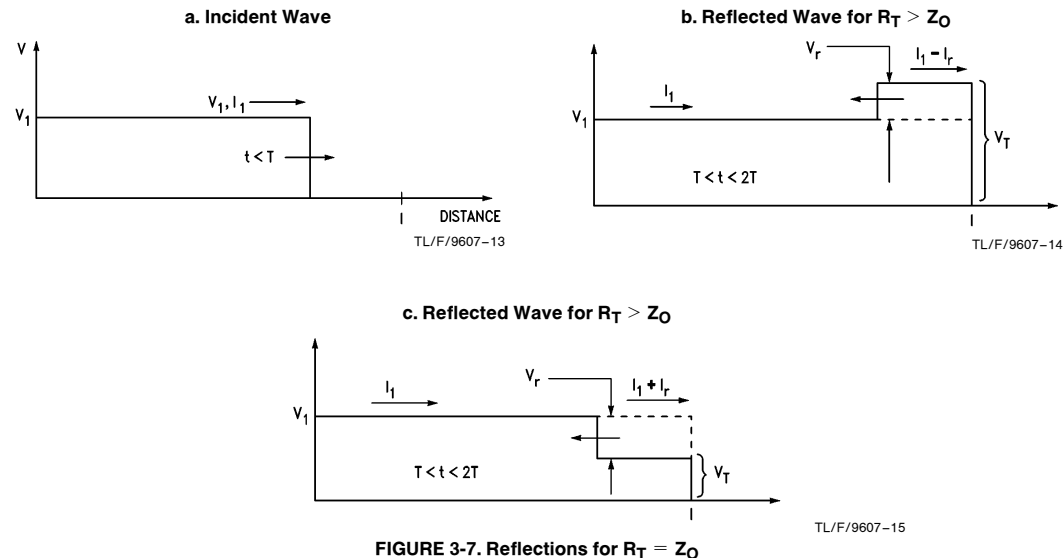
When a reflected voltage arrives back at the source (generator), the reflection coefficient at the source determines the response to V_r . The coefficient of reflection at the source is governed by Z_0 and the source resistance R_S .

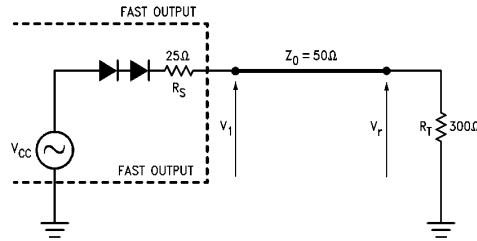
$$\rho_S = (R_S - Z_0)/(R_S + Z_0)$$

If the source impedance matches the line impedance, a reflected voltage arriving at the source is not reflected back toward the load end. Voltage and current on the line are stable with the following values.

$$V_T = V_i + V_r$$

If neither source impedance nor terminating impedance matches Z_0 , multiple reflections occur; the voltage at each end of the line comes closer to the final steady state value with each succeeding reflection. An example of a line mismatched on both ends is shown in *Figure 3-8*. The source is a step function of $V_{CC} = 5.0V$ amplitude occurring at time t_0 . The initial value of V_1 starting down the line is 2.4V due to the voltage divider action of Z_0 and R_S . The time scale in the photograph shows that the line delay is approximately 6 ns. Since neither end of the line is terminated in its characteristic impedance, multiple reflections occur.





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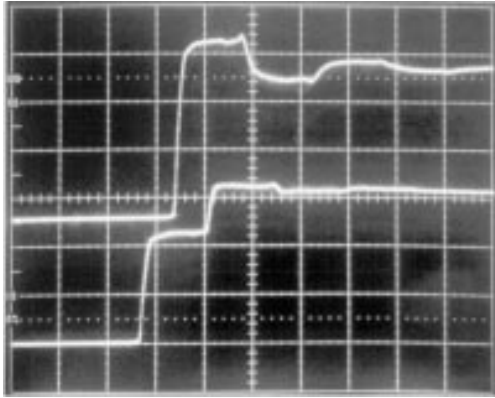
FIGURE 3-8. Multiple Reflections Due to Mismatch at Load and Source

$$V_O = V_{CC} - 2 \cdot V_{BE} = 3.6V$$

$$\rho_S = \frac{(25 - 50)\Omega}{(25 + 50)\Omega} = -0.33$$

$$\text{initially, } V_1 = \frac{Z_O}{Z_O + R_S} \cdot V_O = \frac{50\Omega}{(50 + 25)\Omega} (3.6V) = 2.4V$$

$$\rho_L = \frac{(300 - 50)\Omega}{(300 + 50)\Omega} = 0.71$$



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H = 20 ns/div.
V = 1V/div.

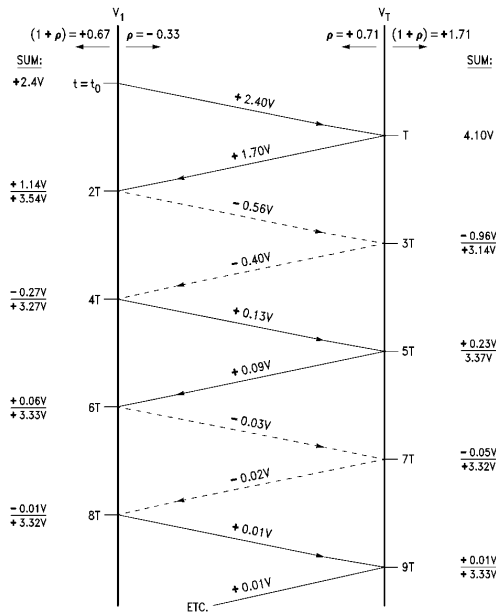
The amplitude and persistence of the ringing shown in *Figure 3-8* become greater with increasing mismatch between the line impedance and source and load impedances. The difference in amplitude between the first two positive peaks observed at the open end is

$$\begin{aligned} V_T - V'_T &= (1 + \rho_L) V_1 - (1 + \rho_L) V_1 \rho_L^2 \rho_S^2 \\ &= (1 + \rho_L) V_1 (1 - \rho_L^2 \rho_S^2) \end{aligned}$$

The factor $(1 - \rho_S^2)$ is similar to the damping factor associated with lumped constant circuitry. It expresses the attenuation of successive positive or negative peaks of ringing.

LATTICE DIAGRAM

In the presence of multiple reflections, keeping track of the incremental waves on the line and the net voltage at the ends becomes a bookkeeping chore. A convenient and systematic method of indicating the conditions which combine magnitude, polarity and time utilizes a graphic construction called a lattice diagram. A lattice diagram for the line conditions of *Figure 3-8* is shown in *Figure 3-9*.



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FIGURE 3-9. Lattice Diagram for the Circuit of Figure 3-8

The vertical lines symbolize discontinuity points, in this case the ends of the line. A time scale is marked off on each line in increments of $2T$, starting at t_0 for V_1 and T voltages traveling between the ends of the line; solid lines are used for positive voltages and dashed lines for transmission multipliers ρ and $(1 + \rho)$ at each vertical line, and to tabulate the incremental and net voltages in columns alongside the vertical lines. Both the lattice diagram and the waveform photograph show that V_1 and V_T asymptotically approach 3.4V, as they must with a 3.4V source driving a lightly loaded line.

SHORTED LINE

The open-ended line in *Figure 3-8* has a reflection coefficient of 0.71 and the successive reflections tend toward the steady state conditions of zero line current and a line voltage equal to the source voltage. In contrast, a shorted line has a reflection coefficient of -1 and successive reflections must cause the line conditions to approach the steady state conditions of zero voltage and a line current determined by the source voltage and resistance.

Shorted line conditions are shown in *Figure 3-10a* with the reflection coefficient at the source end of the line also negative. A negative coefficient at both ends of the line means that any voltage approaching either end of the line is reflected in the opposite polarity. *Figure 3-10b* shows the response to an input step-function with a duration much longer than the line delay. The initial voltage starting down the line is about 2.4V, which is inverted at the shorted end and returned toward the source as $-2.4V$. Arriving back at the source end of the line, this voltage is multiplied by $(1 + \rho_S)$, causing a $-1.61V$ net change in V_1 . Concurrently, a reflected voltage of $+0.80V$ ($-2.4V$ times ρ_S of -0.33) starts back toward the shorted end of the line. The voltage at V_1 is reduced by 50% with each successive round trip of reflections, thus leading to the final condition of zero volts on the line.

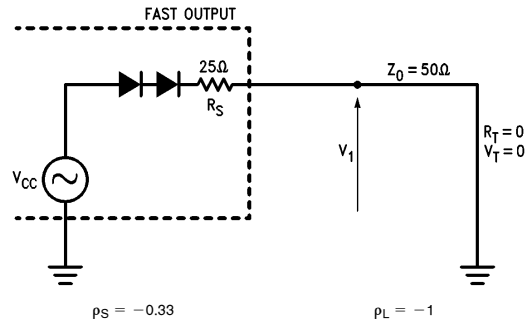
When the duration of the input pulse is less than the delay of the line, the reflections observed at the source end of the line constitute a train of negative pulses, as shown in *Figure 3-10c*. The amplitude decreases by 50% with each successive occurrence as it did in *Figure 3-10b*.

SERIES TERMINATION

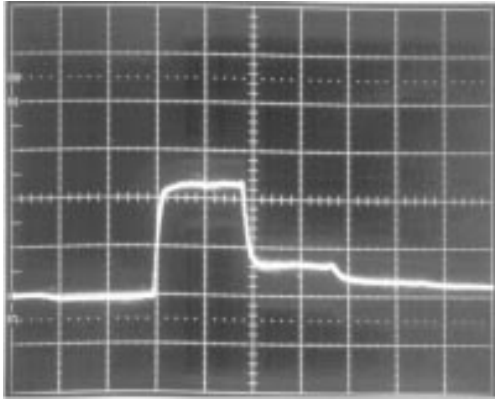
Driving an open-ended line through a source resistance equal to the line impedance is called series termination. It is particularly useful when transmitting signals which originate on a PC board and travel through the back-plane to another board, with the attendant discontinuities, since reflections coming back to the source are absorbed and ringing thereby controlled. The amplitude of the initial signal sent down the line is only half of the generator voltage, while the voltage at the open end of the line is doubled to full amplitude ($1 + \rho_L = 2$). The reflected voltage arriving back at the source raises V_1 to the full amplitude of the generator signal. Since the reflection coefficient at the source is zero, no further changes occur and the line voltage is equal to the generator voltage. Because the initial signal on the line is only half the normal signal swing, the loads must be connected at or near the end of the line to avoid receiving a 2-step input signal.

A TTL output driving a series-terminated line is severely limited in its fanout capabilities due to the IR drop associated with the collective I_{IL} drops of the inputs being driven. For most TTL families other than FAST it should not be considered since either the input currents are so high (TTL, S, H) or the input threshold is very low (LS). In either case the noise margins are severely degraded to the point where the circuit becomes unusable. In FAST, however, the I_{IL} of 0.6 mA, if sunk through a resistor of 25Ω used a series terminating resistor, will reduce the low level noise margin 15 mV for each standard FAST input driven.

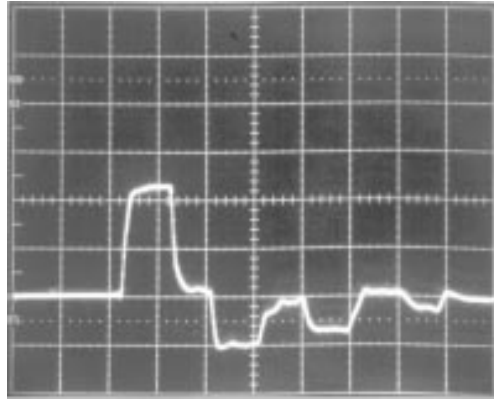
a. Reflection Coefficients for Shorted Line



b. Input Pulse Duration $\gg$ Line Delay



c. Input Pulse Duration $<$ Line Delay



V = 1V/div.
H = 20 ns/div.

FIGURE 3-10. Reflections of Long and Short Pulses on a Shorted Line

TABLE III-IV. Relative Dielectric Constants of Various Materials

Material	ϵ_r
Air	1.0
Polyethylene Foam	1.6
Cellular Polyethylene	1.8
Teflon	2.1
Polyethylene	2.3
Polystyrene	2.5
Nylon	3.0
Silicon Rubber	3.1
Polyvinylchloride (PVC)	3.5
Epoxy Resin	3.6
Delrin	3.7
Epoxy Glass	4.7
Mylar	5.0
Polyurethane	7.0

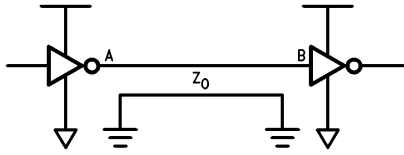
All the above information on impedance and propagation delays are for the circuit interconnect only. The actual impedance and propagation delays will differ from this by the loading effects of gate input and output capacitances, and by any connectors that may be in line. The effective impedance and propagation delay can be determined from the following formula:

$$Z_O' = \sqrt{1 + \left(\frac{C_L}{C_O}\right)} \Omega$$

$$t_{PD} = \sqrt{L_O C_O} \quad \therefore t_{PD}' = t_{PD} \sqrt{1 + \left(\frac{C_L}{C_O}\right)}$$

where C_L is the total of all additional loading.

The results of these formulas will frequently give effective impedances of less than half Z_O , and interconnect propagation delays greater than the driving device propagation delays, thus becoming the predominant delay.



TL/F/9607-22

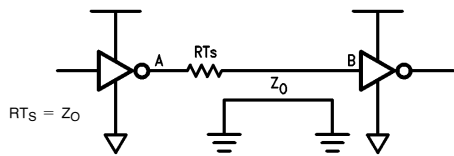
FIGURE 3-11. Unterminated

The maximum length for an unterminated line can be determined by

$$l_{\max} = T_r / 2t_{pd}$$

and for FAST, $t_r = 3$ ns, so $l_{\max} = 10$ inches for trace on GIO epoxy glass PC.

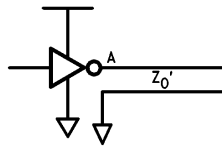
The voltage wave propagated down the transmission line (V step) is the full output drive of the device into Z_0' . Reflections will not be a problem if $l \leq l_{\max}$. Lines longer than $l_{\max}$ will be subject to ringing and reflections and will drive the inputs and outputs below ground.



TL/F/9607-23

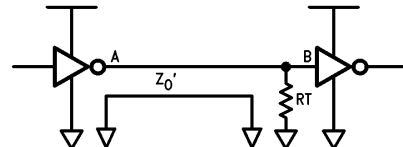
FIGURE 3-12. Series-Terminated

a. RT to V_{CC}
 $RT = Z_0'$



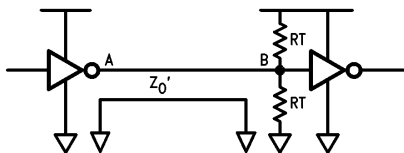
TL/F/9607-24

b. RT to GND
 $RT = Z_0'$



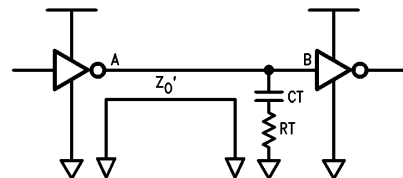
TL/F/9607-25

c. Thevenin Termination
 $RT = 2Z_0'$



TL/F/9607-26

d. AC Termination to GND
 $R_T + X_{CT} = Z_0'$



TL/F/9607-27

FIGURE 3-13. Parallel Terminated

Series termination has limited use in TTL interconnect schemes due to the voltage drop across R_T s in the LOW state, reducing noise margins at the receiver. Series termination is the ideal termination for highly capacitive memory arrays whose DC loadings are minimal. R_T s values of 10Ω to 50Ω are normally found in these applications.

Four possibilities for parallel termination exist:

- A. Z_0' to V_{CC} . This will consume current from V_{CC} when output is LOW;
- B. Z_0' to GND. This will consume current from V_{CC} when output is HIGH;
- C. Thevenin equivalent termination. This will consume half the current of A and B from the output stage, but will have reduced noise margins, and consume current from V_{CC} with outputs HIGH or LOW. If used on a TRI-STATE® bus, this will set the quiescent line voltage to half.

- D. AC Termination. An RC termination to GND, $C = 3tr/Z_0$. This consumes no DC current with outputs in either state. If this is used on a TRI-STATE bus, then the quiescent voltage on the line can be established at V_{CC} or GND by a high value pull up (down) resistor to the appropriate supply rail.

DECOUPLING

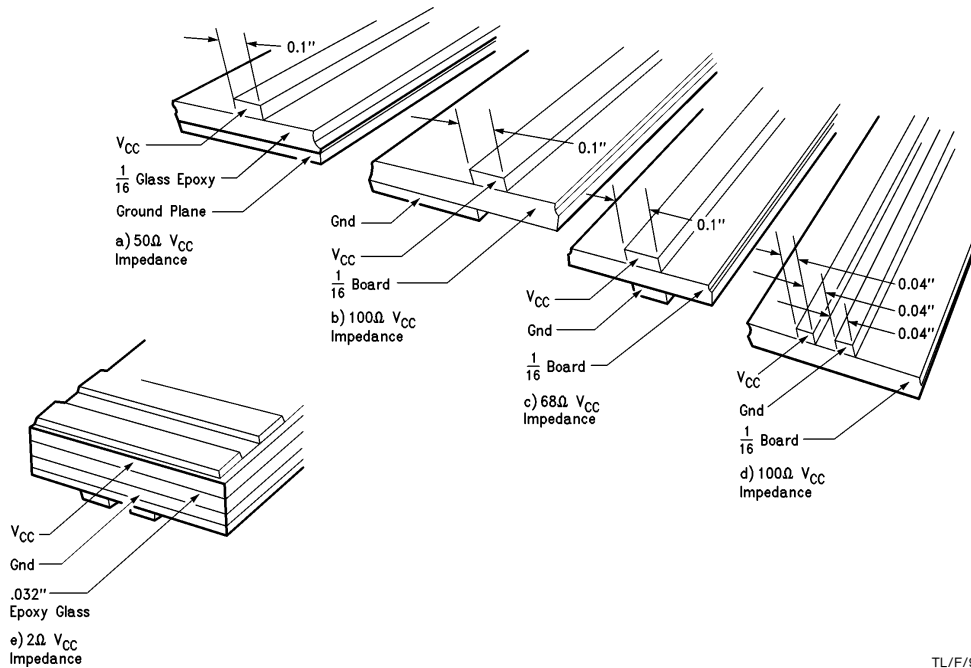


FIGURE 3-14. Typical Dynamic Impedance of Unbypassed V_{CC} Runs

TL/F/9607-28

This diagram shows several schemes for power and ground distribution on logic boards. Figure 3-14 is a cross-section, with a, b, and c showing a 0.1 inch wide V_{CC} bus and ground on the opposite side. Figure 3-14d shows side-by-side V_{CC} and ground strips, each 0.04 inch wide. Figure 3-14e shows a four layer board with embedded power and ground planes.

In Figure 3-14a, the dynamic impedance of V_{CC} with respect to ground is 50Ω , even though the V_{CC} trace width is generous and there is a complete ground plane. In Figure 3-14b, the ground plane stops just below the edge of the V_{CC} bus and the dynamic impedance doubles to 100Ω . In Figure 3-14c, the ground bus is also 0.1 inch wide and runs along under the V_{CC} bus and exhibits a dynamic impedance of about 68Ω . In Figure 3-14d, the trace widths and spacing are such that the traces can run under a DIP, between two

rows of pins. The impedance of the power and ground planes in Figure 3-14e is typically less than 2Ω .

These typical dynamic impedances point out why a sudden current demand due to an IC output switching can cause a momentary reduction in V_{CC} , unless a bypass capacitor is located near the IC.

Decoupling capacitors should be used on every PC card, at least one for every five to ten standard TTL packages, one for every five 'LS and 'S packages, one for every three FAST packages, and one for every one-shot (monostable), line driver and line receiver package. They should be good quality rf capacitors of $0.01\ \mu\text{F}$ to $0.1\ \mu\text{F}$ with short leads. It is particularly important to place good rf capacitors near sequential (bistable) devices. In addition, a larger capacitor (preferably a tantalum capacitor) of $2.0\ \mu\text{F}$ to $20\ \mu\text{F}$ should be included on each card.

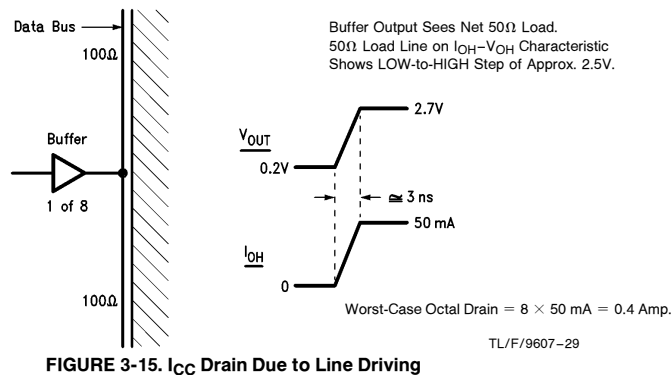
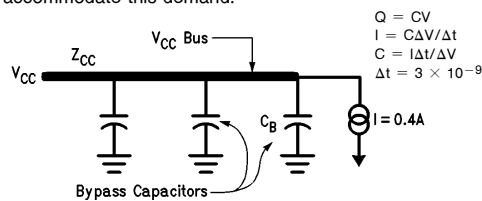


FIGURE 3-15. I_{CC} Drain Due to Line Driving

TL/F/9607-29

This diagram illustrates the sudden demand for current from V_{CC} when a buffer output forces a LOW-to-HIGH transition into the midpoint of a data bus. The sketch shows a wire-over-ground transmission line, but it could also be a twisted pair, flat cable or PC interconnect.

The buffer output effectively sees two 100Ω lines in parallel and thus a 50Ω load. For this value of load impedance, the buffer output will force an initial LOW-to-HIGH transition from 0.2V to 2.7V in about 3 ns. This net charge of 2.5V into a 50Ω load causes an output-HIGH current change of 50 mA. If all eight outputs of an octal buffer switch simultaneously, in this application the current demand on V_{CC} would be 0.4A. Clearly, a nearby V_{CC} bypass capacitor is needed to accommodate this demand.



TL/F/9607-30

FIGURE 3-16. V_{CC} Bypass Capacitor for Octal Driver

Specify V_{CC} Droop = 0.1V max.

$$C = \frac{0.4 \times 3 \times 10^{-9}}{0.1} = 12 \times 10^{-9} = 0.012 \mu F$$

Select $C_B \geq 0.02 \mu F$

A V_{CC} bus with bypass capacitors connected periodically along its length is shown above. Also shown is a current source representing the current demand of the buffer in the preceding application.

The equations illustrate an approximation method of estimating the size of a bypass capacitor based on the current demand, the drop in V_{CC} that can be tolerated and the length of time that the capacitor must supply the charge. While the demand is known, the other two parameters must be chosen. A V_{CC} droop of 0.1V will not cause any appreciable change in performance, while a time duration of 3 ns is long enough for other nearby bypass capacitors to help supply charge. If the current demand continues over a long period of time, charge must be supplied by a very large capacitor on the board. This is the reason for the recommendation that a large capacitor be located where V_{CC} comes onto a board. If the buffers are also located near the connector end of the board, the large capacitor helps supply charge sooner.

DESIGN GUIDELINES

Ground

A good ground system is essential for a PC card containing a large number of packages. The ground can either be a good ground bus, or better, a ground plane which, incorporated with the V_{CC} supply, forms a transmission line power system. Power transmission systems, which can be attached to a PC card to give an excellent power system without the cost of a multilayer PC card, are commercially available. Ground loops on or off PC cards are to be avoided unless they approximate a ground plane.

With the advent of FAST/FASTr, with considerably faster edge rates and switching times, proper grounding practice has become of primary concern in printed circuit layout. Poor circuit grounding layout techniques may result in crosstalk and slowed switching rates. This reduces overall circuit performance and may necessitate costly redesign. Also when FAST chips are substituted for standard TTL-designed printed circuit boards, faster edge rates can cause noise problems. The source of these problems can be sorted into three categories:

1. V_{CC} droop due to faster load capacitance charging;
2. Coupling via ground paths adjacent to both signal sources and loads; and
3. Crosstalk caused by parallel signal paths.

V_{CC} droop can be remedied with better or more bypassing to ground. The rule here is to place $0.01 \mu F$ capacitors from V_{CC} to ground for every FAST/FASTr circuit used, as near the IC as possible. The other two problems are not as easily corrected, because PC boards, may already be manufactured and utilized. In this case, simply replacing TTL circuits with FAST/FASTr compatible circuits is not always as easy as it may seem, especially on two-sided boards. In this situation IC placement is critical at high speeds. Also when designing high density circuit layout, a ground-plane layer is imperative to provide both a sufficiently low inductance current return path and to provide electromagnetic and electrostatic shielding thus preventing noise problem 2 and reducing, by a large degree, noise problem 3.

Two-Sided PC Board Layout Problems

When considering the two-sided PC board, more than one ground trace is often found in a parallel or non-parallel configuration. For this illustration parallel traces tied together at one end are shown. This arrangement is referred to as a ground comb. The ground comb is placed on one side of the PC board while the signal traces are on the other side, thus the two-sided circuit board.

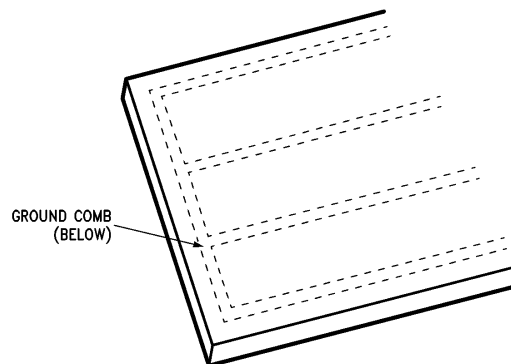


FIGURE 3-17

TL/F/9607-31

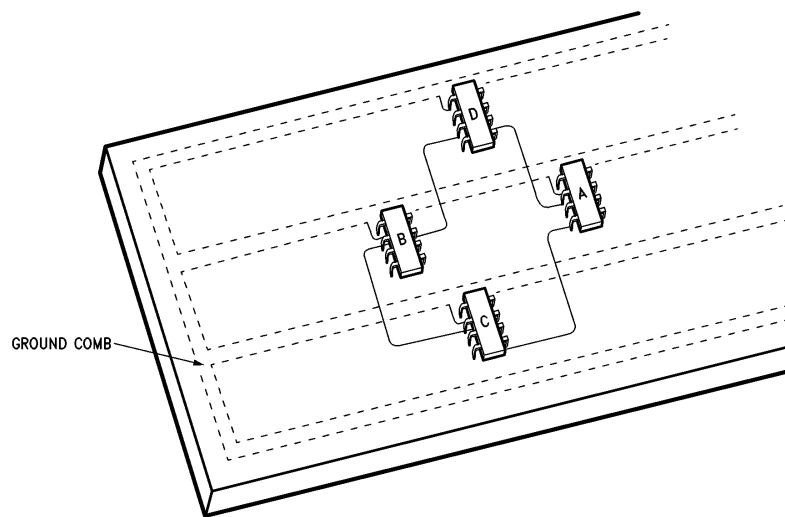


FIGURE 3-18

TL/F/9607-32

Figure 3-18 illustrates how noise is generated even though there is no apparent means of crosstalk between the circuits. If package A has an output which drives package D input and package B output drives package C input, there is no apparent path for crosstalk since mutual signal traces are remotely located. What is significant, and must be emphasized here, is that circuit packages A and B accept their ground link from the same trace. Hence, circuit A may well couple noise to circuit B via the common or shared portion

of the trace. This is especially true at high switching speeds. Because of the noise problems associated with ground combs, they are not recommended for final designs. Solid copper plates or ground planes on multi-layer PC boards are the best solution for ground and V_{CC} connections on advanced high speed circuitry. A ground plane provides the necessary low impedance path for transient ground currents and aids in bypassing V_{CC} .

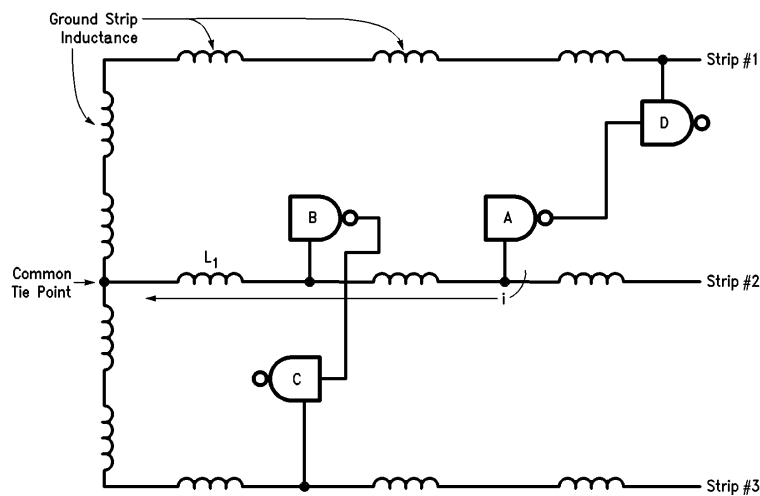


FIGURE 3-19. Ground Trace Coupling

TL/F/9607-33

Ground trace noise coupling is illustrated by a model circuit in *Figure 3-19*. With the ground comb configuration, the ground strips may be shown to contain distributed inductance, as is indeed the case. Referring to *Figure 3-19* we can see that if we switch gate A from HIGH to LOW, the current for the transition is drawn from ground strip number two. Current flows in the direction indicated by the arrow to the common tie point. It can be seen that gate B shares ground strip number two with gate A from the point where gate B is grounded back to the common tie point. This length is represented by L1. When A switches states there is a current transient which occurs on the ground strip in the positive direction. This current spike is caused by the ground strip inductance and it is “felt” by gate B. If gate B is in a LOW state (V_{OL}) the spike will appear on the output since gate B's V_{OL} level is with reference to ground. Thus if gate B's ground reference rises momentarily V_{OL} will also rise. Consequently, if gate B is output to another gate (C in the illustration) problems may arise.

Supply Voltage and Temperature

The normal supply voltage V_{CC} for all TTL circuits is +5.0V. Commercial grade parts are guaranteed to perform with a $\pm 10\%$ supply tolerance (± 500 mV) over an ambient temperature range of 0°C. Military grade parts are guaranteed to perform with $\pm 10\%$ supply tolerance (± 500 mV) over an ambient temperature range of -55°C to +125°C.

The actual junction temperature can be calculated by multiplying the power dissipation of the device with the thermal resistance of the package and adding it to the measured ambient temperature T_A or package (case) temperature T_C . For example, a device in ceramic DIP (θ_{JA} 100°C/W) dissipates typically 145 mW. At +55°C ambient temperature, the junction temperature is

$$T_J = (0.145 \times 100) + 55^\circ\text{C}$$

Designers should note that localized temperatures can rise well above the general ambient in a system enclosure. On a large PC board mounted in a horizontal plane, for example, the local temperature surrounding an IC in the middle of the board can be quite high due to the heating effect of the

surrounding packages and the very poor natural convection. Low velocity forced air cooling is usually sufficient to alleviate such localized static air conditions.

Interfacing

All TTL circuits are compatible, and any TTL output can drive a certain number of TTL inputs. There are only subtle differences in the worst-case noise immunity when low power, standard and Schottky TTL circuits are intermixed. Open-collector outputs, however, require a pull-up resistor to drive TTL inputs reliably.

While TTL is the dominating logic family, and many systems use TTL exclusively, there are cases where different semiconductor technologies are used in one system, either to improve the performance or to lower the cost, size and power dissipation. The following explains how TTL circuits can interface with ECL, CMOS and discrete transistors.

Interfacing TTL and ECL—Mixing ECL and TTL logic families offers the design engineer a new level of freedom and opens the entire VHF frequency spectrum to the advantages of digital measurement, control and logic operation.

The main advantages gained with ECL are high speed, flexibility, design versatility and transmission line compatibility. But application and interfacing cost problems have traditionally discouraged the use of ECL in many areas, particularly in low cost, less sophisticated systems.

The most practical interfacing method for smaller systems involves using a common supply of +5.0V to +5.2V. Care must be exercised with both logic families when using this technique to assure proper bypassing of the power supply to prevent any coupling of noise between circuit families. When larger systems are operated on a common supply, separate power buses to each logic family help prevent problems. Otherwise, good high frequency bypassing techniques are usually sufficient.

ECL devices have high input impedance with input pull-down resistors (> 20 k Ω) to the negative supply. In the TTL to ECL interface circuits in *Figure 3-20*, it is assumed that the ECL devices have high input impedance.

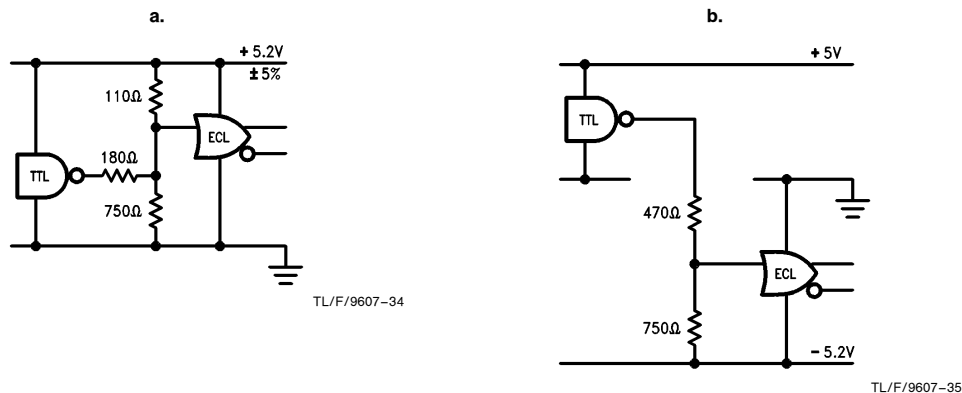


FIGURE 3-20. TTL-to-ECL Conversion

All circuits described operate with $\pm 5\%$ ECL and $\pm 10\%$ TTL supply variations, except those with ECL and TTL on a common supply. In those cases, the supply can be $\pm 10\%$ with ECL. All resistors are $\frac{1}{4}W$, $\pm 5\%$ composition type.

TTL to ECL conversion is easily accomplished with resistors, which simultaneously attenuate the TTL signal swing, shift the signal levels, and provide low impedance for damping and immunity to stray noise pick-up. The resistors should be located as near as possible to the ECL circuit for optimum effect. The circuits in Figure 3-20 assume an unloaded TTL gate as the standard TTL source. ECL input impedance is predominantly capacitive (approximately 3 pF); the net RC time constant of this capacitance with the indicated resistors assures a net propagation delay governed primarily by the TTL signal.

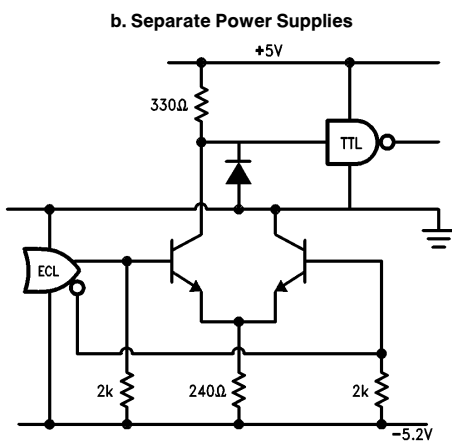
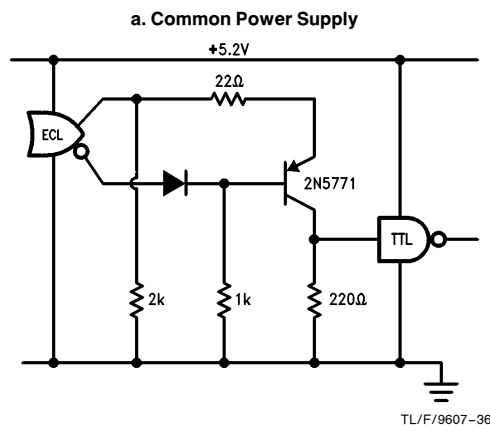


FIGURE 3-21. ECL-to-TTL Conversion

When interfacing between high voltage swing TTL logic and low voltage swing ECL logic, the more difficult conversion is from ECL to TTL. This requires a voltage amplifier to build up the 0.8V logic swing to a minimum of 2.5V. The circuits shown in Figure 3-21 may be used to interface from ECL to TTL.

The higher speed converters usually have the lowest fan-out: only one or two TTL gates. This fanout can be increased simply by adding a TTL buffer gate to the output of the converter. Another option, where ultimate speed is required, is to use additional logic converters.

Interfacing FAST/FASTr and CMOS—Due to their wide operating voltage range, CMOS devices will function outside of the standard $\pm 5V \pm 10\%$ supply levels. For our purposes, only the case where both the FAST and CMOS devices are connected to the same voltage source will be considered.

FAST outputs can sink at least 20 mA in the LOW state. This is more than adequate to drive CMOS inputs to a valid LOW level. Due to their output designs, though, FAST outputs are unable to pull CMOS inputs to above approximately 4.0V. If the CMOS device does not have TTL-compatible input levels, the FAST output should be pulled with a resistor to V_{CC} . The value of this resistor will vary according to the system. Factors that affect the selection of the value are: edge rate—the smaller the resistor, the faster the edge rate; fanout—the smaller the resistor, the greater the fanout; and noise margins—the smaller the resistor, the greater the output HIGH noise margin and the smaller the output LOW noise margin. FAST outputs can directly drive TTL-compatible CMOS inputs, such as the inputs on ACT or HCT devices, without pull up registers.

Most CMOS outputs are capable of directly driving FAST inputs. Be aware, though, that TTL inputs have higher loading specifications than CMOS inputs. Care must be taken to insure that the CMOS outputs are not overloaded by the FAST input loading.

TTL Driving Transistors—Although high voltage, high current ICs are available, it is sometimes necessary to control greater currents or voltages than integrated circuits are capable of handling. When this condition arises, a discrete transistor with sufficient capacity can be driven from a TTL output. Discrete transistors are also used to shift voltages from TTL levels to logic levels for which a standard interface driver is not available.

The two circuits of Figure 3-22 show how TTL can drive npn transistors. The first circuit is the most efficient but requires an open-collector TTL output. The other circuit limits the output current from the TTL totem pole output through a series resistor.

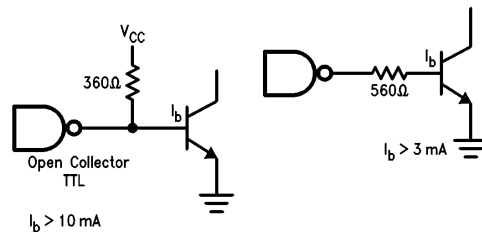


FIGURE 3-22. TTL Driving npn Transistors

TL/F/9607-38

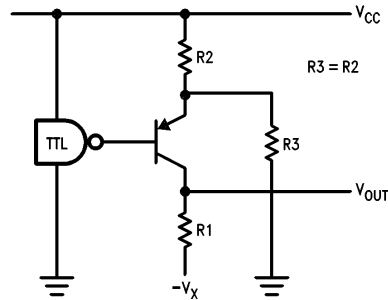


FIGURE 3-23. pnp Transistor Shifting TTL Output

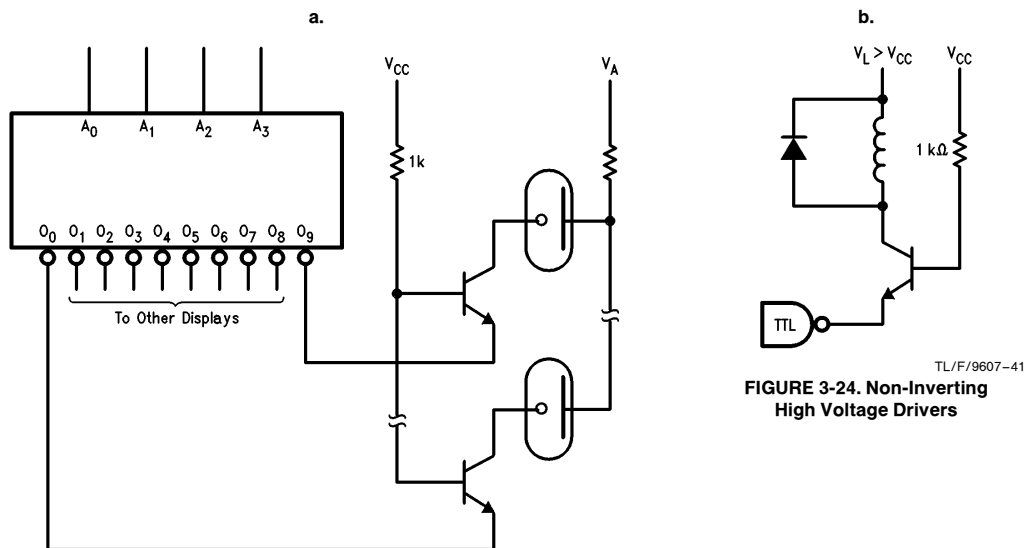
TL/F/9607-39

Shifting a TTL Output to Negative Levels—The circuit of *Figure 3-23* uses a pnp transistor to shift the TTL output to a negative level. When the TTL output is HIGH, the transistor is cut off and the output voltage is $-V_x$. When the TTL output is LOW, the transistor conducts and the output voltage is

$$V_{OUT} = -V_x + R_1/R_2 (V_{CC} - 2.0V)$$

if the transistor is not saturated, or slightly positive if the transistor is allowed to saturate.

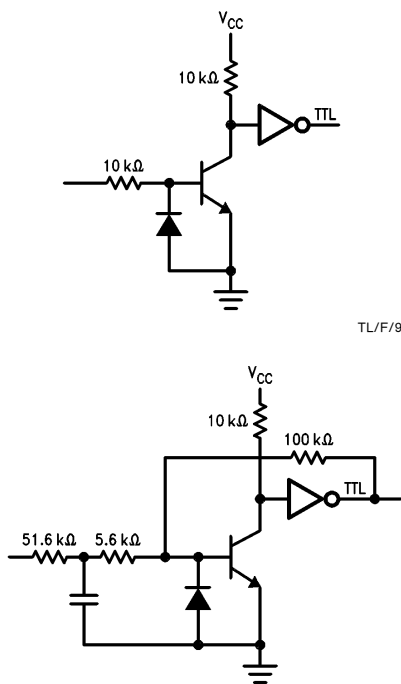
High Voltage Drivers—A TTL output can be used to drive high voltage, low current loads through the simple, non-inverting circuits shown in *Figure 3-24*. This can be useful for driving gas discharge displays or small relays, where the TTL output can handle the current but not the voltage. Load current should not exceed I_{OL} (-4 mA).



TL/F/9607-40

TL/F/9607-41

FIGURE 3-24. Non-Inverting High Voltage Drivers



TL/F/9607-42

TL/F/9607-43

FIGURE 3-25. Transistors Driving TTL

Transistors Driving TTL—It is sometimes difficult to drive the relatively low impedance and narrow voltage range of TTL inputs directly from external sources, particularly in a rough, electrically noisy environment. The circuits shown in *Figure 3-25* can handle input signal swings in excess of $\pm 100\text{V}$ without harming the circuits. The second circuit has input RC filter that suppresses noise. Unambiguous TTL voltage levels are generated by the positive feedback (Schmitt trigger) connection.

OPEN COLLECTOR OUTPUTS

A number of available circuits have no pull-up circuit on the outputs. Open collector outputs are used for interfacing or for wired-OR (actually wired-AND) functions. The latter is achieved by connecting open collector outputs together and adding an external pull-up resistor.

The value of the pull-up resistor is determined by considering the fanout of the OR tie and the number of devices in the OR tie. The pull-up resistor value is chosen from a range between maximum value (established to maintain the required V_{OH} with all the OR-tied outputs HIGH) and a minimum value (established so that the OR tie fanout is not exceeded when only one output is LOW).

MINIMUM AND MAXIMUM PULL-UP RESISTOR VALUES

$$R_{X(MIN)} = \left(\frac{V_{CC(MAX)} - V_{OL}}{I_{OL} - N_2(LOW) \bullet 1.6 \text{ mA}} \right)$$

$$R_{X(MAX)} = \left(\frac{V_{CC(MIN)} - V_{OH}}{N_1 I_{OH} + N_2(HIGH) \bullet 40 \mu A} \right)$$

where:

R_X = External pull-up resistor

N_1 = Number of wired-OR outputs

N_2 = Number of input unit loads being driven

$I_{OH} = I_{CEX}$ = Output HIGH leakage current

I_{OL} = LOW level fanout current of driving element

V_{OL} = Output LOW voltage level (0.5V)

V_{OH} = Output HIGH voltage level (2.5V)

V_{CC} = Power Supply Voltage

Example: four 'F524 gate outputs driving four other gates or MSI inputs.

$$R_{X(MIN)} = \left(\frac{5.5V - 0.5V}{8.0 \text{ mA} - 2.4 \text{ mA}} = \frac{5.0V}{5.6 \text{ mA}} \right) = 893\Omega$$

$$R_{X(MAX)} = \left(\frac{4.5V - 2.5V}{4 \bullet 250 \mu A + 2 \bullet 40 \mu A} = \frac{2.0V}{1.08 \text{ mA}} \right) = 1852\Omega$$

where:

$$N_1 = 4$$

$$N_2(HIGH) = 4 \bullet 0.5 \text{ U.L.} = 2 \text{ U.L.}$$

$$N_2(LOW) = 4 \bullet 0.375 \text{ U.L.} = 1.5 \text{ U.L.}$$

$$I_{OH} = 250 \mu A$$

$$I_{OL} = 8.0 \text{ mA}$$

$$V_{OL} = 0.5V$$

$$V_{OH} = 2.5V$$

Any values of pull-up resistor between 893 Ω and 1852 Ω can be used. The lower values yield the fastest speeds while the higher values yield the lowest power dissipation.

INCREASING FANOUT

To increase fanout, inputs and outputs of gates on the same package may be paralleled to those in a single package to avoid large transient supply currents due to different switching times of the gates. This is not detrimental to the devices, but could cause logic problems if the gates are being used as clock drivers.

UNUSED INPUTS

Theoretically, an unconnected input assumes the HIGH logic level, but practically speaking it is in an undefined logic state because it tends to act as an antenna for noise. Only a few hundred millivolts of noise may cause the unconnected input to go to the logic LOW state. On devices with memory (flip-flops, latches, registers, counters), it is particularly important to terminate unused inputs (MR, PE, PL, CP) properly since a noise spike on these inputs might change the contents of the memory. It is a poor design practice to leave unused inputs floating.

If the logic function calls for a LOW input, such as in NOR or OR gates, the input can be connected directly to ground. For a permanent HIGH signal, unused inputs can be tied directly to V_{CC} . An unused input may also be tied to a used input having the same logic function, such as NAND and AND gates, provided that the driver can handle the added I_{IH} . This practice is not recommended for diode-type inputs in a noisy environment, since each diode represents a small capacitor and two or more in parallel can act as an entry port for negative spikes superimposed on a HIGH level and cause momentary turn-off of Q2.

LIFE SUPPORT POLICY

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

 National Semiconductor Corporation 2900 Semiconductor Drive P.O. Box 58090 Santa Clara, CA 95052-8090 Tel: 1(800) 272-9959 TWX: (910) 339-9240	National Semiconductor GmbH Livny-Gargan-Str. 10 D-82256 Fürstenfeldbruck Germany Tel: (81-41) 35-0 Telex: 527849 Fax: (81-41) 35-1	National Semiconductor Japan Ltd. Sumitomo Chemical Engineering Center Bldg. 7F 1-7-1, Nakase, Mihama-Ku Chiba-City, Ciba Prefecture 261 Tel: (043) 299-2300 Fax: (043) 299-2500	National Semiconductor Hong Kong Ltd. 13th Floor, Straight Block, Ocean Centre, 5 Canton Rd. Tsimshatsui, Kowloon Hong Kong Tel: (852) 2737-1600 Fax: (852) 2736-9960	National Semicondutores Do Brazil Ltda. Rue Deputado Lacorda Franco 120-3A Sao Paulo-SP Brazil 05418-000 Tel: (55-11) 212-5066 Telex: 391-1131931 NSBR BR Fax: (55-11) 212-1181	National Semiconductor (Australia) Pty, Ltd. Building 16 Business Park Drive Monash Business Park Nottingham, Melbourne Victoria 3168 Australia Tel: (3) 558-9999 Fax: (3) 558-9998
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