Burst Performance and Burst Transfer Behavior for the NS32GX32 and NS32532

National Semiconductor
Application Note 630
Zeev Bikowsky, Aharon Ostrer
July 1989

INTRODUCTION

The NS32GX32 burst mode is a mechanism for increasing the bus transfer rate. Implementing the burst mode enables the CPU to read 4 double words in 5 cycles. During nonburst mode, on the other hand, the CPU can read 4 double words in eight cycles (1 double word every two cycles).

Burst is important because it increases the bus bandwidth and frees the bus for other transactions. This is particularly useful during instruction fetches and data reads from 32-bit buses.

The NS32GX32 burst mode may be implemented with a number of different options. These include Instruction Cache (IC) on/off, data reference cacheable/non cacheable, wait states, etc . . . , and other events that enable the user to tune the CPU performance to his application needs.

This application note describes how to use the NS32GX32 during burst mode. the first part describes those parameters that affect burst performance. The second part presents those events that affect burst behavior.

Note that all features described in this application note also apply to the NS32532.

BACKGROUND

The NS32GX32 microprocessor communicates with its environment via parallel busses and signals. These include a 32-bit data bus, a 32-bit address bus, a number of control signals and five bus status pins.

The processor has instruction and data caches. The on-chip caches duplicate a subset of external memory. The contents of an on-chip cache are acquired in one clock cycle, while it takes a minimum of two clocks to fetch data from external memory. Therefore, on-chip caches substantially reduce average memory access time when they contain the code and data the processor needs.

On each memory access, the processor initiates a memory access cycle while searching the internal cache. This reduces access time, since the memory cycle is already in process when the cache does not contain the needed information. During a read that fails to find the data in the cache (a cache miss), the memory cycle continues and the processor fetches the data from external memory. Unless declared non-cacheable, the information is placed in the internal instruction or data cache for future reference. Conversely, when the instruction or data cache contains the sought information (a cache hit), the processor cancels the memory access cycle.

A memory write is always treated as a cache miss, so that external memory is updated: this is a ''write through'' cache policy. When an internal cache contains a copy of the memory location being updated, the processor also updates the cache using a ''write allocate'' cache policy, thus ensuring that both copies of the data are the same.

The NS32GX32 is capable of performing burst transfers, which increase bus efficiency and tend to raise the internal cache hit rate. Burst is only available in instruction fetch and data read cycles from 32-bit memories.

A burst cycle consists of two parts. The first is a regular (opening) cycle, in which the processor outputs its status and asserts the relevant control signals. The processor asserts $\overline{\text{BOUT}}$ to indicate that it wants to perform burst cycles. If the selected memory supports burst mode, it notifies the processor via $\overline{\text{BIN}}$ low. If the memory does not allow burst ($\overline{\text{BIN}}$ high) and the cycle extension has not been requested via $\overline{\text{RDY}}$, the memory cycle terminates at the end of T2 and the processor deasserts $\overline{\text{BOUT}}$. If the memory supports burst and the processor has not deasserted $\overline{\text{BOUT}}$, the second part of the burst cycle occurs and $\overline{\text{BOUT}}$ remains active until termination of the operation.

The second part of the burst consists of up to three nibbles in state T2B. In each of these nibbles, the processor reads a 32-bit data item. After each data read, address bits A_0–A_1 go to zero and A_2–A_3 increment, and all byte enable outputs $\overline{\text{BE}}_0$–$\overline{\text{BE}}_3$ are activated. If the $\overline{\text{RDY}}$ pin is high at the end of each T2B, the processor inserts additional T2B states to allow slow memories to work with the burst cycle.

DESCRIPTION

The following parameters affect burst performance:

1. Instruction Cache on/off. The Instruction cache (IC) is set **on** or **off** through the IC bit in the CFG register. Although the best burst results are achieved when the IC is on, it is still possible to increase performance by 26% (based on the dhrystone benchmark) even when the IC is off. This is because the IC's internal 16 byte buffer remains active regardless of whether the cache is active or not (Table I).
2. Cacheable/non-cacheable Data References when the data cache is **on**. Using burst mode when data references are not cacheable will generate lower performance than non-burst mode. According to Tables I and II, this degradation is 8.8% because the effect of the burst is like 3 wait states even when the data cache is **on** during non-cacheable mode. Only one double word is used out of four.
3. Wait States. The internal bus interface makes it possible to assert wait states during any burst cycle. When using interleaved memory when address to data time is insufficient, it is advisable to assert RDY only in the first transaction of the burst (Diagram 4). According to Table III, one wait state on every burst transaction (as compared to one wait state on the first transaction only) will decrease performance by 5.3%.

RRD-B30M75/Printed in U. S. A.

TABLE I. DHRYSTONE Performance @ 30 MHz with DC OFF and IC OFF (Million Loops/Sec)

Burst OFF	Burst ON
9683	12240

TABLE II. DHRYSTONE Performance with DC ON and IC OFF, Non-Cacheable Data References and Instruction Fetches

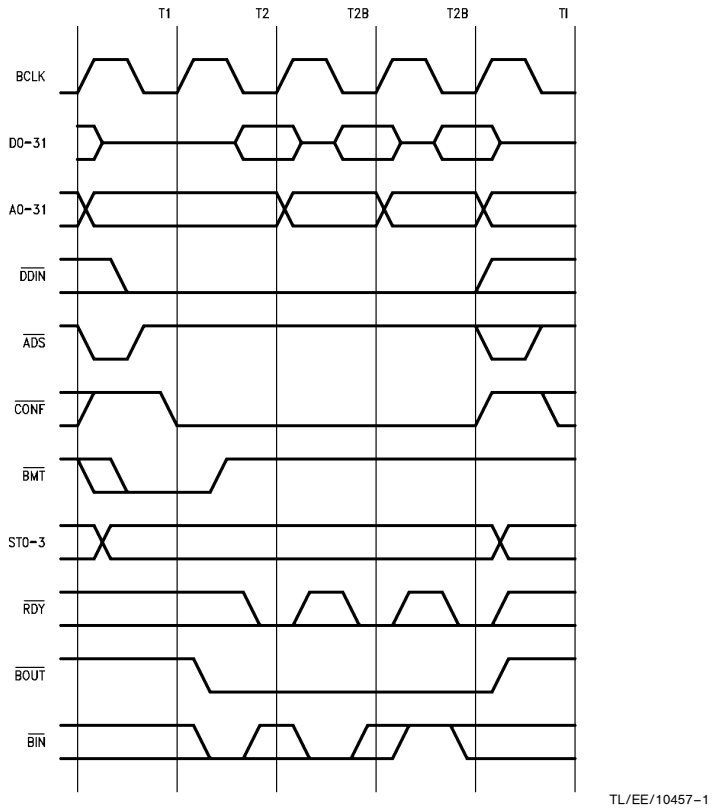
Burst OFF	Burst ON
9683	11250

TABLE III. DHRYSTONE Performance with DC on and Other Parameters Varied

IC	Wait States	Burst	DHRYSTONE Performance @ 30 MHz
OFF	0	OFF	10338
OFF	0	ON	14166
OFF	1 Every 1st Trans	OFF	8999
OFF	1 Every 1st Trans	ON	13190
OFF	1 Every Transaction	OFF	8999
OFF	1 Every Transaction	ON	12338
ON	0	OFF	13540
ON	0	ON	17000
ON	1 Every 1st Trans	OFF	12240
ON	1 Every 1st Trans	ON	16276
ON	1 Every Transaction	OFF	12240
ON	1 Every Transaction	ON	15454

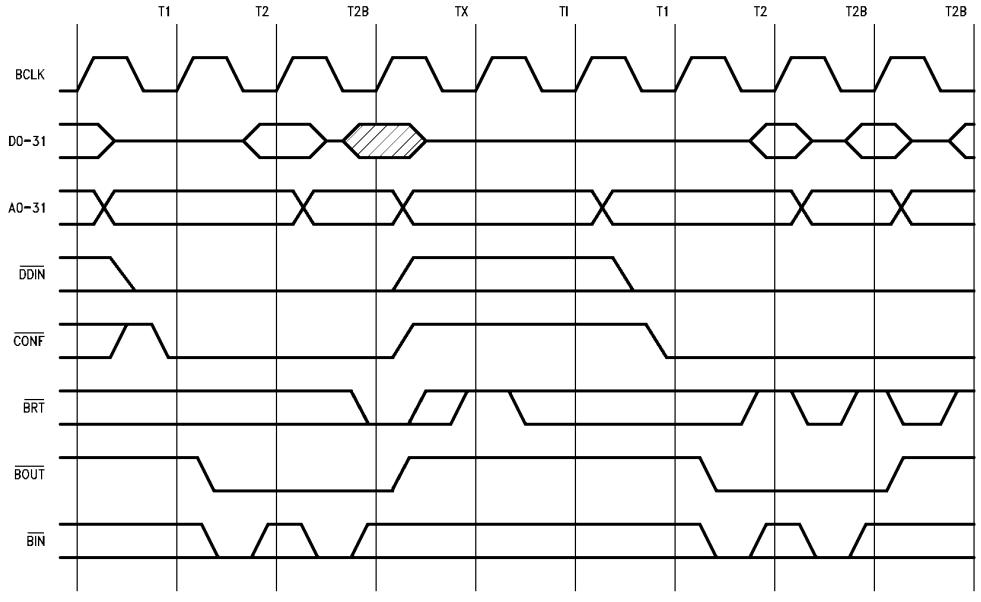
The following events affect burst behavior:

1. $\overline{\text{BIN}}$: deasserting $\overline{\text{BIN}}$ stops burst mode even in the middle of the entry (diagram 1). Note that an entry equals four doubles words, where each double word is 4 bytes. Thus, an entry equals 16 bytes.
2. BW0−1: Burst is only allowed when BW0−1 = 3. When this is the case, bus width is a double word (4 bytes).
3. $\overline{\text{IODEC}}$: Asserting $\overline{\text{IODEC}}$ forces non-burst mode.
4. $\overline{\text{BRT}}$: Retry can be asserted during any burst cycle. The next burst cycle will be cancelled and the current cycle will be reissued (diagram 2).
5. $\overline{\text{BER}}$: (Bus Error)—The bus error indication is latched internally, the burst continues normally on the system bus, but the data that was read after the assertion of BER is discarded (diagram 3).
6. Program flow alteration e.g. BR instruction or exception. All instruction fetches or data reads that follow an exception or any alteration of the program flow are ignored. The situation is indicated by de-asserting $\overline{\text{BOUT}}$ (diagram 5).



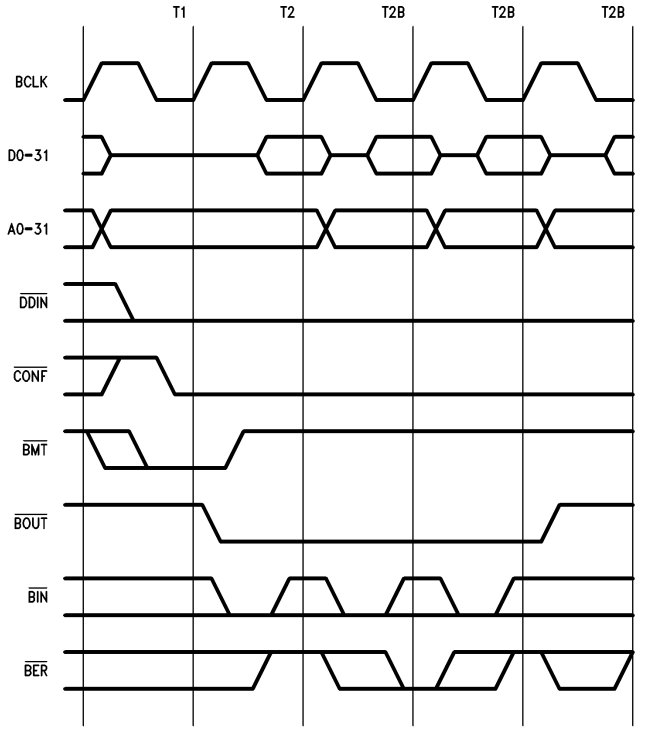
TL/EE/10457–1

DIAGRAM 1. Stop Burst with BIN Inactive



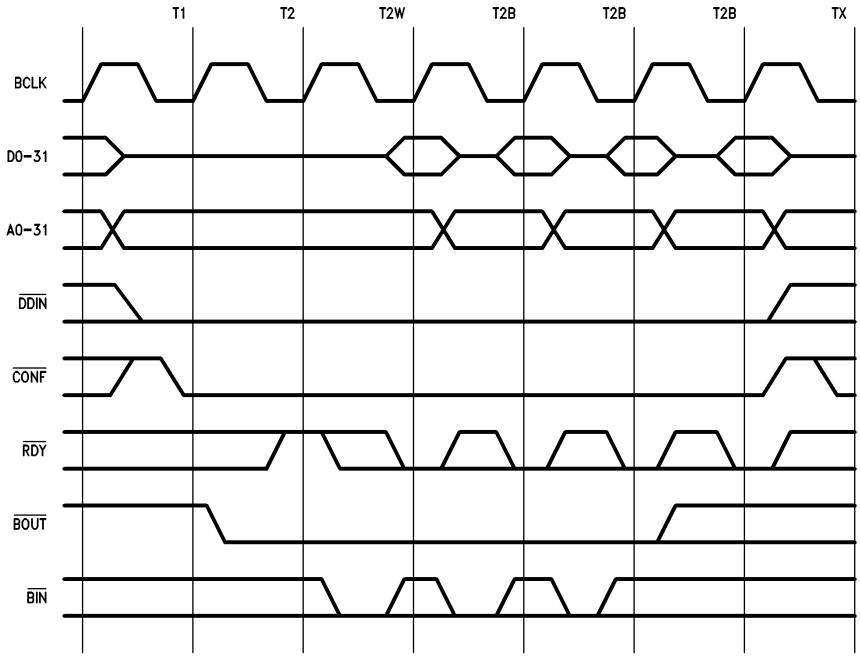
TL/EE/10457–2

DIAGRAM 2. Retry on Burst Transaction



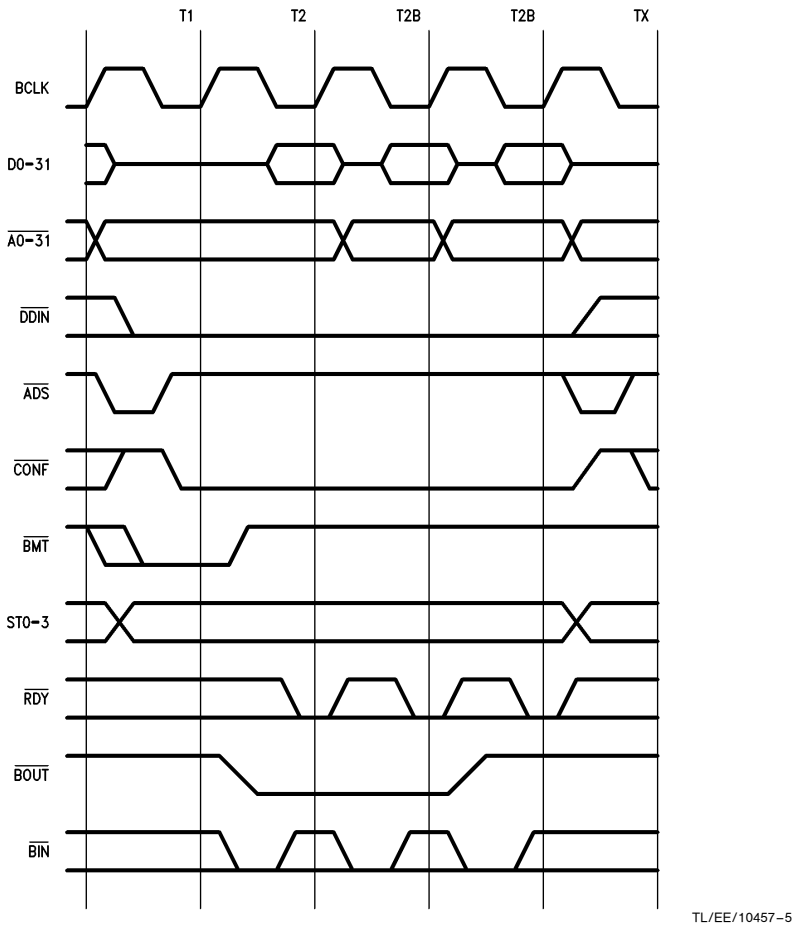
TL/EE/10457–3

DIAGRAM 3. Bus Error during Burst Transaction



TL/EE/10457–4

DIAGRAM 4. Burst with One Wait State on the First Transaction



TL/EE/10457–5

DIAGRAM 5. Stop Burst because of Internal Cancel

Lit. # 100630

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090
Tel: 1(800) 272-9959
TWX: (910) 339-9240

National Semiconductor GmbH
Livry-Gargan-Str. 10
D-82256 Fürstenfeldbruck
Germany
Tel: (81-41) 35-0
Telex: 527649
Fax: (81-41) 35-1

National Semiconductor Japan Ltd.
Sumitomo Chemical
Engineering Center
Bldg. 7F
1-7-1, Nakase, Mihama-Ku
Chiba-City,
Ciba Prefecture 261
Tel: (043) 299-2300
Fax: (043) 299-2500

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductores Do Brazil Ltda.
Rue Deputado Lacorda Franco
120-3A
Sao Paulo-SP
Brazil 05418-000
Tel: (55-11) 212-5066
Telex: 391-1131931 NSBR BR
Fax: (55-11) 212-1181

National Semiconductor (Australia) Pty, Ltd.
Building 16
Business Park Drive
Monash Business Park
Nottinghill, Melbourne
Victoria 3168 Australia
Tel: (3) 558-9999
Fax: (3) 558-9998