Interfacing the DP8420A/21A/22A to the 80386 (Zero Wait State Burst Mode Access)

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INTRODUCTION

This application note describes how to interface the 80386 microprocessor to the DP8422A DRAM controller (also applicable to DP8420A/21A) with burst mode access. The 80386 is running at 16 MHz, 20 MHz, or 25 MHz speed. It is assumed that the reader is familiar with the 80386 and DP8422A modes operation.

DESCRIPTION

Two designs in this application note are provided to support page mode access in interfacing the DP8422A to the 80386 microprocessor. The DP8422A is operated in Mode 1 in both designs. An access cycle begins when the 80386 places a valid address on the address bus and asserts the Address Strobe (/ADS) if a refresh or Port B (DP8422A only) access is not in progress. During the burst access all /RAS's are kept low while toggling /CAS's. The burst access can be terminated when out of page signal is detected. The High Speed Access (/HSA) output signal of page detector (ALS6311) is used as an out of page signal to indicate whether the current access is in the same page as previous access or not. In other words, the row and bank select addresses have been changed from one access to the next.

I. Design #1 Description

This design simply consists of a DP8422A DRAM controller, a page detector (ALS6311), and two PALs (386PALN1 and 386PALN2). THE 386PALN1 is used to generate /CAS's and /WE signals. Where the 386PALN2 is to generate /ADS (or /AREQ), /NA, and /READY signals. This design can accommodate two banks of DRAM, 32 bits in each bank, giving a maximum memory capacity of 8 Mbytes (1M x 1 DRAMs) or 32 Mbytes (4M x 1 DRAMs). The schematic diagram is shown in *Figure 1*.

II. Design #2 Description

This design consists of the DP8422A DRAM controller, a page detector (ALS6311), a count up and down counter (F169), two 20R4D PALs, and two 16R4D PALs. The count up and down counter is to hold the number of refresh being missed. The maximum missed refreshes are six to guarantee /RAS pulse width maximum timing (t_{RASP} = 100 μs). The external refresh control logic forces DRAM controller to initiate refresh as soon as the 80386 is not accessing the memory. 386PAL1 is used to generate /ECAS(3:0) and /BED(3:0) signals. 386PAL2 is to generate /ADS, /AREQ, /NA, and some intermediate signals. 386PAL3 is to generate /MOE, /RFSHCK, and /RFIPDn signals. 386PAL4 is to generate /WE, /READY, and some intermediate signals. The schematic diagram is shown in *Figure 5*. Two designs, based upon the load capacity, are described in the following:

A. Design #2 Description for Light Load

This design interface the DP8422A to the 80386 that can accommodate two banks of DRAM, each bank being 32 bits in width, giving a maximum memory capacity of 2 Mbytes (256k by 4 DRAM). During read or write burst access cycles, zero wait state can be achieved when the 80386 is running up to 25 MHz. /MOE is tied to /OE of DRAM for /OE controlled write access. Transceivers were eliminated in this design for gaining speed. During nonburst or initial access cycles that one, two, or three wait states are required depending upon the speed of the system clock.

B. Design #2 Description for Heavy Load

This design is to interface the DP8422A to the 80386 and up to 8 Mbytes (1 Mbits DRAM) or 32 Mbytes (4 Mbits DRAM) memory. Zero wait state can be achieved during read burst access cycle. During write burst access cycles, one wait state has to be inserted to the 80386 bus cycle in order to guarantee data valid before /CAS going low and column address hold time after /CAS going low. One, two, or three wait states are required for microprocessor to read or write valid data during nonburst or initial access cycles. The number of required wait states depends upon the speed of the system clock.

PROGRAMMING MODE BITS FOR DESIGN #1 AND #2

u = User Define x = Don't Care

Programming Bits		Description
R9	= u	Stagger or /RAS Refresh
R8	= 1	Noninterleaved Mode
R7	= 1	/DTACK is selected
R6	= x	/WAITIN Controlled /DTACK High
R5, R4	= 1, 1	No Wait State during Burst Mode
R3, R2	= u, u	Wait State during Nonburst Mode
R1, R0	= u, u	/RAS Low and Precharge Time
C9	= 0	/CAS is same for READ & WRITE
C8, C7	= 1, 1	t_{RAH} 15 ns and t_{ASC} 0 ns
C6, C5, C4	= u u, u	/RAS and /CAS Configuration
C3	= 0	Refresh Clock Divider
C2, C1, C0	= u, u, u	Refresh Clock Divisor Select
B1	= 1	Mode 1 Selected
B0	= 1	Fall through Selected
/ECAS0	= 1	Extend /CAS and Refresh Request

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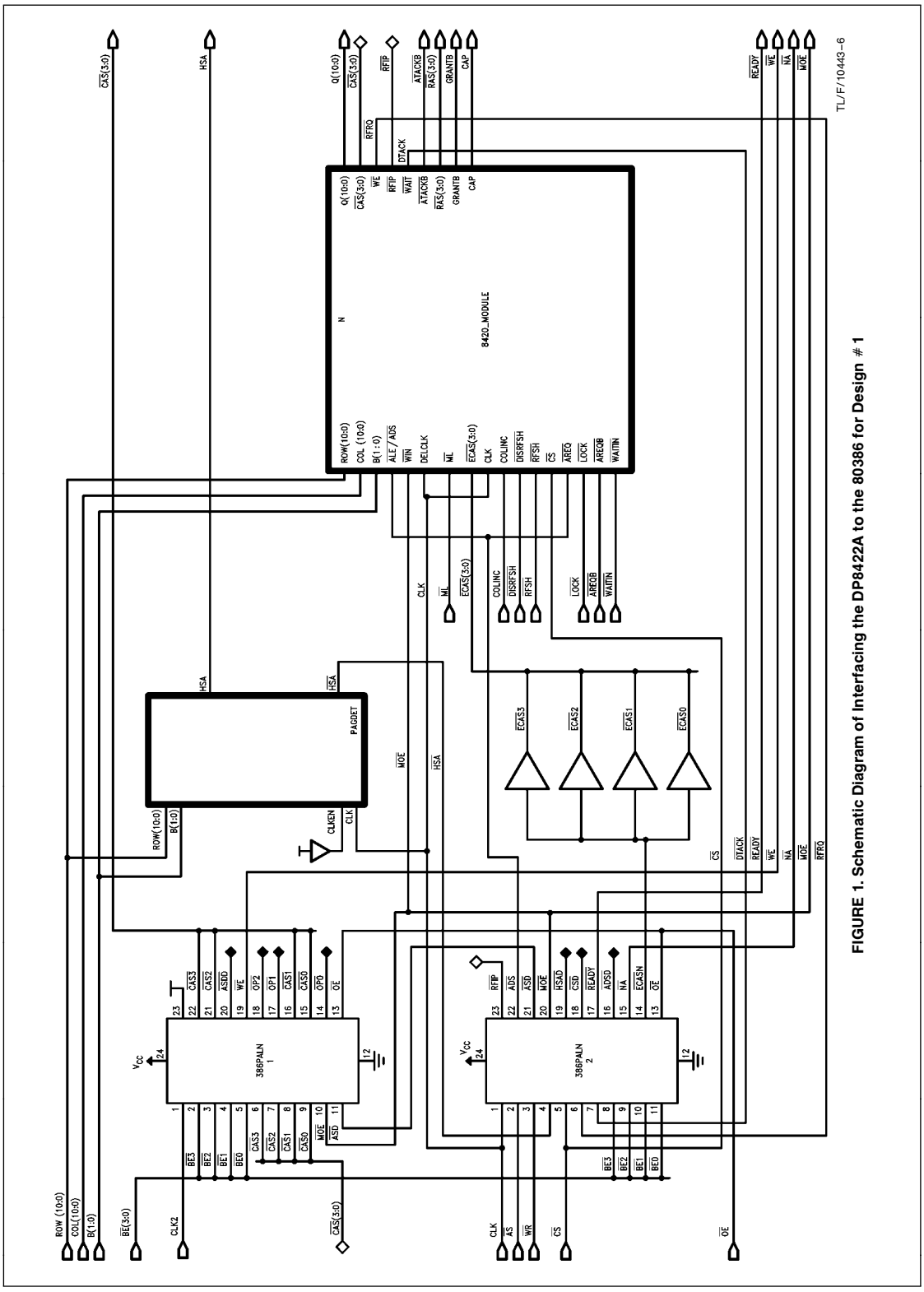

FIGURE 1. Schematic Diagram of Interfacing the DP8422A to the 80386 for Design # 1

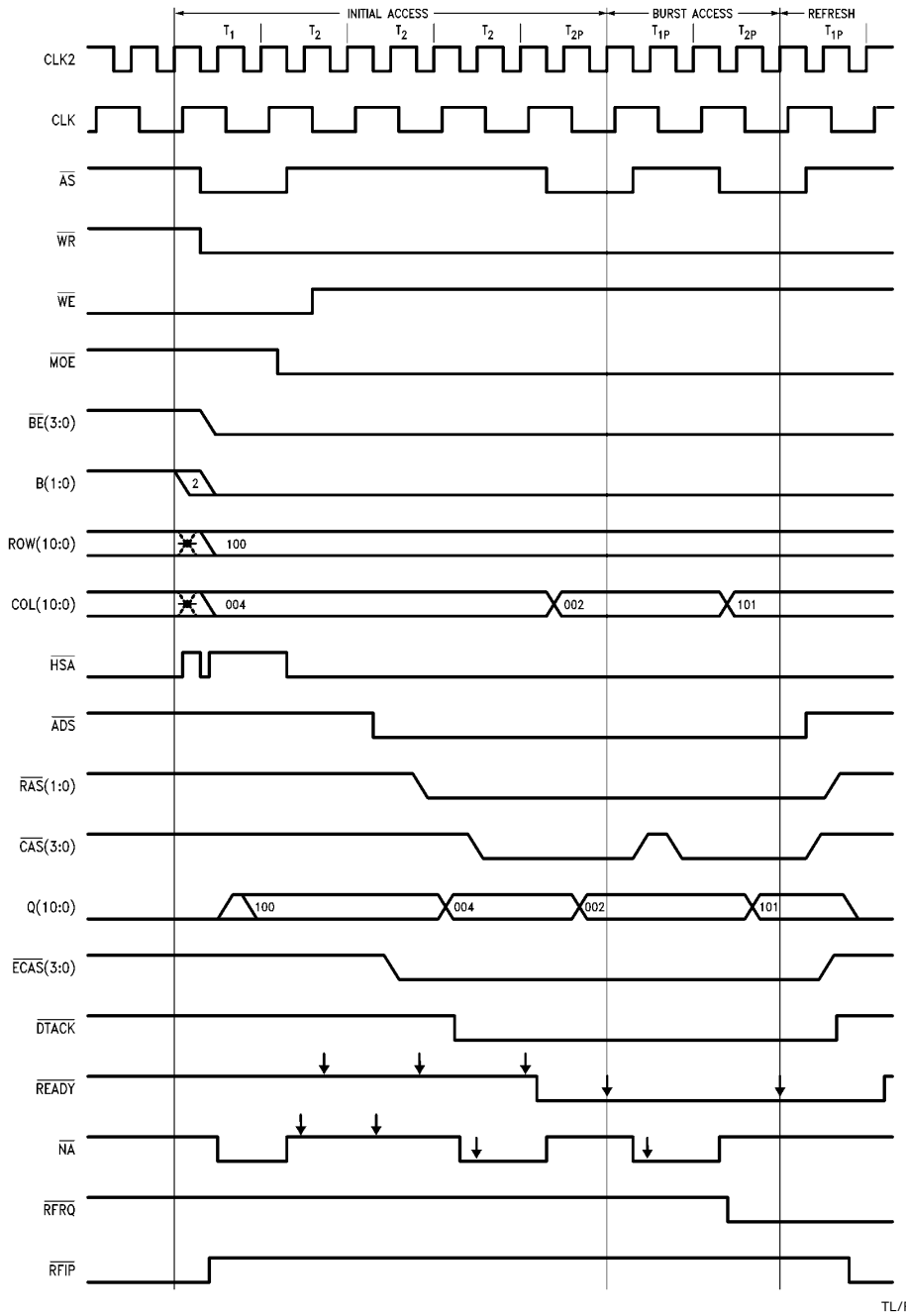

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FIGURE 2. Timing Diagram of Initial and Burst Access for Design # 1

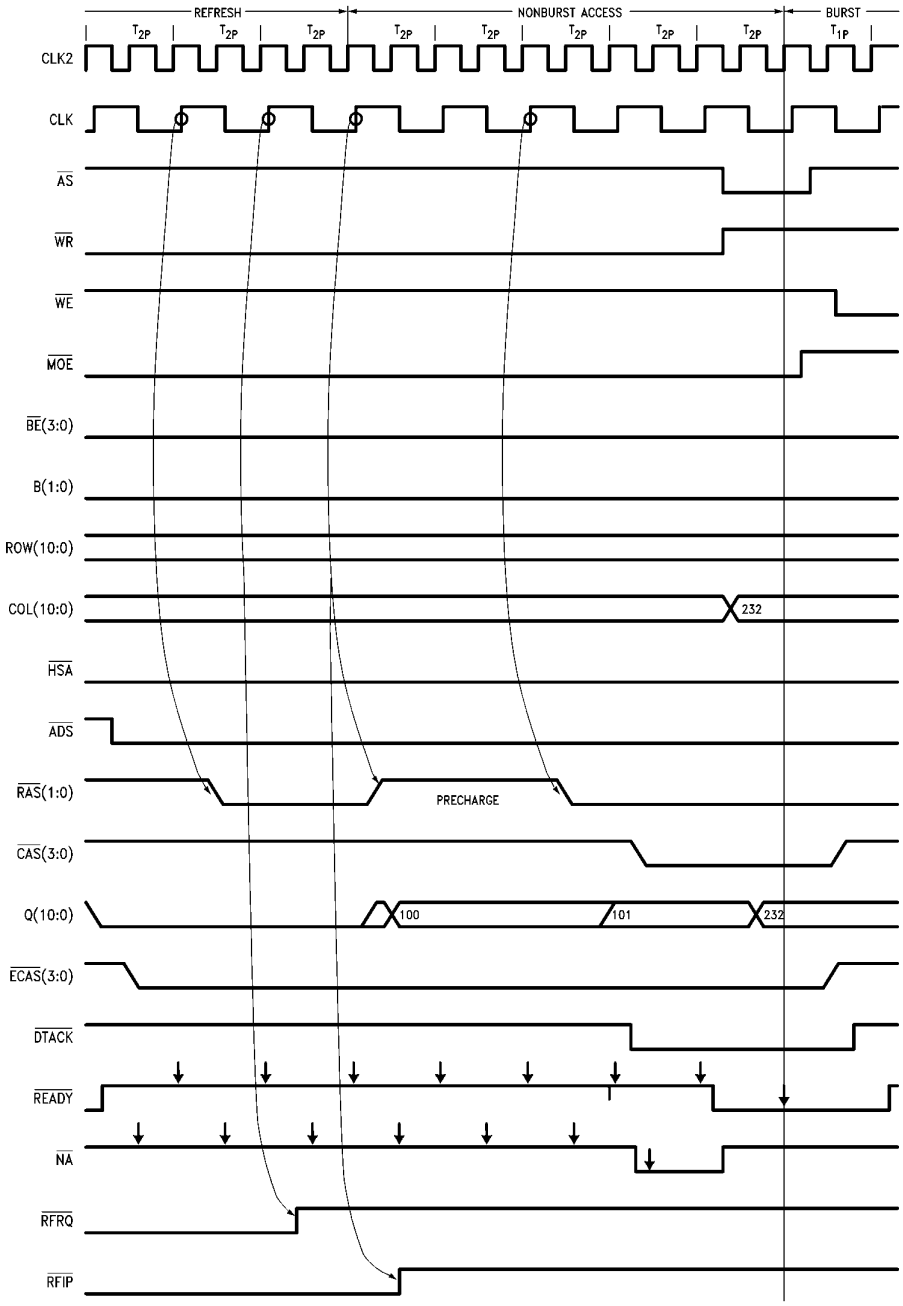

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FIGURE 3. Timing Diagram of Refresh Cycle for Design # 1

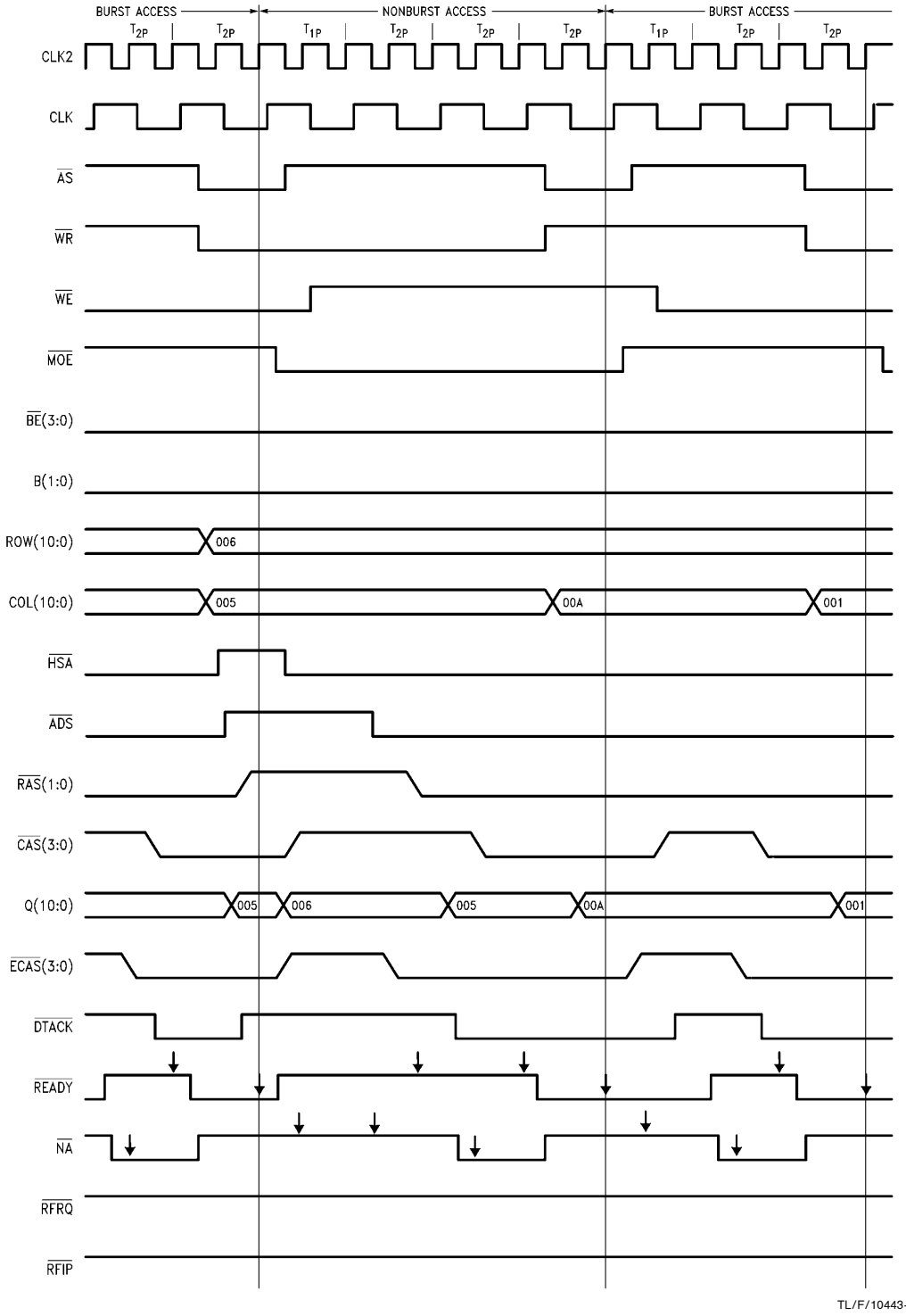

FIGURE 4. Timing Diagram of Burst and Non-Burst Access for Design # 1

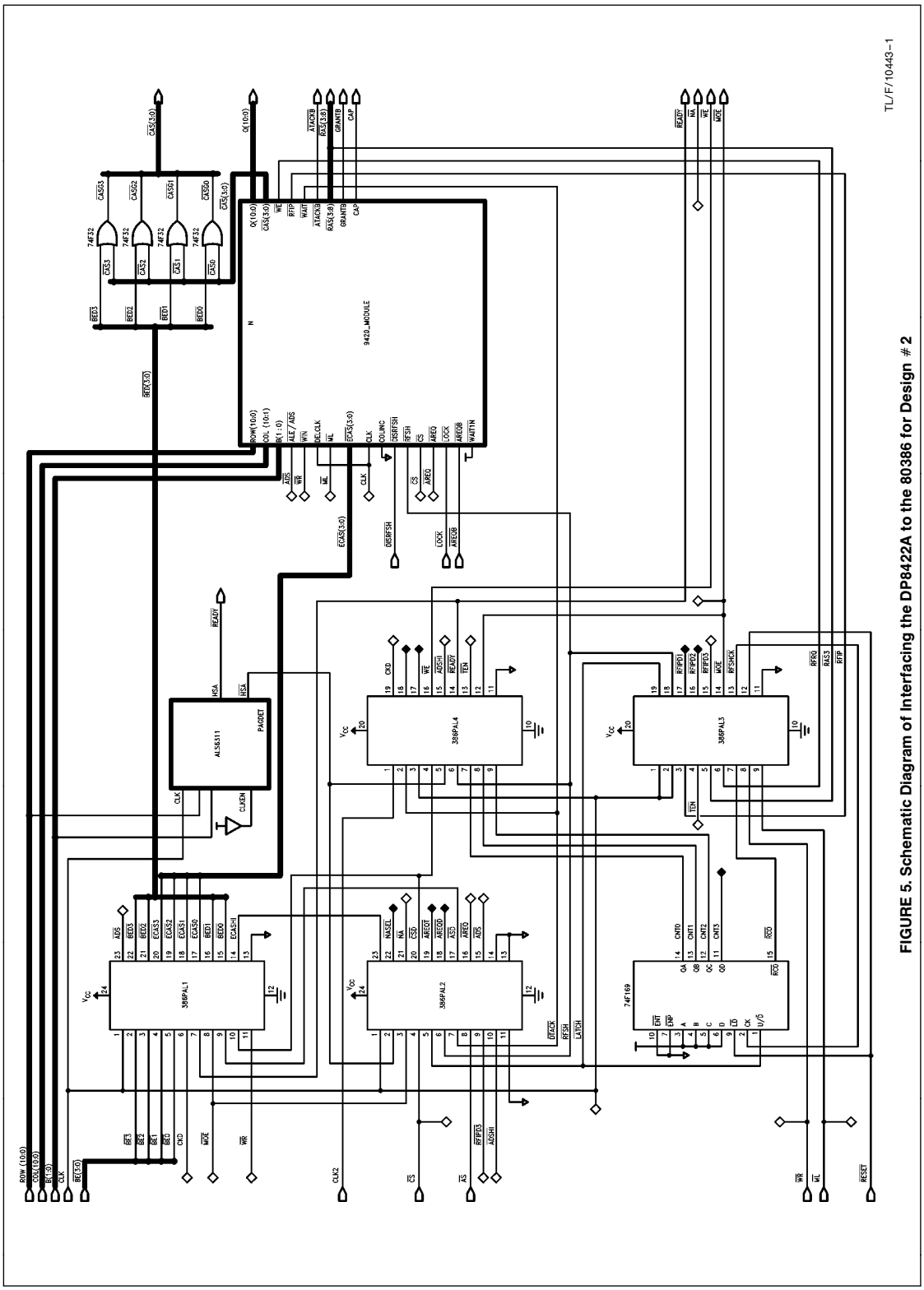

FIGURE 5. Schematic Diagram of Interfacing the DP8422A to the 80386 for Design # 2

DESIGN TIMING PARAMETERS

AC timing parameters are referred to under the heavy load when using n M x 1 or n K x 1 DRAMs, and under light load when using n M x 4 or n K x 4 DRAMs.

Times that begin with a "$" refer to DP8422A data sheet July 1988 and a "#" refer to Intel 1989 Microprocessor and Peripheral Handbook. The timing diagrams are shown in *Figure 2* through *Figure 4* and *Figure 6* through *Figure 9.* The simulation timing is based on 10 MHz clock. It may use E speed PAL for 25 MHz design.

I. Timing Calculation for Design #1

25 MHz t_{CP} = 40 ns with light load

$400b: /ADS Asserted Setup to CLK

t_{CP} − PAL20R4E CLK t_p max. − PAL20R4E t_p max.

= 40 ns − 7 ns − 8 ns = 25 ns (@ 25 MHz)

$401: /CS Setup to /ADS Asserted

2 t_{CP} + PAL20R6E CLK t_p min. + PAL20R6E t_p min. − #6 Address Valid − Decoder t_p max.

= 80 ns + 4 ns + 6 ns − 21 ns − 9 ns

= 40 ns (@ 25 MHz)

$416: /AREQ Negated to /ADS Asserted

2 t_{CP} + PAL20R6E CLK t_p min. + Skew of CLK2 and CLK min. − #6 Address Valid − /HSA t_p max.

= 80 ns + 4 ns + 3.5 ns − 21 ns − 14 ns

= 52.5 ns (@ 25 MHz)

a. Address pipelined burst mode access with 0 wait state:

t_{CAC} = 2 t_{CP} − PAL20R4E t_{CLK} max. − PAL20R4E t_p max. − #21 (Data Setup) − ½ t_{CP} − Skew of CLK2 and CLK max. − Transceiver t_p max.

= 80 ns − 7 ns − 8 ns − 7 ns − 20 ns − 10 ns − 6 ns

= 22 ns (DP8422A-25 Part)

t_{AA} = 3 t_{CP} − $26 (Address to Q Valid) − #6 (Address Valid) − #21 (Data Setup) − Transceiver t_p max.

= 120 ns − 26 ns − 21 ns − 6 ns

= 60 ns (DP8422A-25 Part)

t_{OEA} = 2 t_{CP} − PAL20R6E CLK Out t_p max. − #21 (Data Setup) − Transceiver t_p max.

= 80 ns − 7 ns − 11 ns − 6 ns

= 56 ns (DP8422A-25 Part)

b. Address pipelined nonburst mode access with 3 wait states and initial access with 4 wait states.

t_{RAC} = 4 t_{CP} − PAL20R6E t_{CLK} max. − PAL20R6E t_p max. − $402 (/ADS low to /RAS low) − #21 (Data Setup) − Skew of CLK2 and CLK t_p max. − Transceiver t_p max.

= 160 ns − 7 ns − 8 ns − 29 ns − 7 ns − 10 ns − 6 ns

= 93 ns (DP8422A-25 Part)

t_{CAC} = 4 t_{CP} − PAL20R6E t_{CLK} max. − PAL20R6E t_p max. − $403 (/ADS low to /CAS low) − #21 (Data Setup) − Skew of CLK2 and CLK t_p max. — Transceiver t_p max.

= 160 ns − 7 ns − 8 ns − 82 ns − 7 ns − 10 ns − 6 ns

= 40 ns (DP8422A-25 Part)

t_{AA} = 4 t_{CP} − PAL20R6E t_{CLK} max. − PAL20R6E t_p max. − $417 (/ADS low to Column Address valid) − #21 (Data Setup) − Skew of CLK2 and CLK t_p max. − Transceiver t_p max.

= 160 ns − 7 ns − 8 ns − 78 ns − 7 ns − 10 ns − 6 ns

= 44 ns (DP8422A-25 Part)

t_{OEA} = 5 t_{CP} − PAL20R6E t_{CLK} max. − #21 (Data Setup) − Skew CLK2 and CLK t_p max. − Transceiver t_p max.

= 200 ns − 7 ns − 7 ns − 10 ns − 6 ns

= 170 ns (DP8422A-25 Part)

II. Timing Calculation for Design #2

$400b: /ADS Asserted Setup to CLK

t_{CP} − PAL16R4D CLK t_p max. − PAL20R4D t_p max.

= 62.5 ns − 8 ns − 10 ns = 44.5 ns (@ 16 MHz)

= 50 ns − 8 ns − 10 ns = 32 ns (@ 20 MHz)

= 40 ns − 8 ns − 10 ns = 22 ns (@ 25 MHz)

$401: /CS Setup to /ADS Asserted

3 t_{CP} + PAL20R4D CLK t_p min. + PAL20R4D t_p min. − #6 Address Valid − Decoder t_p max.

= 187.5 ns + 5.5 ns + 7.1 ns − 36 ns − 9 ns

= 155 ns (@ 16 MHz)

= 150 ns + 5.5 ns + 7.1 ns − 30 ns − 9 ns

= 123.6 ns (@ 20 MHz)

= 120 ns + 5.5 ns + 7.1 ns − 21 ns − 9 ns

= 102.6 ns (@ 25 MHz)

$416: /AREQ Negated to /ADS Asserted

2 t_{CP} + PAL20R4D CLK t_p min. + Skew of CLK2 and CLK min. − #6 Address Valid − PAL20R4D t_p max.

= 125 ns + 4 ns + 3.5 ns − 36 ns − 10 ns

= 86.5 ns (@ 16 MHz)

= 100 ns + 4 ns + 3.5 ns − 30 ns − 10 ns

= 67.5 ns (@ 20 MHz)

= 80 ns + 4 ns + 3.5 ns − 21 ns − 10 ns

= 56.5 ns (@25 MHz)

A. Design #2 Light Load Timing Calculation (No Transceivers):

1. 16 MHz t_{CP} = 62.5 ns with light load

a. Address pipelined burst mode access with 0 wait state.

t_{CAC} = 2 t_{CP} − PAL20R4D t_p max. − 74F32 t_p max. − #21 (Data Setup) − ½ t_{CP}

= 125 ns − 10 ns − 6 ns − 11 ns − 31 ns

= 67 ns (DP8422A-20 and DP8422A-25 Part)

t_{AA} = 3 t_{CP} − $26 (Address to Q Valid) − #6 (Address Valid) − #21 (Data Setup)
= 187.5 ns − 26 ns − 36 ns − 11 ns
= 114.5 ns (DP8422A-25 Part)
= 187.5 ns − 29 ns − 36 ns − 11 ns
= 111.5 ns (DP8422A-20 Part)

t_{OEA} = 2 t_{CP} − PAL16R4D CLK Out t_p max. − #21 (Data Setup)
= 125 ns − 8 ns − 11 ns
= 106 ns (DP8422A-20 and DP8422A-25 Part)

b. Address pipelined nonburst mode access with 2 wait states.

t_{RAC} = 3 t_{CP} − $307 (CLK High to /RAS Low) − #21 (Data Setup)
= 187.5 ns − 22 ns − 11 ns
= 154 ns (DP8422A-25 Part)
= 187.5 ns − 27 ns − 11 ns
= 149.5 ns (DP8422A-20 Part)

t_{CAC} = 3 t_{CP} − $308 (CLK High to /CAS Low) − #21 (Data Setup) − 74F32 t_p max.
= 187.5 ns − 72 ns − 11 ns − 6 ns
= 98.5 ns (DP8422A-25 Part)
= 187.5 ns − 81 ns − 11 ns − 6 ns
= 89.5 ns (DP8422A-20 Part)

t_{AA} = 3 t_{CP} − $316 (CLK High to Column Address Valid) − #21 (Data Setup)
= 187.5 ns − 66 ns − 11 ns
= 110.5 ns (DP8422A-25 Part)
= 187.5 ns − 78 ns − 11 ns
= 98.5 ns (DP8422A-20 Part)

t_{OEA} = 4 t_{CP} − PAL16R4D CLK out t_p max. − #21 (Data Setup)
= 250 ns − 8 ns − 11 ns
= 231 ns (DP8422A-20 and DP8422A-25 Part)

c. Initial Access with 3 Wait States.

t_{RAC} = 3 t_{CP} − PAL20R4D CLK t_p max. − $402 (/ADS Low to /RAS Low) − #21 (Data Setup)
= 187.5 ns − 8 ns − 25 ns − 11 ns
= 143.5 ns (DP8422A-25 Part)
= 187.5 ns − 8 ns − 30 ns − 11 ns
= 138.5 ns (DP8422A-20 Part)

t_{CAC} = 3 t_{CP} − PAL20R4D CLK t_p max. − $403 (/ADS Low to /CAS Low) − #21 (Data Setup) − 74F32 t_p Max.
= 187.5 ns − 8 ns − 75 ns − 11 ns − 6 ns
= 87.5 ns (DP8422A-25 Part)
= 187.5 ns − 8 ns − 86 ns − 11 ns − 6 ns
= 76.5 ns (DP8422A-20 Part)

t_{AA} = 3 t_{CP} − PAL20R4D CLK t_p max. − $417 (/ADS Low to Column Address Valid) − #21 (Data Setup)
= 187.5 ns − 8 ns − 69 ns − 11 ns
= 99.5 ns (DP8422A-25 Part)
= 187.5 ns − 8 ns − 83 ns − 11 ns
= 85.5 ns (DP8422A-20 Part)

t_{OEA} = 3 t_{CP} − PAL16R4D CLK Out t_p max. − #21 (Data Setup)
= 187.5 ns − 8 ns −11 ns
= 168.5 ns (DP8422A-20 and DP8422A-25 Part)

2. 20 MHz t_{CP} = 50 ns with light load

a. Address pipelined burst mode access with 0 wait state.

t_{CAC} = 2 t_{CP} − PAL20R4D t_p max. − 74F32 t_p max. − #21 (Data Setup) − ½ t_{CP}.
= 100 ns − 10 ns − 6 ns − 11 ns − 25 ns
= 48 ns (DP8422A-20 and DP8422A-25 Part)

t_{AA} = 3 t_{CP} − $26 (Address to Q Valid) − #6 (Address Valid) − #21 (Data Setup)
= 150 ns − 26 ns − 30 ns − 11 ns
= 83 ns (DP8422A-25 Part)
= 150 ns − 29 ns − 30 ns − 11 ns
= 80 ns (DP8422A-20 Part)

t_{OEA} = 2 t_{CP} − PAL16R4D CLK out t_p max − #21 (Data Setup)
= 100 ns − 8 ns − 11 ns
= 81 ns (DP8422A-20 and DP8422A-25 Part)

b. Address pipelined nonburst mode access with 2 wait states.

t_{RAC} = 3 t_{CP} − $307 (CLK High to /RAS Low) − #21 (Data Setup)
= 150 ns − 22 ns − 11 ns
= 117 ns (DP8422A-25 Part)
= 150 ns − 27 ns − 11 ns
= 112 ns (DP8422A-20 Part)

t_{CAC} = 3 t_{CP} − $308 (CLK High to /CAS Low) − #21 (Data Setup) − 74F32 t_p max.
= 150 ns − 72 ns − 11 ns − 6 ns
= 61 ns (DP8422A-25 Part)
= 150 ns − 81 ns − 11 ns − 6 ns
= 52 ns (DP8422A-20 Part)

t_{AA} = 3 t_{CP} − $316 (CLK High to Column Address Valid) − #21 (Data Setup)
= 150 ns − 66 ns − 11 ns
= 73 ns (DP8422A-25 Part)
= 150 ns − 78 ns − 11 ns
= 61 ns (DP8422A-20 Part)

t_{OEA} = 4 t_{CP} − PAL16R4D CLK out t_p max. − #21 (Data Setup)
= 200 ns − 8 ns − 11 ns
= 181 ns (DP8422A-20 and DP8422A-25 Part)

c. Initial access with 3 wait states.

t_{RAC} = 3 t_{CP} − PAL20R4D CLK t_p max. − $402 (/ADS Low to /RAS Low) − #21 (Data Setup)
= 150 ns − 8 ns − 25 ns − 11 ns
= 106 ns (DP8422A-25 Part)
= 150 ns − 8 ns − 30 ns − 11 ns
= 101 ns (DP8422A-20 Part)

t_{CAC} = 3 t_{CP} − PAL20R4D CLK t_p max. − $403 (/ADS Low to /CAS Low) − #21 (Data Setup) − 74F32 t_p max.
= 150 ns − 8 ns − 75 ns − 11 ns − 6 ns
= 50 ns (DP8422A-25 Part)
= 150 ns − 8 ns − 86 ns − 11 ns − 6 ns
= 39 ns (DP8422A-20 Part)

t_{AA} = 3 t_{CP} − PAL20R4D CLK t_p max. $417 (/ADS Low to Column Address Valid) − #21 (Data Setup)
= 150 ns − 8 ns − 69 ns − 11 ns
= 62 ns (DP8422A-25 Part)
= 150 ns − 8 ns − 83 ns − 11 ns
= 48 ns (DP8422A-20 Part)

t_{OEA} = 3 t_{CP} − PAL16R4D CLK Out t_p max. − #21 (Data Setup)
= 150 ns − 8 ns − 11 ns
= 131 ns (DP8422A-20 and DP8422A-25 Part)

3. 25 MHz t_{CP} = 40 ns with light load

a. Address pipelined burst mode access with 0 wait state.

t_{CAC} = 2 t_{CP} − PAL20R4D t_p max. − 74F32 t_p max. − #21 (Data Setup) − ½ t_{CP}.
= 80 ns − 10 ns − 6 ns − 7 ns − 20 ns
= 37 ns (DP8422A-25 Part)

t_{AA} = 3 t_{CP} − $26 (Address to Q Valid) − #6 (Address Valid) − #21 (Data Setup)
= 120 ns − 26 ns − 21 ns − 7 ns
= 83 ns (DP8422A-25 Part)

t_{OEA} = 2 t_{CP} − PAL16R4D CLK Out t_p max. − #21 (Data Setup)
= 80 ns − 8 ns − 11 ns
= 65 ns (DP8422A-25 Part)

b. Address pipelined nonburst mode access with 2 wait states.

t_{RAC} = 3 t_{CP} − $307 (CLK High to /RAS Low) − #21 (Data Setup)
= 120 ns − 22 ns − 7 ns
= 91 ns (DP8422A-25 Part)

t_{CAC} = 3 t_{CP} − $308 (CLK High to /CAS Low) − #21 (Data Setup) − 74F32 t_p max.
= 120 ns − 72 ns − 7 ns − 6 ns
= 35 ns (DP8422A-25 Part)

t_{AA} = 3 t_{CP} − $316 (CLK High to Column Address Valid) − #21 (Data Setup)
= 120 ns − 66 ns − 7 ns
= 47 ns (DP8422A-25 Part)

t_{OEA} = 4 t_{CP} − PAL16R4D CLK Out t_p max. − #21 (Data Setup)
= 160 ns − 8 ns − 7 ns
= 145 ns (DP8422A-25 Part)

c. Initial access with 4 wait states.

t_{RAC} = 4 t_{CP} − PAL20R4D CLK t_p max. − $402 (/ADS Low to /RAS Low) − #21 (Data Setup)
= 160 ns − 8 ns − 25 ns − 7 ns
= 120 ns (DP8422A-25 Part)

t_{CAC} = 4 t_{CP} − PAL20R4D CLK t_p max. − $403 (/ADS Low to /CAS Low) − #21 (Data Setup) − 74F32 t_p max.
= 160 ns − 8 ns − 75 ns − 7 ns − 6 ns
= 64 ns (DP8422A-25 Part)

t_{AA} = 4 t_{CP} − PAL20R4D CLK t_p max. − $417 (/ADS Low to Column Address Valid) − #21 (Data Setup)
= 160 ns − 8 ns − 69 ns − 7 ns
= 76 ns (DP8422A-25 Part)

t_{OEA} = 4 t_{CP} − PAL16R4D CLK Out t_p max. − #21 (Data Setup)
= 160 ns − 8 ns − 7 ns
= 145 ns (DP8422A-25 Part)

B. Design #2 Heavy Load Timing Calculation:

1. 16 MHz t_{CP} = 62.5 ns with Heavy Load

a. Address pipelined burst mode access with 0 wait state.

t_{CAC} = 2 t_{CP} − PAL20R4D t_p max. − 74F32 t_p max. − #21 (Data Setup) − ½ t_{CP} Transceiver t_p max.
= 125 ns − 10 ns − 8 ns − 11 ns − 31 ns − 7 ns
= 48 ns (DP8422A-20 and DP8422A-25 Part)

t_{AA} = 3 t_{CP} − $26 (Address to Q Valid) − #6 (Address Valid) − #21 (Data Setup) − Transceiver t_p max.
= 187.5 ns − 35 ns − 36 ns − 11 ns − 7 ns
= 98.5 ns (DP8422A-25 Part)
= 187.5 ns − 38 ns − 36 ns − 11 ns − 7 ns
= 95.5 ns (DP8422A-20 Part)

t_{OEA} = 2 t_{CP} − PAL16R4D CLK Out t_p Max. − #21 (Data Setup) − Transceiver t_p max.
= 125 ns − 8 ns − 11 ns − 7 ns
= 89 ns (DP8422A-20 and DP8422A-25 Part)

b. Address pipelined nonburst mode access with 2 wait states.

t_{RAC} = 3 t_{CP} − $307 (CLK High to /RAS Low) − #21 (Data Setup) − Transceiver t_p max.
= 187.5 ns − 26 ns − 11 ns − 7 ns
= 143.5 ns (DP8422A-25 Part)
= 187.5 ns − 32 ns − 11 ns − 7 ns
= 137.5 ns (DP8422A-20 Part)

t_{CAC} = 3 t_{CP} − $308 (CLK High to /CAS Low) − #21 (Data Setup) − 74F32 t_p max. − Transceiver t_p max.
= 187.5 ns − 72 ns − 11 ns − 8 ns − 7 ns
= 89.5 ns (DP8422A-25 Part)
= 187.5 ns − 81 ns − 11 ns − 8 ns − 7 ns
= 80.5 ns (DP8422A-20 Part)

t_{AA} = 3 t_{CP} − $316 (CLK High to Column Address Valid) − #21 (Data Setup) − Transceiver t_p max.
= 187.5 ns − 75 ns − 11 ns − 7 ns
= 94.5 ns (DP8422A-25 Part)
= 187.5 ns − 87 ns − 11 ns − 7 ns
= 82.5 ns (DP8422A-20 Part)

t_{OEA} = 4 t_{CP} − PAL16R4D CLK Out t_p max. − #21 (Data Setup) − Transceiver t_p max.
= 250 ns − 8 ns − 11 ns − 7 ns
= 224 ns (DP8422A-20 and DP8422A-25 Part)

c. Initial Access with 3 Wait States.

t_{RAC} = 3 t_{CP} − PAL20R4D CLK t_p max. − $402 (/ADS Low to /RAS Low) − #21 (Data Setup) − Transceiver t_p max.
= 187.5 ns − 8 ns − 29 ns − 11 ns − 7 ns
= 132.5 ns (DP8422A-25 Part)
= 187.5 ns − 8 ns − 35 ns − 11 ns − 7 ns
= 126.5 ns (DP8422A-20 Part)

t_{CAC} = 3 t_{CP} − PAL20R4D CLK t_p max. − $403 (/ADS Low to /CAS Low) − #21 (Data Setup) − 74F32 t_p max. − Transceiver t_p max.
= 187.5 ns − 8 ns − 75 ns − 11 ns − 8 ns − 7 ns
= 78.5 ns (DP8422A-25 Part)
= 187.5 ns − 8 ns − 86 ns − 11 ns − 8 ns − 7 ns
= 67.5 ns (DP8422A-20 Part)

t_{AA} = 3 t_{CP} − PAL20R4D CLK t_p max. − $417 (/ADS Low to Column Address Valid) − #21 (Data Setup) − Transceiver t_p max.
= 187.5 ns − 8 ns − 78 ns − 11 ns − 7 ns
= 83.5 ns (DP8422A-25 Part)
= 187.5 ns − 8 ns − 92 ns − 11 ns − 7 ns
= 69.5 ns (DP8422A-20 Part)

t_{OEA} = 3 t_{CP} − PAL16R4D CLK Out t_p max. − #21 (Data Setup) − Transceiver t_p max.
= 187.5 ns − 8 ns − 11 ns − 7 ns
= 161.5 ns (DP8422A-20 and DP8422A-25 Part)

2. 20 MHz t_{CP} = 50 ns with heavy load

a. Address pipelined burst mode access with 0 wait state.

t_{CAC} = 2 t_{CP} − PAL20R4D t_p max. − 74F32 t_p max. − #21 (Data Setup) − ½ t_{CP} − Transceiver t_p max.
= 100 ns − 10 ns − 8 ns − 11 ns − 25 ns − 7 ns
= 29 ns (DP8422A-20 and DP8422A-25 Part)

t_{AA} = 3 t_{CP} − $26 (Address to Q Valid) − #6 (Address Valid) − #21 (Data Setup) − Transceiver t_p max.
= 150 ns − 35 ns − 30 ns − 11 ns − 7 ns
= 67 ns (DP8422A-25 Part)
= 150 ns − 38 ns − 30 ns − 11 ns − 7 ns
= 64 ns (DP8422A-20 Part)

t_{OEA} = 2 t_{CP} − PAL16R4D CLK Out t_p max. − #21 (Data Setup) − Transceiver t_p max.
= 100 ns − 8 ns − 11 ns − 7 ns
= 74 ns (DP8422A-20 and DP8422A-25 Part)

b. Address pipelined nonburst mode access with 2 wait states

t_{RAC} = 3 t_{CP} − $307 (CLK High to /RAS Low) − #21 (Data Setup) − Transceiver t_p max.
= 150 ns − 26 ns − 11 ns − 7 ns
= 106 ns (DP8422A-25 Part)
= 150 ns − 32 ns − 11 ns − 7 ns
= 100 ns (DP8422A-20 Part)

t_{CAC} = 3 t_{CP} − $308 (CLK High to /CAS Low) − #21 (Data Setup) − 74F32 t_p max. − Transceiver t_p max.
= 150 ns − 72 ns − 11 ns − 8 ns − 7 ns
= 52 ns (DP8422A-25 Part)
= 150 ns − 81 ns − 11 ns − 8 ns − 7 ns
= 43 ns (DP8422A-20 Part)

t_{AA} = 3 t_{CP} − $316 (CL High to Column Address Valid) − #21 (Data Setup) − Transceiver t_p max.
= 150 ns − 75 ns − 11 ns − 7 ns
= 57 ns (DP8422A-25 Part)
= 150 ns − 87 ns − 11 ns − 7 ns
= 45 ns (DP8422A-20 Part)

t_{OEA} = 4 t_{CP} − PAL16R4D CLK Out t_p max. − #21 (Data Setup) − Transceiver t_p max.
= 200 ns − 8 ns − 11 ns − 7 ns
= 174 ns (DP8422A-20 and DP8422A-25 Part)

c. Initial access with 4 wait states.

t_{RAC} = 4 t_{CP} − PAL20R4D CLK t_p max. − $402 (/ADS Low to /RAS Low) − #21 (Data Setup) − Transceiver t_p max.
= 200 ns − 8 ns − 29 ns − 11 ns − 7 ns
= 145 ns (DP8422A-25 Part)
= 200 ns − 8 ns − 35 ns − 11 ns − 7 ns
= 139 ns (DP8422A-20 Part)

t_{CAC} = 4 t_{CP} − PAL20R4D CLK t_p max. − $403 (/ADS Low to /CAS Low) − #21 (Data Setup) − 74F32 t_p max. − Transceiver t_p max.
= 200 ns − 8 ns − 75 ns − 11 ns − 8 ns − 7 ns
= 91 ns (DP8422A-25 Part)
= 200 ns − 8 ns − 86 ns − 11 ns − 8 ns − 7 ns
= 80 ns (DP8422A-20 Part)

t_{AA} = 4 t_{CP} − PAL20R4D CLK t_p max. − $417 (/ADS Low to Column Address Valid) − #21 (Data Setup) − Transceiver t_p max.
= 200 ns − 8 ns − 78 ns − 11 ns − 7 ns
= 96 ns (DP8422A-25 Part)
= 200 ns − 8 ns − 92 ns − 11 ns − 7 ns
= 82 ns (DP8422A-20 Part)

t_{OEA} = 4 t_{CP} − PAL16R4D CLK Out t_p max. − #21 (Data Setup) − Transceiver t_p max.
= 200 ns − 8 ns − 11 ns − 7 ns
= 174 ns (DP8422A-20 and DP8422A-25 Part)

PAL EQUATIONS

The Boolean entry operators are listed as:

"=" Equality
":=" Replaced by (After Clock)
"*" AND
"+" OR
"/" Complement
"N" Active Low

The brief explanation of PAL output signals

CAS(3:0)~ These combinational output signals are Column Address Strobes

ASDD~ This sequential output signal is ASD~ Delayed by one CLK2 clock.

HSAD~ This sequential output signal is HSA~ Delayed by one clock.

ADSD~ This sequential output signal is ADS~ Delayed by one clock.

BED(3:0)~ These combinational output signals are used to toggle CAS of DRAM directly during burst and nonburst access cycles.

ECAS~(3:0) These sequential output signals are used to hold CAS low during the burst access except design #2 heavy load burst write access cycles.

ADS~ This combinational output signal is Address Strobe to the DP8422A.

AREQ~ This combinational output signal is Access Request to the DP8422A.

NASEL~ This combinational output signal selects Next Address from either initial or noninitial access cycles.

NA~ This combinational output signal is Next Address to the 80386.

CSD~ This sequential output signal is Chip Select Delayed by one clock.

AREQT~ This sequential output signal is Access Request Transition that holds HSA~ (High Speed Access) one clock during CSD~ is low.

AREQD~ This sequential output signal is Access Request Delayed by one clock.

ASD~ This sequential output signal is Address Strobe Delayed by one clock.

WE~ This combinational output signal is Write Enable to the DRAM.

LATCH~ This combinational output signal is to hold external refresh request.

RFSH~ This combinational output signal is complement of LATCH~.

RFSHCK~ This combinational output signal is used to clock count up and down counter.

RFIPD1~ This sequential output signal is Refresh In Progress Delayed by one clock.

RFIPD2~ This sequential output signal is Refresh In Progress Delayed by two clocks.

RFIPD3~ This sequential output signal is Refresh in Progress Delayed by three clocks.

MOE~ This sequential output signal is Memory Output Enable to control the data output of the DRAM.

TEN~ This combinational output signal indicates that six missed refreshes are reached.

CKD This combinational output signal is normal CLK delayed by PAL.

READY~ This sequential output signal is delayed DTACK~ by one clock.

ADSHI~ This sequential output signal indicates whether the 80386 is accessing the DRAM or the DP8422A is refreshing the DRAM.

Ia. 386PALN1 (PAL20R4E) for Design #1

Inputs: CLK2, BE3~, BE2~, BE1~, BE0~, CAS~3, CAS~2, CAS~1, CAS~0, MOE~, ASD~;

Outputs:

/CAS3~ = (/ASDD~ * /CAS~3) + (ASD~ * /CAS~3) + (MOE~ * /CAS~3) + (BE3~ * /CAS~3);

/CAS2~ = (/ASDD~ * /CAS~2) + (ASD~ * /CAS~2) + MOE~ * /CAS~2) + (BE2~ * /CAS~2);

/CAS1~ = (/ASDD~ * /CAS~1) + (ASD~ * /CAS~1) + MOE~ * /CAS~1) + (BE1~ * /CAS~1);

/CAS0~ = (/ASDD~ * /CAS~0) + (ASD~ * /CAS~0) + MOE~ * /CAS~0) + (BE0~ * /CAS~0);

/ASDD~ := /ASD~;

/WE~ := MOE~;

Ib. 386PALN2 (PAL20R6E) for Design # 1

Inputs: CLK, BE3~, BE2~, BE1~, BE0~, CS~, HSA~, RFRQ~, RFIP~, DTACK~, AS~, WR~;

Outputs:

/ADS~ = (/HSAD~ * RFRQ~ * /HHA~) + (ASD~ * /RFRQ~);

/NA~ = (READY~ * /DTACK~ * RFRQ~ * RFIP~) + (READY~ * MOE~ * RFRQ~ * RFIP~) + (/READY~ * RFRQ~ * /MOE~ * /ASD~ * RFIP~);

/ECAS~N = (ASD~ * /HSAD~ * RFRQ~) + (BE3~ * BE2~ * BE1~ * BE0~ * /HSAD~ * RFRQ~) + (/MOE~ * /HSAD~ * RFRQ~) + (CSD~ * /HSAD~ * RFRQ~) + (ASD~ * /RFRQ~);

/CSD~ := /CS~;

/ASD~ := /AS~;

/MOE~ := /WR~;

/HSAD~ := /HSA~ * /CSD~;

/READY~ := /DTACK~;

/ADSD~ := /ADS~;

II a. 386PAL1 (PAL20R4D) for Design #2 Light Load

Inputs: CLK, BE3~, BE2~, BE1~, BE0~, READY~, CKD, MOE~, ASD~, CSD~, WR~, ADS~;

Outputs:

/BED3~ = (READY~ * /ECAS~3) + (/ASD~ * /ECAS~3) + (/CKD * /ECAS~3);

```
/BED2~      = (READY~ * /ECAS~2) + (/ASD~ *
              /ECAS~2) + (/CKD * /ECAS~2);
/BED1~      = (READY~ * /ECAS~1) + (/ASD~ *
              /ECAS~1) + (/CKD * /ECAS~1);
/BED0~      = (READY~ * /ECAS~0) + (/ASD~ *
              /ECAS~0) + (/CKD * /ECAS~0);
/ECAS~3     := (/BE3~ * /CSD~ * READY~)
               + (/BE3~ * /CSD~ * /ADS~);
/ECAS~2     := (/BE2~ * /CSD~ * READY~)
               + (/BE2~ * /CSD~ * /ADS~);
/ECAS~1     := (/BE1~ * /CSD~ * READY~)
               + (/BE1~ * /CSD~ * /ADS~);
/ECAS~0     := (/BE0~ * /CSD~ * READY~)
               + (/BE0~ * /CSD~ * /ADS~);
/ECASHI     := (/ECAS~3 + /ECAS~2
               + /ECAS~1 + /ECAS~0;
```

IIb. 386PAL1 (PAL20R4D) for Design #2 Heavy Load

Inputs: CLK, BE3~, BE2~, BE1~, BE0~, READY~, CKD, MOE~, ASD~, CSD~, WR~, ADS~;

Outputs:

```
/BED3~      = (READY~ * /ECAS~3) + (ASD~ *
              /ECAS~3) + (/CKD * /ECAS~3)
               + (MOE~ * ECAS~3);
/BED2~      = (READY~ * /ECAS~2) + (ASD~*
              /ECAS~2) + (/CKD * /ECAS~2)
               + (MOE~ * ECAS~2);
/BED1~      = (READY~ * /ECAS~1) + (ASD~ *
              /ECAS~1) + (/CKD * /ECAS~1)
               + (MOE~ * ECAS~1);
/BED0~      = (READY~ * /ECAS~0) + (ASD~ *
              /ECAS~0) + (/CKD * /ECAS~0)
               + (MOE~ * ECAS~0);
/ECAS~3:= (/BE3~ * /CSD~ * READY~) +
          (/BE3~ * /CSD~ * READY~ * /ASD~)
          +
          (/BE3~ * /CSD~ * READY~ * /WR~)
          +
          (/BE3~ * /CSD~ * /ADS~ * READY~)
          +
          (/BE3~ * /CSD~ * /ADS~) +
          (/BE3~ * /CSD~ * /ADS~ * /WR~);
/ECAS~2:= (/BE2~ * /CSD~ * READY~) +
          (/BE2~ * /CSD~ * READY~ * /ASD~)
          +
          (/BE2~ * /CSD~ * READY~ * /WR~)
          +
          (/BE2~ * /CSD~ * /ADS~ * READY~)
          +
          (/BE2~ * /CSD~ * /ADS~) +
          (/BE2~ * /CSD~ * /ADS~ * /WR~);
/ECAS~1:= (/BE1~ * /CSD~ * READY~) +
          (/BE1~ * /CSD~ * READY~ * /ASD~)
          +
          (/BE1~ * /CSD~ * READY~ * /WR~)
          +
          (/BE1~ * /CSD~ * /ADS~ * READY~)
          +
          (/BE1~ * /CSD~ * /ADS~) +
          (/BE1~ * /CSD~ * /ADS~ * /WR~);
/ECAS~0:= (/BE0~ * /CSD~ * READY~) +
          (/BE0~ * /CSD~ * READY~ * /ASD~)
          +
          (/BE0~ * /CSD~ * READY~ * /WR~)
          +
          (/BE0~ * /CSD~ * /ADS~ * READY~)
          +
          (/BE0~ * /CSD~ * /ADS~) +
          (/BE0~ * /CSD~ * /ADS~ * /WR~);
/ECASHI:=  /ECAS~3 + /ECAS~2 + /ECAS~1 +
           /ECAS~0;
```

IIc. 386PAL2 (PAL20R4D) for Design #2 Light and Heavy Load

Inputs: CLK, CS~, HSA~, LATCH~, RFSH~, DTACK~, AS~, RFIPD3~, MOE~, ECASHI;

Outputs:

```
/ADS~       = (/CS~ * /AS~) + (/AREQT~ *
              /LATCH~);
/AREQ~      = (/HSA~ * CSD~ * /AREQT~ * /CS~
              * AS~) + (/HSA~ * CSD~ *
              /AREQT~ * /LATCH~) + (/RFSH~ *
              /CS~ * AS~) + (/RFSH~ *
              /LATCH~);
/NASEL~     = (/CS~ * /DTACK~ * /AS~) + (/NA-
              SEL~ * CS~);
/NA~        = (NASEL~ * /HSA~ * /CSD~ *
              /AREQT~) + (/NASEL~ * /ECASHI *
              MOE~) + (/NASEL~ * /AREQD~ *
              /MOE~ * RFSH~ * RFIPD3~);
/CSD~       := /CS~;
/AREQT~     := /HSA~ * /CSD~;
/AREQD~     := /AREQ~;
/ASD~       := /AS~;
```

IId. 386PAL3 (PAL16R4D) for Design #2 Light and Heavy Load

Inputs: CLK, CK, RCO~, ML~, RAS~3, RFRQ~, RFIP~, TEN~, WR~;

Outputs:

```
/LATCH~     = /RCO + RFSH~;
/RFSHCK~    = /CK + (/LATCH~ * /RFRQ~) +
              (/LATCH * /RAS~3);
/RFSH~      = /TEN~ + LATCH~;
/RFIPD1~    := /RFIP~;
/RFIPD2~    := /RFIPD1~;
/RFIPD3~    := /RFIPD2~;
/MOE~       := /WR~;
```

IIe. 386PAL4 (PAL16R4D) for Design #2 Light and Heavy Load

Inputs: CLK2, DTACK~, CSD~, HSA~, RFSH~, CK, CNT0, CNT1, CNT2, MOE~;

Outputs:

```
/TEN~       = /CNT0 * CNT1 * /CNT2;
/CKD        = /CK;
/READY~     := (/DTACK~ * CK) + (/READY~ * /CK);
/ADSHI~     := (/CSD~ * /HSA~ * RFSH~) +
               /RFSH~;
/WE~        := /MOE~;
```

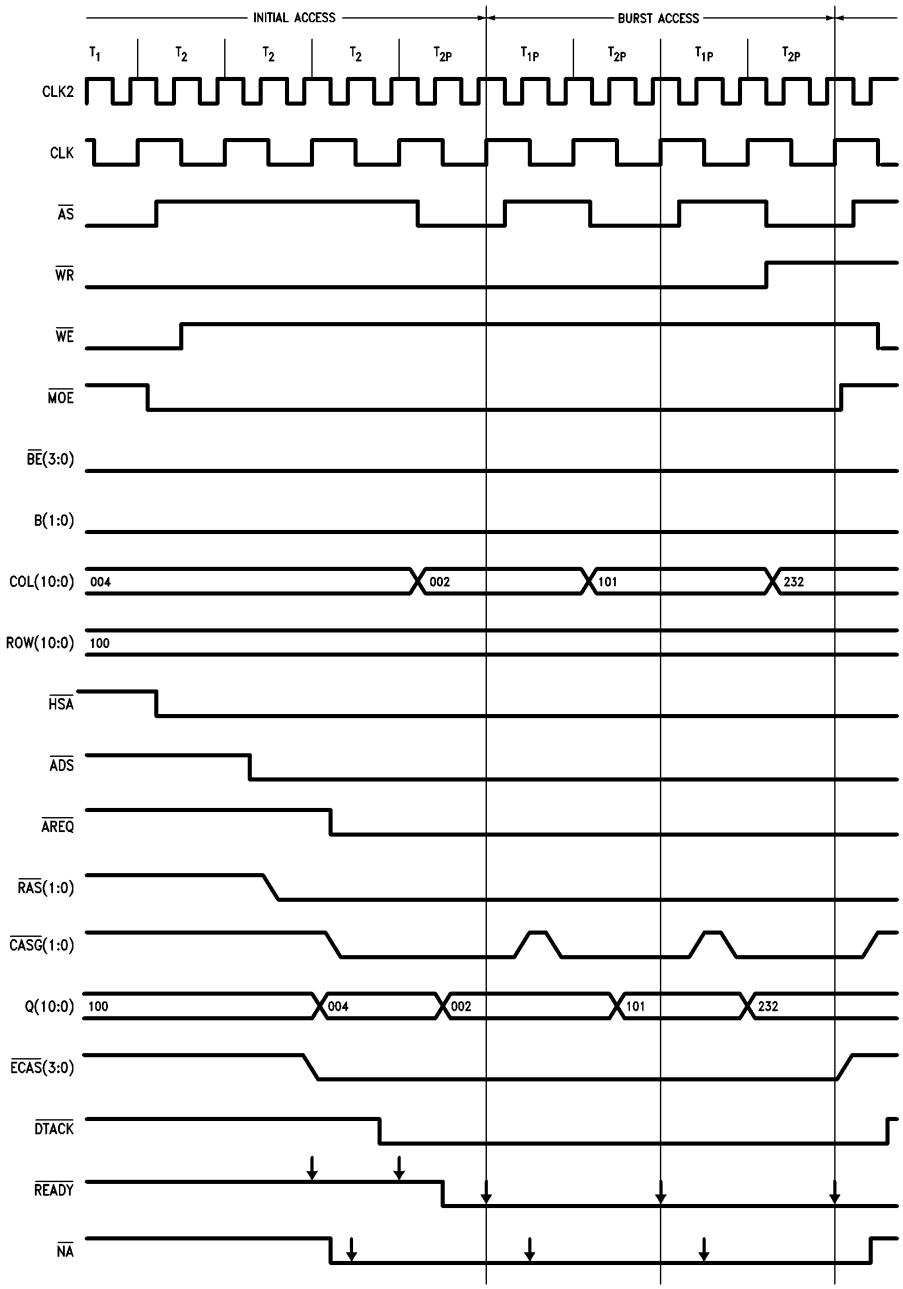

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FIGURE 6. Timing Diagram of Initial and Burst Access Cycles for Design #2

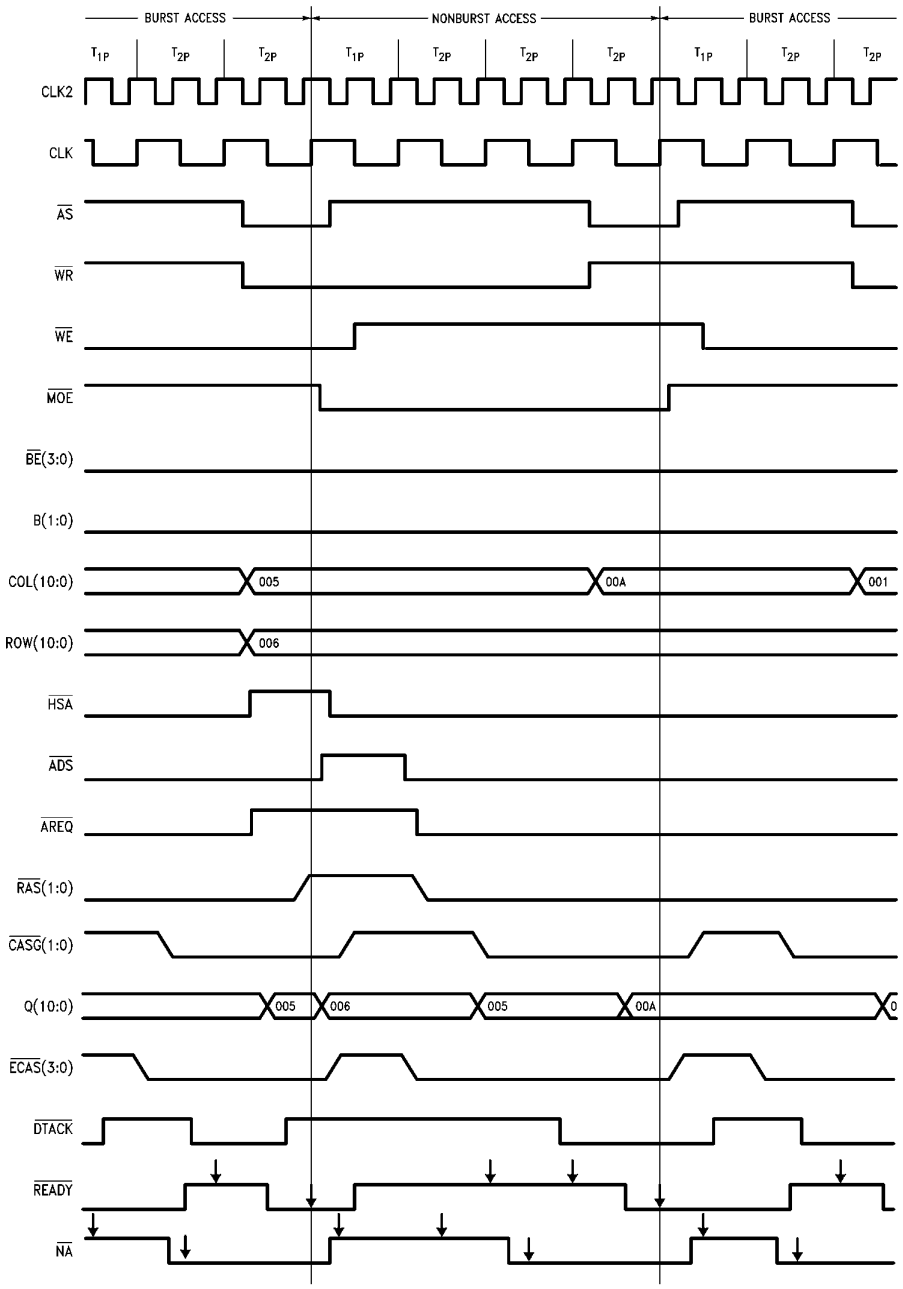

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FIGURE 7. Timing Diagram of Non-Burst and Burst Access Cycles for Design #2

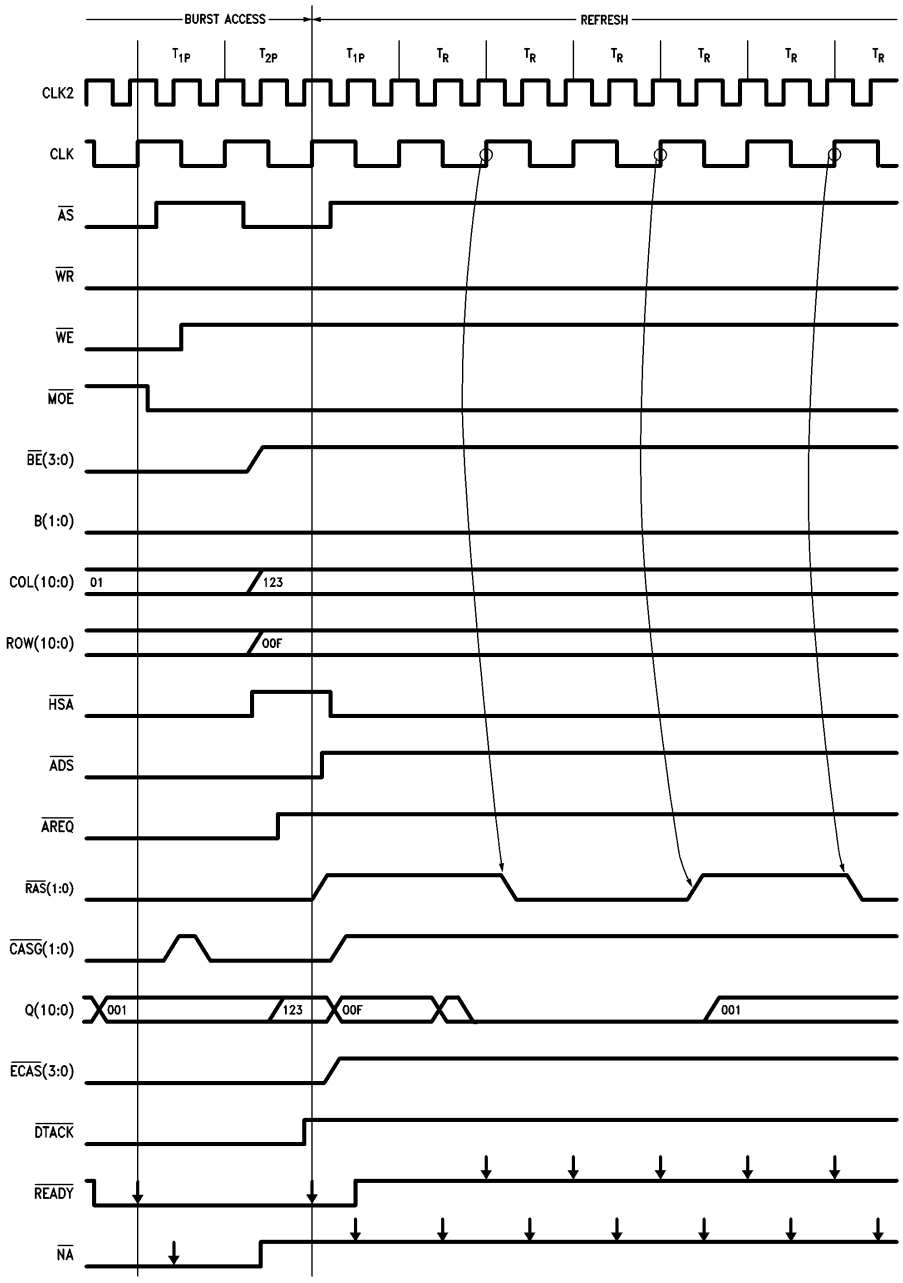

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FIGURE 8. Timing Diagram of Refresh Cycles following Burst Access Cycles for Design #2

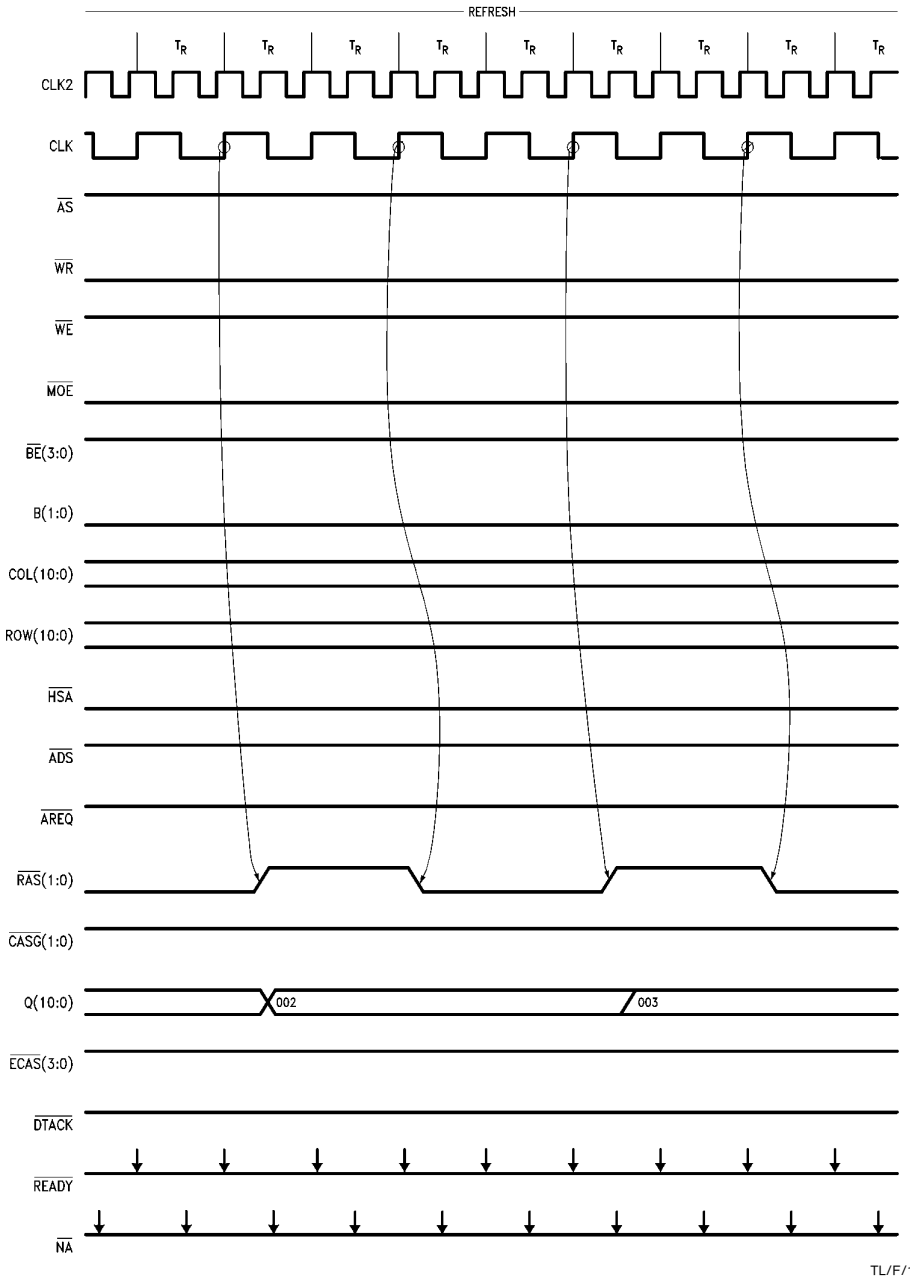

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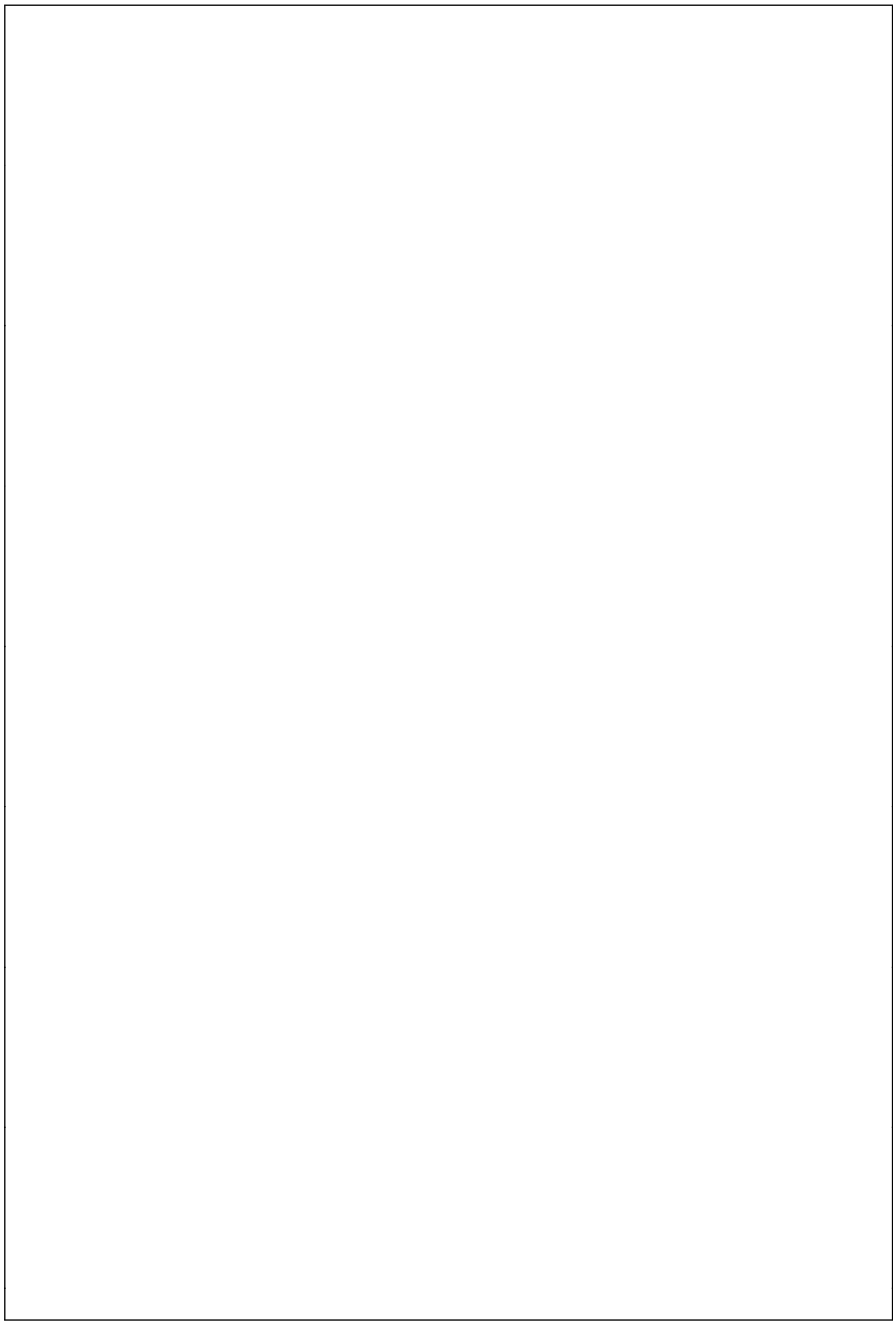
FIGURE 9. Timing Diagram of Refresh Cycles for Design # 2



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