COMBO® II Programmable PCM CODEC/Filter Family Application Guide

National Semiconductor
Application Note 614
Gary Rothrock
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1.0 INTRODUCTION

CODEC/Filter COMBO devices are designed for use in telecommunication systems such as digital Central Office switches, PABXs, PCM transmission equipment and digital telephone sets. The TP3070 series COMBO II devices are second generation combined PCM CODEC and Filter devices having a number of functions which are programmable via a serial control port. Please refer to the TP3070/TP3071 and TP3076 data sheets for a detailed description of the device functions and specifications. This application note will expand on those areas needing additional emphasis and treat a number of other areas as well.

2.0 DIFFERENCES AMONG DEVICES IN THE FAMILY

The COMBO II device family consists of three devices at the present time—TP3070, TP3071 and TP3076. It is expected that new derivative members will join the family as warranted by the marketplace. The TP3070 is the basic device type and exhibits the full feature set. This device is mounted in a 28-pin package. The TP3071 utilizes the same die and is mounted in a 20-pin package, sacrificing several features due to pin limitations. The TP3070 is suitable for almost any CODEC/Filter application where programmable features are needed. The TP3071 is recommended in applications where some of these features are not needed and can be traded off for a smaller package size.

The TP3076 devices have the hybrid balance function deleted. This device is targeted for ISDN and digital phone applications where the COMBO is in the phone and the connection is 4-wire all the way to the handset. This completely eliminates the need for the hybrid balance function and allows a reduction in the cost of the device. Another application for these devices is in 4-wire trunks, where again the hybrid balance function is not needed. The TP3076 is mounted in a 20-pin package and has a reduced feature set suitable for low cost digital phone applications.

The TP3070 has dual PCM ports which allow on-chip access to system redundant PCM bus structures. This provides increased reliability in the event one bus goes down, allowing traffic to be switched to the other bus and preventing any lines from being out of service. Redundant bussing also provides twice the traffic capacity of a single bus system. In the event of failure of one bus, only half the traffic capacity is lost. With BCLK rates of 4.096 MHz, 64 timeslots are available on each bus, for a total of 128 timeslots accessible directly by the device.

The TP3071 and TP3076 have only a single PCM port (Port 0 for the TP3071 and Port 1 for the TP3076) rather than the dual ports of the TP3070, eliminating the on-chip access to redundant PCM bus structures. At the same time, the number of accessible timeslots is also halved relative to the number available in a system with redundant PCM busses. With the single PCM port and BCLK rates of 4.096 MHz, a maximum of 64 timeslots are available.

The TP3070 has six interface latches available while the TP3071 is limited to five and the TP3076 has four. The control interface for the TP3070 and TP3076 consists of four pins; chip select ($\overline{CS}$), control clock (CCLK), control data input (CI), and control data output (CO). The TP3071 has the control input and control output pins combined into a single control input/output (CI/O) pin.

Separate bit clock (BCLK) and master clock (MCLK) pins are provided for the TP3070 and TP3076. Allowable bit clock rates are 64 kHz to 4.096 MHz, in 8 kHz increments, as long as BCLK is synchronous with MCLK. Allowable MCLK rates are 512 kHz, 1.536, 1.544, 2.048 and 4.096 MHz. The TP3071 device has a single pin which serves both BCLK and MCLK functions. Because of this, BCLK rates for the TP3071 are restricted to the MCLK rates only.

The TP3076 has no Master Reset (MR) pin for resetting the internal registers. All devices reset internal registers to a benign state when power is applied to the device pins and can also be programmed to the same conditions via the serial control interface.

The transmit gain of the TP3076 is 1.4 dB higher than the TP3070 and TP3071. With the transmit programmable gain set for 0 dB, the TP3070 and TP3071 levels at VF_XI corresponding to 0 dBm0 are $+6.4$ dBm (600Ω). For the TP3076, the 0 dBm0 levels at VF_XI are $+5.0$ dBm (600Ω).

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3.0 ABSOLUTE vs RELATIVE SIGNAL LEVELS

In the COMBO II specifications, many signal and noise levels are specified as relative levels (dBm0, dBm0p, dBrnc0) rather than absolute levels (dBm, dBmp, dBrn). When doing measurements of device performance, it is necessary to convert the absolute level readings to relative levels for comparison to specifications. The conversion factor needed will depend on the transmit gain and receive attenuation programmed into the device.

Most meters which have a dBm readout assume a 600Ω impedance, although they only measure voltage. A reading of 0.775 Vrms will be displayed as 0 dBm, no matter what the actual circuit impedance or power level. PCM levels are specified relative to the overload level (CODEC full scale). The 0 dBm0 test tone level is defined to be 3.17 dB below the overload level for μ-Law systems and 3.14 dB below the overload level for A-Law systems.

For the TP3070 and TP3071, with the transmit gain programmed to 0 dB (11111111), the overload level at VF_XI is 2.33 Vrms for μ-Law and 2.32 Vrms for A-Law. With the receive attenuation programmed for 0 dB (11111111), the overload level at VF_RO is 2.83 Vrms for μ-Law and 2.82 Vrms for A-Law. The 0 dBm0 test tone level will be 3.17 or 3.14 dB below the overload levels, or 1.619 Vrms (transmit) and 1.964 Vrms (receive). A meter calibrated in 600Ω will read these levels as +6.4 dBm (transmit) and +8.1 dBm (receive). To convert to relative dBm0, dBm0p, or dBrnc0 levels, 6.4 dB must be subtracted from the meter reading for transmit levels, and 8.1 dB must be subtracted for receive levels. At any other programmed transmit gain or receive attenuation, the conversion factors will be different. In general, the transmit conversion factor to be subtracted from the meter reading is:

+6.4 dB − programmed gain (dB)

The receive conversion factor to be subtracted is:

+8.1 dB − programmed attenuation (dB)

For the TP3076, the transmit conversion factor to be subtracted from meter readings is:

+5.0 dB − programmed gain (dB)

The receive conversion factor for the TP3076 is the same as that of the TP3070 and TP3071. See Appendix I. for a complete listing of binary gain codes for all 255 transmit and receive gains and corresponding 0dBm0 levels in dBm and Vrms at VF_XI and VF_RO. Note that the circuit points under discussion here are at the device VF_XI and VF_RO pins. When doing in-system tests, levels on the telephone line tip and ring conductors will probably differ because of circuit gains and/or losses between the device pins and the telephone line. Additional conversion factors will be necessary to account for these gains and losses.

4.0 TRANSMIT GAIN/RECEIVE ATTENUATION CODE BIT VALUES

The data sheet gives equations to calculate the binary codes required for given VF_XI input and VF_RO output rms voltages at 0 dBm0. Table I is convenient for converting the programmed gain value in dB to the binary code and vice versa. For dB to binary conversion, use the following algorithm:

1. To determine Bits 7 and 6, select the largest dB value in the left table which is less than or equal to the gain value to be converted.
2. Subtract the selected dB value from the gain value to be converted.
3. To determine bits 5 and 4, select the largest dB value in the center table which is less than or equal to the remainder.
4. Subtract this selected dB value from the remainder.
5. To determine bits 3, 2, 1 and 0, look up this remainder in the rightmost table.

See Note 1. in the table for binary to dB conversion.

5.0 NOISE PERFORMANCE AT HIGH TRANSMIT GAINS

In general, the use of high values of transmit gain is not recommended for the TP3070 and TP3071 devices unless system noise requirements are not stringent. The Transmit (idle channel) Noise and Transmit Signal to Total Distortion are both specified with transmit gain set to 0 dB. Although

TABLE I. Transmit Gain and Receive Attenuation Code Bit Values

Bit Number 7	Bit Number 6	Gain dB
0	0	19.2
0	1	12.8
1	0	6.4
1	1	0.0

Bit Number 5	Bit Number 4	Gain dB
0	0	4.8
0	1	3.2
1	0	1.6
1	1	0.0

Bit Number 3	Bit Number 2	Bit Number 1	Bit Number 0	Gain dB
0	0	0	0	1.5
0	0	0	1	1.4
0	0	1	0	1.3
0	0	1	1	1.2
0	1	0	0	1.1
0	1	0	1	1.0
0	1	1	0	0.9
0	1	1	1	0.8
1	0	0	0	0.7
1	0	0	1	0.6
1	0	1	0	0.5
1	0	1	1	0.4
1	1	0	0	0.3
1	1	0	1	0.2
1	1	1	0	0.1
1	1	1	1	0.0

Note 1: Add the three dB values for transmit gain or receive attenuation. Bit 7 = MSB.

Note 2: All zero code specifies no output.

the transmit amplifiers are designed for low noise, there will still be some degradation in noise performance for these parameters at high transmit gains. The degradation in S/D and idle noise for the TP3070 and TP3071 is about 2.5 dB at low signal levels and 25.4 dB gain, while the TP3076 is about 1.5 dB to 2 dB better due to the elimination of the input summing amplifier, as shown in *Figures 1* and *2*.

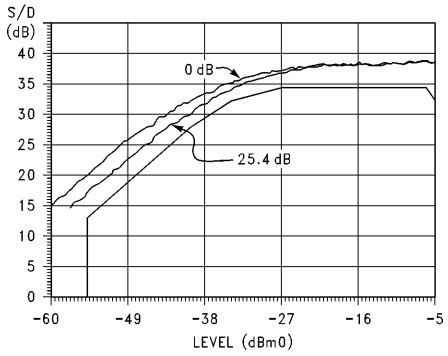

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FIGURE 1. TP3070 and TP3071 S/D at 0 dB and 25.4 dB gain (Noise Method)

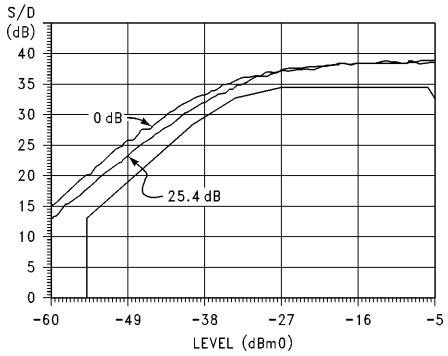

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FIGURE 2. TP3076 S/D at 0 dB and 25.4 dB gain (Noise Method)

6.0 MINIMUM RECEIVE ATTENUATION vs. OUTPUT LOADING

When programmed for 0 dB receive attenuation, the nominal receive 0 dBm0 level at VF_RO will be 1.964 Vrms. This is equivalent to a +3.17 dBm0 overload level of 2.83 Vrms for μ-Law, or 4 Vpk; slightly less for A-Law. The receive output can drive to ±4 Vpk with load impedances of ≥15 kΩ. When driving heavier loads, the output swing capability is reduced. To prevent distortion on signal peaks, some attenuation should be programmed in. For a load impedance at VF_RO of ≥600Ω, the maximum output is ±3.8 Vpk. To account for this, a minimum attenuation of at least 0.5 dB [= 20 log (3.8/4.0) rounded up to the next higher tenth of a dB] should be programmed in. For load impedances of ≥300Ω, the maximum output level is ±3.5 Vpk, and a minimum attenuation of 1.2 dB should be programmed in.

The maximum output power obtainable with 300Ω and 600Ω loads, assuming the minimum programmed attenuations, is more than sufficient for most 2-wire applications. With 0.5 dB of programmed attenuation and 600Ω load, the +3.17 dBm0 output level will be 2.67 Vrms. Maximum power delivered from the amplifier will be 11.9 mW = +10.75 dBm. With 1.2 dB of programmed attenuation and 300Ω load, the +3.17 dBm0 output level will be 2.46 Vrms. Maximum power delivered from the amplifier will be 20.2 mW = +13.06 dBm.

The 2-wire line interface is usually at 0TLP (transmission level point) or less on the receive side of a digital switch. Assuming 0TLP, the 0 dBm0 level will be 0 dBm, and the overload level will be +3.17 dBm. Allowing 1 dB for transformer loss and 3 dB for loss in the matching resistor typically used in series with the amplifier output, the maximum power the amplifier needs to supply is +7.17 dBm. With 600Ω load there will be over 3.5 dB of margin and with 300Ω load there will be about 5.9 dB of margin.

7.0 RECEIVE OUTPUT COUPLING—AC vs. DC

When driving a transformer load, AC coupling may or may not be necessary. Required capacitance values can be large because of the low impedances, transformer roll-off due to magnetizing inductance, and tight specs on frequency response and return loss at low frequencies. It is therefore desirable to use DC coupling if possible. This can be done if the DC current flow from the VF_RO output is kept low.

The output offset voltage at VF_RO is specified at ±200 mV, maximum. In a typical circuit configuration, VF_RO is connected through a matching resistor to the transformer winding, the other end of which is connected to ground. DC current will flow through the matching resistor and transformer winding as a result of this voltage offset from ground. The VF_RO output can supply 3.5V peak with a 300Ω load, or 11.6 mA peak. The sum of DC current and peak AC signal current should not exceed this to prevent distortion of the full load signal peaks.

Example: If we assume we need +3 dBm delivered to the line at + 3 dBm0, and transformer and matching resistor losses total 4 dB, the amplifier will need to supply +7 dBm = 5 mW. Assuming the reflected transformer impedance and matching resistor total 600Ω, the amplifer output voltage will be $E = \sqrt{PR}$ = 1.732 Vrms = 2.45 Vpk. Peak signal current will be I = E/R = 2.45/0.6 = 4.1 mA. DC current flow should then be less than 11.6 − 4.1 = 7.5 mA. If the matching resistor and transformer winding resistance total 300Ω, the actual DC current flow will be no more than I = 0.2V/0.3k = 0.67 mA and no capacitor is required in this case. Note that for high levels of output signal, lower values of resistance to ground, and/or lower impedance levels, a large value capacitor may be required.

The effect of the DC current flow on the transformer also needs to be considered. If an iron core transformer is being used which can handle the DC loop current, the few mA flowing due to offset will probably be of little or no consequence. Small ferrite transformers not designed to handle a DC flux should be evaluated to determine the effect on inductance and signal distortion of the expected worst case DC current flow. Even currents below 1 mA can impact performance of some ferrite transformers. If transformer performance is inadequate because of the DC flux, a capacitor will be needed.

8.0 TRANSMIT INPUT COUPLING—AC vs. DC

AC coupling to the transmit input (VF_XI) may or may not be necessary. The device has sufficient headroom to handle up to 200 mV of DC offset applied at the VF_XI input when the transmit gain is programmed for 0 dB, and up to about

10 mV when programmed for 25.4 dB gain. The product of applied input offset voltage and programmed transmit gain should not exceed 200 mV. If it does, distortion and noise performance may be degraded for high level signals near +3 dBm0.

In applications where this 200 mV product may be exceeded, capacitive coupling should be used to eliminate the DC offset. No ground reference is required at VF_XI. The minimum input resistance spec at VF_XI is 390 kΩ, and if a 0.1 μF coupling capacitor is used, the response at 300 Hz will be down only an additional 0.0008 dB.

9.0 VARIATION OF TRANSMIT INPUT RESISTANCE WITH SIGNAL LEVEL

The input resistance (R_{VFXI}) at VF_XI is specified as 390 kΩ, minimum. Typically, it is about 600 kΩ and will vary slightly with the input signal level at VF_XI. This variation in input resistance with signal level will result in low level signal distortion since the loading on the source impedance will not be constant. The magnitude of distortion will depend on the source impedance. Source impedances of 10 kΩ or less will ensure distortion products are better than 80 dB down. At typical telecom impedances of 900Ω or less, distortion products will be down more than 100 dB. Unless good distortion performance is not important in the application, source impedances much above 10 kΩ are not recommended as measurable impact on system distortion performance may result.

The absolute gain will also be impacted by loading on the source impedance. This error will be ≤0.02 dB for 1 kΩ source impedances and ≤0.22 dB for 10 kΩ source impedances.

10.0 TRANSMIT TO RECEIVE INTRACHANNEL CROSSTALK

The COMBO II CODEC/Filter is manufactured using the National high density M2CMOS process. One characteristic of this process is high digital speeds which induce large current transients in the power supply and ground lines. In particular, the D_X0 or D_X1 digital output drivers will produce significant V_{CC} and GND transients when their outputs change state, if heavy capacitive loading exists on the outputs. These transients may be under sampled by internal analog circuitry and will produce in-band noise. For most parameters there is little effect, but *for crosstalk from transmit to receive (CTXR), the effect can be quite large*. In many applications, CTXR is not important. Two wire circuits, for example, normally have no spec on crosstalk between the transmit and receive sides of the same line or trunk circuit. However, in applications such as four wire trunk circuits, transmit to receive intrachannel crosstalk performance is important, and care is required to ensure specifications will be met.

Three approaches for reducing the effects of internally generated digital noise are: reduce the magnitude of the noise at the source, i.e., the current transients; reduce the resulting V_{CC} voltage noise caused by the current transients; and reduce the sensitivity of the device to V_{CC} noise.

The D_X0 and D_X1 output buffers have the largest effect on device noise performance, and as may be expected, D_X0 and D_X1 capacitive loading also has a significant effect. For best results, National recommends that the capacitive loading on D_X0 and D_X1 be limited to about 50 pF.

Another technique which can be used in cases where heavy capacitive loading is unavoidable, is to use a small resistor (100Ω) in series with the D_X0 and D_X1 outputs. This also reduces the magnitude of the current spikes as well as provides device protection in the event of shorts on the bus. The effect of this impedance on timing will be minimal but it should be taken into account to ensure no timing specs are violated under worst case conditions.

To reduce the internally generated supply noise each COMBO II device should have a 0.1 μF capacitor connected from V_{CC} to GND as close as possible to the device pins. This is essentially the same precaution as recommended for externally generated digital noise, except the focus is on minimizing the distance from the device to the 0.1 μF bypass capacitor. Ideally it should be placed physically on the pins of the COMBO II device. The use of sockets moves the bypass capacitor physically further from the device, and therefore should be avoided. If sockets are necessary, the low profile type (i.e., Augat) may be used with minimal degradation.

As discussed above, it is critical to minimize the distance and inductance from the device to the bypass capacitor. It follows that larger packages force the capacitor further from the device in the same way that sockets do. Therefore, if CTXR is a critical parameter, it is advisable to use the TP3070V (28-Pin PLCC) or the TP3071J/76J (20-Pin DIP) devices in place of the TP3070J (28-Pin DIP).

Another important consideration for minimizing crosstalk is to provide separate signal ground return paths for the transmit and receive circuitry external to the COMBO device. The transmit line coupling transformer and any other transmit circuitry ground return should be kept separate from the receive line coupling transformer and other receive circuitry ground return all the way back to the COMBO GND pin. There should be no commonality anywhere in the ground return path for transmit and receive signals.

11.0 PRINCIPLES OF QUIET LINE CARD DESIGN

PCM CODEC/Filter COMBO devices are complex analog and digital sub-systems on a single chip. They contain, for example, an A/D and D/A converter, each with 13 bit (for μ-Law) resolution in the lowest chord, near the origin of the companded transfer characteristic. This corresponds to a dynamic range of about 78 dB. In addition, the COMBO II family of devices has programmable transmit gain and receive attenuation with a programming range of 25.4 dB, giving an overall dynamic range of about 103 dB. With the transmit side programmed for 25.4 dB gain, the 0 dBm0 level at the VF_XI input pin will be 87 mVrms. At −75 dBm0, the input signal level will be 15.5 μVrms. Needless to say, very low level noise signals may impact transmission performance.

Due to the high resolution and low noise requirements of the analog circuitry, care must be taken to minimize the effect of digital noise on analog performance. By understanding the potential problems and taking precautionary measures, the COMBO II will deliver the performance required for high quality voice transmission even in the unfriendly electrical environment of a multi-line subscriber line card. Layout of printed circuit boards and breadboards **MUST** be considered part of the design task if low noise performance is to be assured.

Logic noise is generated both externally and internally in a typical COMBO II application. The use of high speed digital circuitry on the line card produces high frequency noise on the +5V supply line which is coupled into the analog circuitry by parasitic capacitances, device non-linearities and finite power supply rejection ratios of the amplifiers. This noise is mixed with the switching frequency of the switched capacitor clocks or the encoder or decoder clocks and may produce frequency components which lie within the voice band.

11.1 General Principles for Logic Circuitry

Linecards typically involve digital as well as analog circuitry on the card and it is important to minimize logic circuit noise not only to maintain good noise margins for the logic, but also to keep the overall logic noise level on the board as low as possible for the analog circuitry. The basic points for logic portions of the board are:

1. Provide a high quality power and ground system.
2. Provide good high frequency supply decoupling on each component as well as low frequency decoupling for the board.
3. Keep signal line and component lead lengths as short as possible.
4. Route signal lines such that potential noise sources and logic signals are kept well away from analog circuits and analog power supply lines. In addition, special care may be needed for sensitive low level signal lines and high impedance points.
5. Take into consideration ground return and supply current paths.
6. Use the 74HC CMOS logic family or similar rather than TTL or LSTTL.

A good power and ground system has several beneficial effects. Since logic circuits draw relatively large transient currents during switching, ground and power lines must be low impedance to prevent appreciable voltage spikes from being developed. Because of the very high frequency components associated with the current spikes, ground and power lines must be low inductance as well as low resistance. For low inductance, power and ground traces on PC boards should be as wide as practical.

The ideal ground arrangement is a ground plane since inductance and resistance are very low and signal lines benefit from the closeness of ground as well. A ground plane will provide a lower characteristic impedance for the signal lines which helps reduce crosstalk noise from other signal lines. Noise will be injected into lines via a voltage divider formed by the capacitive coupling between lines and the line impedance. Reducing the line impedance therefore reduces the coupled noise voltage. In addition, the presence of ground has a shielding effect between lines which reduces crosstalk even further. The line characteristic impedance will be mainly a function of the dielectric constant of the board material, thickness of the board, and width of the conductor. For common $1/16$th inch epoxy fiberglass PC boards with a dielectric constant of about 5, a trace width of 20 mils (0.02 inch) will provide a characteristic impedance of 105Ω, which is reasonable for logic interconnections. The ground plane is normally on the component side of the board and all (or nearly all) interconnections between components are placed on the other side.

If a ground plane is not feasible because of high circuit density or is unavailable for other reasons, the next best approach is to simulate a ground plane by providing a rectangular grid of ground and power lines. Ground traces are run all around the digital circuit area of the board on all four sides. The ICs are then placed in rows with a ground bus running between each row. The ground busses are connected through at both ends to the ground busses on the periphery of the digital circuit area. A similar bussing arrangement is provided for the +5V supply as well, although it may not completely encircle the logic area and busses may not be connected through on both ends. Ground and +5 traces may be on either or both sides of the board. Generally, most traces are run vertically on one side of the board and horizontally on the other to avoid as many crossovers as possible. IC locations should be selected to minimize trace lengths between chips as well as between chips and connector pins. After the signal lines are run, interconnections between the ground busses should be placed wherever possible. It is often possible to add additional ground interconnections by rerouting a few traces or changing them to the other side of the board. This rectangular grid helps minimize the pathlength for the logic ground return currents. Because of the greater distance from ground, the characteristic impedance of signal lines will be higher than with a ground plane, resulting in more crosstalk due to capacitive coupling and reduced shielding effect. Noise on power and ground lines will also be higher because of higher resistance and inductance than with a ground plane. There will, however, be a great improvement over the situation where little attention is paid to power and ground arrangements and minimizing signal trace lengths.

The major functions of power supply decoupling for logic circuits are to maintain a very low supply impedance at high frequencies throughout the logic area, and to supply transient currents locally, which will reduce spikes on power and ground lines greatly. It is good practice to place a large electrolytic capacitor (at least 10 μF) and a ceramic disc capacitor (0.1 μF) from each supply to ground as close to the point where power enters the board as possible. This helps prevent external noise on the system backplane power and ground busses from entering the board. In addition, it reduces the amount of noise injected into the backplane busses from the linecard. The +5V and ground paths between these capacitors and the backplane connector should be kept very short. If the path lengths are significant, large transients may be produced in the +5V and ground lines due to capacitor in-rush currents when power is applied to the circuit. To prevent excessive inrush currents and possible burning of contacts, overly large values of electrolytic decoupling capacitor should be avoided. Both types of capacitor are necessary to provide a low impedance at both low and high frequencies. An electrolytic will provide the large capacitance needed to maintain a low impedance at lower frequencies. At frequencies above 1 MHz, most electrolytics appear inductive and a good high frequency capacitor with low Effective Series Resistance (ESR), such as a ceramic disc capacitor, is necessary to maintain a low impedance at higher frequencies.

Additional ceramic disc capacitors should be placed from +5V to ground throughout the logic circuit area, one for every IC. Ideally, the local bypass capacitor should supply all of the transient current required by the logic device it

serves. Capacitor lead lengths should be kept short to minimize inductance and capacitor placement should minimize the current path length between the capacitor and the power and ground pins of the chip it serves. Illustrated in *Figure 3* are some examples of PC layouts for logic devices, for different bussing schemes. Note that in all cases, the logic device V_{CC} and GND connections meet the bus connections at the capacitor solder pads. This ensures that transient currents flowing from the busses to the capacitor do not flow in the paths between the capacitor and device power pins, minimizing the magnitude of transient voltages applied to the device.

Short line lengths will help to reduce crosstalk between signal lines due to capacitive coupling. For digital circuits, however, the major advantage of short line lengths will be in greatly reduced distortion of signal waveforms due to reflections. Reflections occur on a signal line wherever impedance changes occur on the line. All signal conductors have some characteristic impedance which is a function of their physical dimensions and distance from ground. If the line characteristic impedance (Z_0) is equal to the load impedance, all energy will be transferred to the load and no reflection will result. The problem with logic circuits is that normally the gate input impedance is much higher than the line impedance and a gross mismatch occurs which causes reflections. If the round trip propagation delay from driving gate to receiving gate and back to the driving gate is much less than the transition time of the signal at the driver output, all reflections (and re-reflections) will occur and die out before the transition is complete and will not be noticeable on the waveform. For round trip delays approaching the order of the driver rise and fall times, some waveform distortion will be noticeable, while large overshoots and ringing will occur for longer line lengths. Propagation delays of 1.5–2 ns/foot are typical for epoxy fiberglass PC boards. The implications of this are greatest for backplane logic signals where distances are significant.

TTL and LSTTL logic families draw considerably different supply currents when their outputs are in the HIGH and LOW logic states, causing large switching currents to flow through the busses and decoupling capacitors. In contrast, CMOS logic circuits only draw significant currents during state transitions, and these currents are substantially equal. A CMOS logic system therefore generates far less electrical noise than a similar TTL system. Use of the 74HC CMOS logic family is highly recommended for line card design. It helps to preserve high quality transmission performance in the analog circuits and offers better noise margins than TTL in the presence of transient voltages induced by relays and ringing signals.

11.2 General Principles for Analog Circuitry and COMBO II Devices

Different techniques are necessary for the layout of analog circuits (COMBO II, SLIC and any external analog sections) than for digital logic circuits on the card.

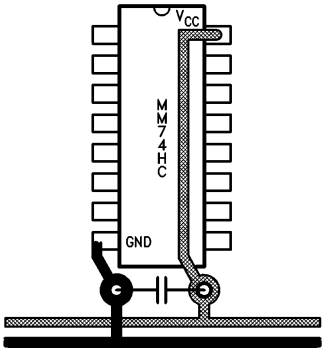
The GND pin of each COMBO II device should be used as the Ground Reference Point (GRP) for each line circuit. All analog ground connections for a single line circuit should connect directly to the reference point. This includes:

1. The analog ground from the 4-wire side of the SLIC circuit
2. The grounds for any analog networks or gain stages at the transmit VF_XI input or receive VF_RO output.
3. The ground side of the 0.1 μF decoupling capacitors for the $+5$V and -5V COMBO II power supplies.

Ground return currents from logic circuits, relays, etc., must not flow through the analog ground lines to avoid generating noise transient voltages in the ground lines. Separate analog and digital ground busses should be used on the card and should meet only at the point where $+5$V and -5V are decoupled to ground near the card connector. Likewise, separate analog and digital $+5$V busses should be run to the analog circuitry and to the logic circuits from the decoupled point near the card connector. It is NOT recommended to run separate analog and digital ground busses nor separate analog and digital $+5$V lines all the way to the system backplane. The analog $+5$V and -5V supply busses should be routed adjacent to the analog ground bus to help ensure that any noise pick-up is common mode. Relays and other circuits operating from the -48V battery supply should, however, have a separate return bus to the battery ground.

All signals and circuits capable of inducing large emf's into the analog circuitry should be located around the edge of the card whenever possible. This includes:

1. Relay drive and output signals



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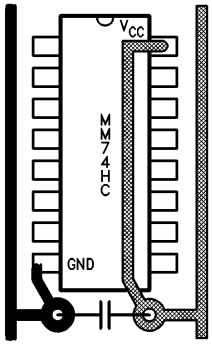

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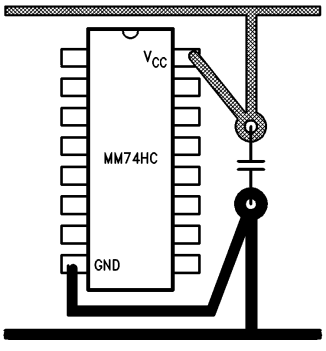

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FIGURE 3. PC Layout Examples for Logic Devices

2. Ringing distribution
3. The 2-wire side of SLIC circuitry
4. −48V battery
5. DC to DC converters.

The switching frequency of converters **MUST** be synchronized with COMBO II clocks to prevent audible beat frequencies which may otherwise fall in the passband.

To minimize external digital noise injection into the COMBO II device, it is very important to connect a 0.1 μF ceramic capacitor from V_{CC} to GND near the COMBO II device as well as at each noise source. It is critical that the length of the capacitor leads (and lead extensions via PCB traces to the device V_{CC} and GND pins) be kept as short as possible to minimize lead resistance and inductance and the resulting voltage spikes generated by transient currents flowing through these supply impedances. The V_{CC} and GND traces from the COMBO II pins and those from the supply busses should meet at the capacitor through holes or solder pads as shown in *Figure 4*. This eliminates the generation of voltage spikes in the COMBO II V_{CC} and GND connections to the capacitor due to logic transient currents flowing through a common trace length to the capacitor.

Another technique sometimes used to further decouple V_{CC} is to add a small impedance, such as an inductor or a resistor, in series with the COMBO II V_{CC} trace on the backplane side of the 0.1 μF capacitor. There are potential problems with this approach in that the COMBO II supply may increase more slowly than that of the digital circuitry. This may result in COMBO II inputs momentarily becoming more positive than the V_{CC} potential, possibly triggering latch-up. For this reason, a series impedance in the COMBO II V_{CC} line is not recommended unless Schottky diodes are used as described in the section on latch-up. A second potential problem is the reduction is supply voltage at the device power supply pins, especially under heavy loading conditions. Generally, a series resistance should not exceed 10Ω.

Normally, there is far less noise on the V_{SS} supply line allowing simple bypassing with a 0.1 μF capacitor. Decoupling V_{SS} with a series resistor or inductor is not recommended since the impedance reduces the effectiveness of the Schottky clamping diode which should be connected between V_{SS} and GND as described in the section on latch-up. If decoupling with a series element is required, the Schottky diode must be connected on the device side of the impedance, in essence requiring a diode for each COMBO II device rather than one per board.

Shown in *Figure 5* is an example of a PC layout for a portion of a line card utilizing the techniques described above.

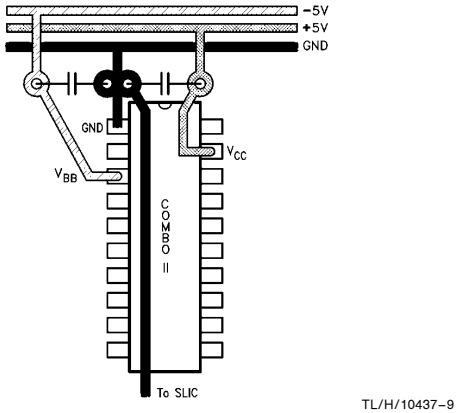

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FIGURE 4. PC Layout Example for COMBO II Devices

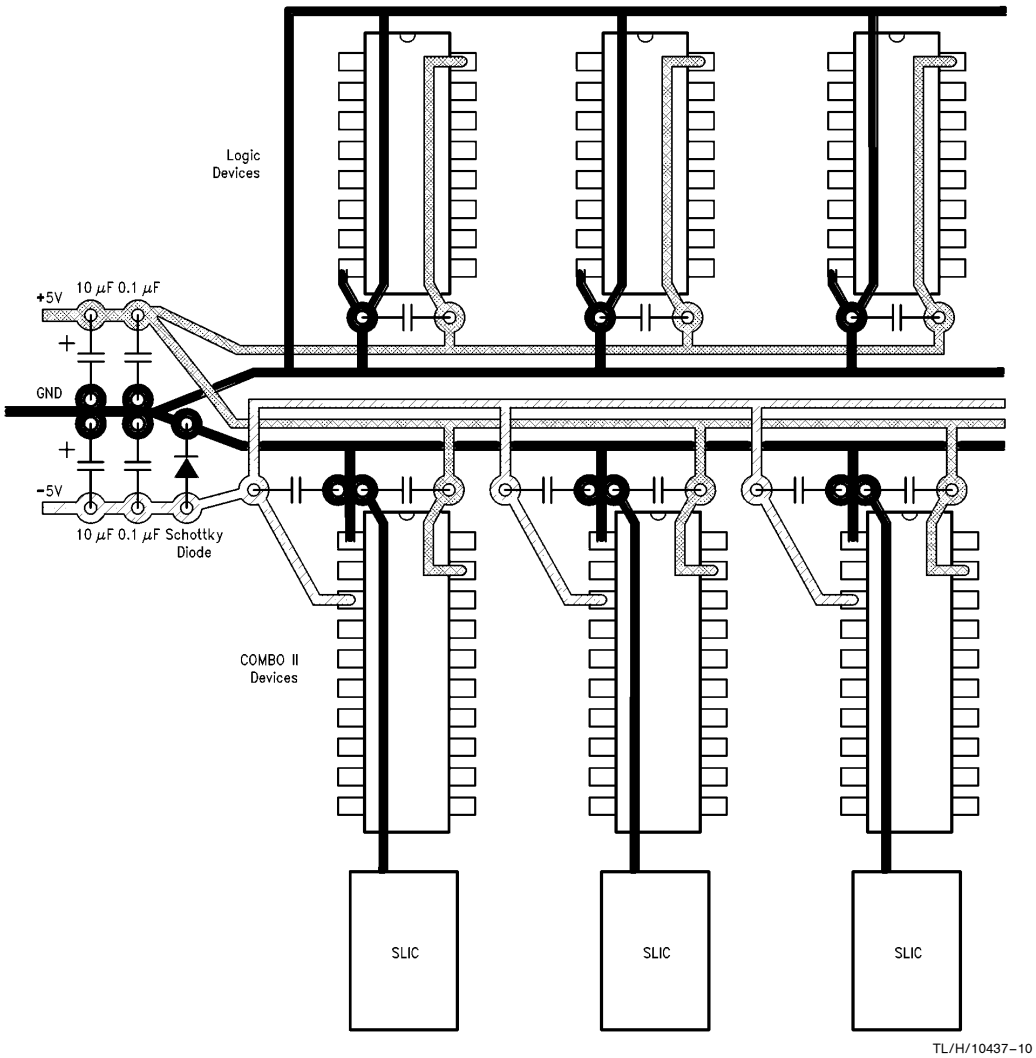

FIGURE 5. PC Board Layout Example

12.0 LATCH-UP PREVENTION TECHNIQUES

CMOS devices are subject to latch-up under certain conditions and it is important to understand what conditions can cause latch-up so the proper precautions can be taken. This is particularly important in telecommunications applications where it is necessary to insert a PC board into a system which is already powered up. Latch-up is a parasitic SCR type action which, when once triggered, causes continuous current flow through the device, usually limited only by circuit impedances and power supply capability.

With COMBO II devices, this SCR takes the form of parasitic bipolar NPN and PNP transistors. The NPN transistor base is the device substrate (also V_{BB}). The emitter is at Ground, collector at V_{CC}. If V_{BB} is allowed to go above Ground enough to turn on the base-emitter junction, the NPN will conduct current from V_{CC} to Ground. Current flow in the NPN also supplies base current to the PNP, which in turn supplies more current for the NPN. If the currents are large enough, the base currents may be sustained by internal IR drops even if V_{BB} is then connected to $-5V$, resulting in latch-up. This scenario can occur when boards are plugged into a ''hot'' system, if precautions are not taken. When connector contacts are allowed to mate in random order, logic signals, Ground and V_{CC} may be applied to the device before V_{BB} comes up. The logic signals then forward bias input protection diodes, charging the floating V_{BB} to above Ground potential, and turning on the parasitic NPN.

There are two types of protective measures:

1. Proper sequencing of logic signals and power supplies to prevent the NPN turn-on
2. Limiting the V_{BB} voltage to no more than a few tenths of a volt above Ground

The ideal sequence of power supplies and logic signals is Ground first, V_{BB}, then V_{CC}, and logic signals last. This ensures that Absolute Maximum Ratings for inputs are not exceeded, even momentarily during the power up transient, as logic signals will not exceed power supply voltages. It also ensures that the parasitic NPN is not turned on by having V_{BB} floating while Ground, V_{CC} and/or logic signals are applied. Given below are some practical methods of sequencing logic signals and power supplies and other methods of achieving protection.

Mechanically, sequencing of connections can be accomplished by using advanced connector pins or selectively shortening card edge connector contact metal. If ground, V_{BB} and V_{CC} are mechanically sequenced, these pins should be close together to minimize angle errors when inserting boards. Some sequencing can be done electrically as well. If COMBO inputs and outputs are buffered from the backplane by logic devices running from the same V_{CC} supply as the COMBO device, the logic signals cannot exceed the V_{CC} voltage. Note that if different V_{CC} supplies are used for the buffer logic and the COMBO, this protection will be lost unless the COMBO supply comes up first. Even when a single V_{CC} source is used, power supply decoupling which includes a series element in the V_{CC} line to the COMBO can cause the same effect by slowing the rise of V_{CC} voltage at the COMBO V_{CC} pin.

Buffering of all inputs and outputs from the backplane is also recommended to prevent ringing of logic signals on the buses which may exceed the supply rails from being applied to the COMBO device input and output pins. If input buffers are not used, series 1 kΩ resistors are recommended to limit current to inputs which go directly to the backplane. Note that use of series resistors will have a small impact on worst case signal timing. Even though inputs are buffered, other circuits connected between V_{CC} and V_{BB}, such as op amps, may pull V_{BB} above ground if V_{CC} precedes V_{BB}. If this other circuitry can supply enough current to trigger latch-up, a Schottky diode will be needed across V_{BB} as explained below.

If full sequencing is not practical in the application, at least the Ground pin should be advanced to ensure that Ground makes contact first. A Schottky diode should then be placed between V_{BB} and Ground such that it is forward biased if V_{BB} goes above Ground (anode connected to V_{BB}). This will limit the NPN base-emitter voltage to a few tenths of a Volt and prevent turn-on. A low cost device suitable for this application is the 1N5820. One per board should be sufficient unless series impedances are used in the V_{BB} line between the diode and the COMBO II V_{BB} pin. If series impedances are necessary to provide additional supply decoupling, or for other reasons, it is likely that one diode per COMBO II device will be necessary, as the series impedance will spoil the low voltage clamping action of the Schottky diode. In designs where series impedances are used along with one diode per COMBO II device, a smaller diode, the 1N5817, may be considered.

12.1 All Schottky Diodes Are Not Created Equal

Schottky diodes are recommended to clamp instantaneous supply reversals instead of regular silicon diodes for two reasons. First, Schottky diodes are very fast, and can effectively clamp very high speed transients. In addition, the forward voltage is generally lower than silicon junctions for similar current levels. This is very important, since the function of the Schottky diode is to prevent or limit current flow in the parasitic bipolar device base-emitter junction, which is effectively in parallel with the Schottky diode. If the Schottky forward voltage is equal to or greater than the base-emitter junction forward voltage, the protection value will be lost. For this reason, one must consider how much current the Schottky will have to conduct during the transient condition and the device specification on forward voltage at that current.

Reference to data sheets for typical devices shows a wide variation in maximum forward voltage versus device type and forward current as illustrated below.

	0.1A	1.0A	3.0A	
1N5817	0.320	0.450	0.750	V
1N5818	0.330	0.550	0.875	V
1N5819	0.340	0.600	0.900	V
1N5820		0.370	0.475	V

Notice the almost three to one spread in forward voltages among these devices over the range of currents. These voltages are for 25°C. Allowance for temperature variations should also be included. The 1N5820 provides protection for currents up to about 3A and is probably the best choice from the protection standpoint. The other devices come in a smaller package but are not suitable for large currents. The 1N5817 is recommended over the 1N5818 and 1N5819 and is usable for currents up to about 1A.

If trace lengths on the PC board between the Schottky diode and one or more COMBO devices are long and/or very high speed transients exist, there may be enough inductance in the traces to prevent adequate clamping of the high speed transients. In this case, traces can be widened to reduce inductance and another Schottky diode placed near the devices experiencing a problem.

12.2 Latch-up DOs and DON'Ts

DO — Use an advanced ground pin

— Use a 1N5820 Schottky Diode from V_{BB} to GND

— Buffer backplane logic signals with on-card logic

— Use 1 kΩ series resistors on any unbuffered digital inputs

— Use series resistors to limit VF_XI current to $<$10 mA or back to back zener diodes if input is subject to overvoltage

DON'T— Use different logic and COMBO V_{CC} supplies

— Use different op amp and COMBO supplies (unless series limiting resistor is used per above)

— Use series resistors or inductors in supply lines to COMBO

No matter which latch-up protection method is selected, the final circuit should be thoroughly tested for immunity to latch-up. Testing should include repeated insertion of a number of boards of each type into the actual live system and monitoring for latch-up. Boards should be inserted at different angles to simulate all possible connector contact sequences which can occur. Manual sequencing of signals and power supplies to the boards should also be performed to ensure all possible combinations have been tested.

13.0 ASYNCHRONOUS OPERATION

The COMBO II family of devices was not designed for asynchronous transmission applications where independent transmit and receive clocks are required. The devices have only one master clock pin (MCLK) and one bit clock pin (BCLK) which serve both transmit and receive sides of the device. With the use of a minor amount of external logic, however, operation in asynchronous systems can be achieved. Impact on transmission performance due to resynchronizing receive data will be negligible, but a high degree of care is required to minimize the level of beat frequencies produced in the output to an acceptable level. These beat frequencies are the difference between the two asynchronous clock frequencies and tend to fall below 200 Hz. If close attention is paid to power supply decoupling, grounding, and reducing receive clock noise on these as well as signal lines, these frequencies will not be audible. The COMBO device **MUST** be well isolated from the receive clock frequency and its higher order components.

The basic concept consists of buffering the receive data and retiming both the data and receive frame sync pulse using the transmit bit clock. In this way, the COMBO II device itself can continue to operate entirely in a synchronous manner. There are many ways to implement this—per bit, per sample, per frame, per line, per linecard, per system, etc. The technique and circuit described below uses a per sample and per line technique and can be used to demonstrate and/or evaluate transmission performance with asynchronous operation. Type of system, system requirements, and how partitioning and implementation of various functions have been accomplished will determine which is the optimum approach for each COMBO II application. To minimize cost and associated PC board area, the synchronization logic circuitry could be incorporated into a gate array chip which is commonly used to handle the backplane interface and other miscellaneous logic functions required on the linecard.

The per sample per line technique consists of temporarily storing each receive PCM data byte in a buffer (see *Figure 6*). The byte is clocked into the buffer using the system receive clock ($BCLK_R$). After all eight bits have been received, the system transmit clock ($BCLK_X$), also used as BCLK for COMBO II, is used to clock the byte out of the register, and into the COMBO device. At the same time, a new receive frame sync pulse (FS_R') is generated for the COMBO II device, using the system $BCLK_X$ timing. The system transmit clock ($BCLK_X$) should also be used as MCLK for the COMBO II device (i.e., BCLK and MCLK pins connected together). If BCLK is not an allowable MCLK frequency (512, 1536, 1544, 2048 or 4096 kHz), BCLK and MCLK must still be synchronous with respect to each other.

Assuming 2.048 MHz BCLK rates and that clocking of data out of the buffer begins two bit periods after the buffer is filled, the delay will be 10 BCLK periods, or about 5 μs. This delay will change as $BCLK_X$ and $BCLK_R$ drift with respect to each other, until a full BCLK period of delay change has accumulated. At this point, a jump of one $BCLK_X$ period occurs in the delay associated with the generation of the new receive frame sync pulse, as well as in clocking of data into the COMBO device. Note that no data bits have been lost, only a $BCLK_X$ period has been slipped resulting in a slight jitter of the decoded sample pulse width. The peak to peak magnitude of this jitter will be one BCLK period, or about 0.5 μs. Since the sample pulse width is 125 μs, distortion components would be down about 48 dB if this jitter occurred on every sample. Assuming 50 ppm clock accuracies, the worst case difference frequency is 200 Hz, which will also equal the number of samples per second which have jitter. With 8k samples per second occurring, distortion will be down another 32 dB because of the low density of jittered samples. Considering both aspects, the worst case distortion levels to be expected from this jitter will be 80 dB below the signal level, at least 40 dB below the level of normal quantizing distortion. If clock frequencies are better than their specified tolerance, as they typically should be, actual distortion will be even lower.

Figure 7 illustrates a circuit for implementing the block diagram for non-delayed timing mode. The circuit consists of an MM74HC164 shift register (R1) which is used as the data buffer, another MM74HC164 which counts the received data bits (R2), and some additional logic which selects the clocks to be applied to the buffer and generates the new receive frame sync pulse. FF1 senses the beginning of the cycle by clocking in a HIGH on the system receive frame sync rising edge. FF2 and FF3 control the switchover from $BCLK_R$ to $BCLK_X$ to prevent overlap of clock pulses at R1 and R2 clock inputs. FF4 provides a one bit delay to prevent missing the first data bit of the byte. The 100 kΩ resistor and 0.01 μF capacitor function as a power-up clear to ensure the register starts in the all zero state.

Figure 8 is a timing diagram for the circuit. At the end of the previous cycle, FF1 has been cleared to LOW at the Q output, which disables $BCLK_R$ at the L1 clock select logic (MM74HC58). The Q outputs of FF2 and FF3 have also

been cleared to LOW. The LOW at the Q output of FF3 disables $BCLK_X$. The cycle begins with the occurrence of a system receive frame sync pulse, signifying the arrival of another receive data byte. The rising edge of the system receive frame sync pulse (FS_R) clocks a HIGH to the Q output of FF1, since the D input is connected HIGH. This enables $BCLK_R$ at L1, which has been inverted to allow the data to be clocked into R1 in the center of the data period. R2 shifts in a logic HIGH at the A serial input with each $BCLK_R$ pulse. After eight clock pulses, the Qh output goes HIGH. This is inverted and used to clear FF1, which in turn disables further $BCLK_R$ pulses at L1. Since R2 Qh output is now HIGH, FF2 and FF3 are no longer being cleared and are allowed to shift the HIGH at FF2 D input to FF3 Q output after 2 $BCLK_X$ rising edges. $BCLK_X$ is enabled, and the receive data byte is shifted out of R1 and into COMBO II, through FF4. At the same time, since FF1 has been cleared to a LOW at the Q output, R2 now shifts the LOW level present at the A/B inputs into the register. After eight $BCLK_X$ pulses, Qh returns LOW. This again clears FF2 and FF3, and disables $BCLK_X$ at L1. The cycle is now complete. The Q output of FF3 is used as the new receive frame sync pulse (FS_R') as it is HIGH when $BCLK_X$ is enabled.

FF4 provides an additional one bit delay of the receive data to prevent the first data bit from being missed when data is clocked into COMBO II. This is needed because R1 clocks on positive edges while COMBO II clocks in data on negative edges. The MSB data bit will be available at R1 output after eight $BCLK_R$ pulses. When the register is clocked by the rising edge of the first $BCLK_X$ pulse, this data bit will be shifted to FF4. The following negative edge of $BCLK_X$ will clock this bit into the COMBO II. Without FF4, the MSB would be lost.

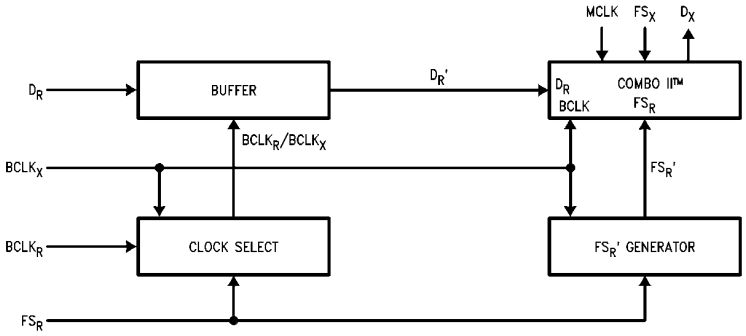

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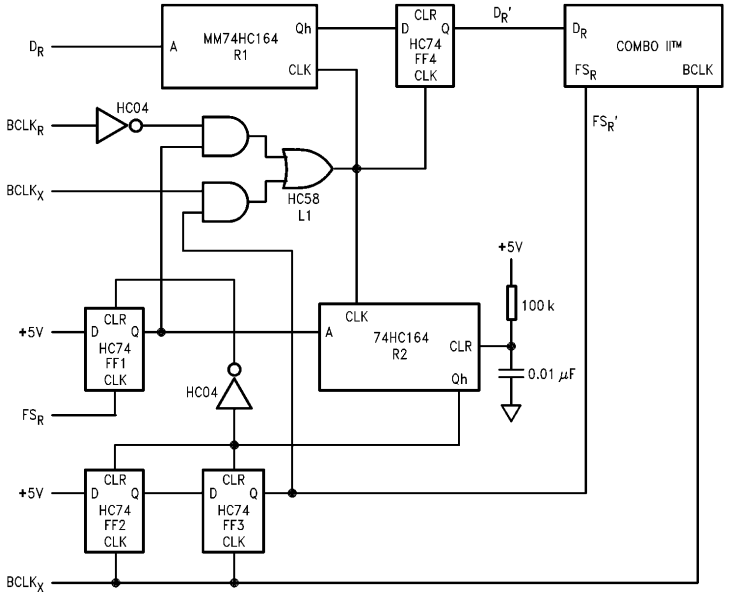
FIGURE 6. Synchronizer Block Diagram



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Note: All unused inputs tied HIGH.

FIGURE 7. Synchronizer Circuit

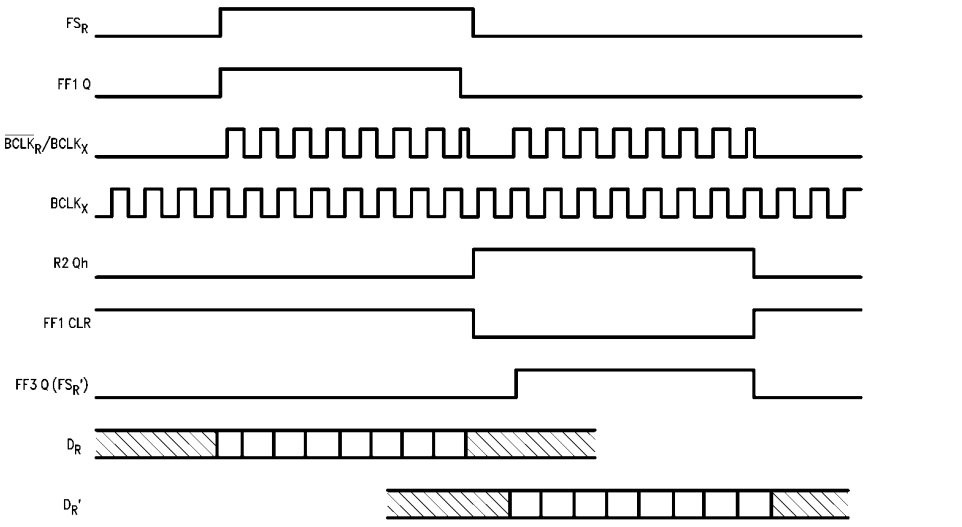

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FIGURE 8. Synchronizer Circuit Timing

14.0 REFRESHING COMBO II REGISTERS

Although it can be done, reading or writing of COMBO II registers during the talking period of a connection is not recommended because of possible noise injection into the speech path. Normally, the registers are all written prior to connection of a speech path, and on the last register write, the device is powered up. Many of the register functions never need changing after the initial setting (i.e., MCLK frequency, μ or A-Law selection, delayed or non-delayed data timing mode, power amp enabled or disabled in power down, latch direction register, and HyBal register settings). Other registers may need an initial set-up before each call. These include the interface latch register (depending on what the latches are controlling), transmit and receive gain registers, and transmit and receive timeslot/port assignment registers. If one of the interface latches is used to pick up the loop status indication from the SLIC, it may need to be read periodically during the talking period to determine when the phone has gone back ON-HOOK. In general, it is probably good design practice to refresh the contents of all registers just prior to powering up the device for the talking part of the connection. This will ensure that any register bits which somehow might have been corrupted in the past will be corrected.

During the talking period, if any repetitive reading or writing of the registers has to be done, three items are very important. First, the scanning rate should be as low as possible to prevent the generation of low level tones which may fall in the speech passband. Secondly, it is very important to use good grounding and power supply decoupling techniques, as the noise coupling path from the control interface logic and registers to the speech path is primarily through the power supply connections on the die. Good supply decoupling is necessary for isolation between the various on-chip circuits as well as isolation between various devices on the card.

Although not required functionally, the control interface signals should be synchronous with the PCM interface clocks to minimize noise.

The timeslot and port assignment registers are a special case. These registers CANNOT be written to or refreshed during the talking period because of distortion of the signals in the speech path. These registers were designed such that when the register is written, the D_X output or D_r input is immediately disabled.

On the transmit side, the D_X output is put in the TRI-STATE® condition, allowing the bus to float. On the second frame following the write to the register, D_X is re-enabled. This is done to prevent the possibility of bus clashes which might occur if switching of timeslots occurred immediately. The delay until the second frame allows the control processor time to deactivate the timeslot being switched to, if necessary. If the transmit timeslot and port assignment register is written during the talking period, an encoded signal sample will be lost each time the register is written. Depending on the interpretation of the floating bus and the amplitude of signal occurring at the lost sample instant, the resulting glitch may be from very large to negligibly small.

On the receive side, D_r is re-enabled immediately after the write is complete, so a sample will be lost only when the write occurs during the active timeslot.

Rewriting the registers can produce an audible click and if done at a high rate, a tone or buzz will result. The glitch will also result in the generation of errors on high speed modems using the channel. Note that the registers can be read without losing a signal sample, and this is recommended over repeatedly writing timeslot registers. Reading is still subject to the comments above about reading and writing the registers during the talking period.

15.0 RESERVED CONTROL INTERFACE REGISTER ADDRESSES

Four bits are used in the first byte of each control register instruction as a register address. Of the sixteen possible combinations, ten are used currently to address programming registers, seven of which are given in Table I of the data sheet. The remaining three hybrid balance register addresses are: Hybal1 = 0110 (hex 6), Hybal 2 = 0111 (hex 7), and Hybal 3 = 1000 (hex 8).

The remaining six addresses, 0011 (hex 3) and 1011 (hex B) through 1111 (hex F) are reserved for future use and should not be used in a control instruction. Attempting access using these addresses may cause improper operation of the device or render it nonfunctional until it is reset or a power down command is issued. Programming software should be written to ensure no spurious addresses are generated.

16.0 TROUBLESHOOTING GUIDE

Trouble	Potential Cause
No Tx Output at D_X	Enable bit set to zero (Tx Time slot and Port assignment register). Tx gain register set to ''off'' (all zeros). Tx Port select bit set incorrectly. For TP3071 devices, this bit must always be set to zero. For TP3076 devices, it must always be set to one. For TP3070, this bit must be set to zero or one depending on which port is being used. Device is powered down. Send any control instruction with bit 7 of byte 1 (power up/down control bit) set to logic LOW. Device has been reset. This may be caused by applying power to the device, Master Reset (MR) pin going HIGH, or large negative transient on V_{CC}. MR should be LOW for normal operation. Program all registers to desired states. Device is in Analog or Digital Loopback. Reprogram Control Register bits 1 and 2 for normal operation (00).
No Rx Output at VF_RO	Enable bit set to zero (Rx Time slot and Port assignment register). Rx gain register set to ''off'' (all zeros). Rx Port select bit set incorrectly. For TP3071 devices, this bit must always be set to zero. For TP3076 devices, it must always be set to one. For TP3070, this bit must be set to zero or one depending on which port is being used. Device is powered down. Send any control instruction with bit 7 of byte 1 (power up/down control bit) set to logic LOW. Device has been reset. This may be caused by applying power to the device, Master Reset (MR) pin going HIGH, or large negative transient on V_{CC}. MR should be LOW for normal operation. Program all registers to desired states.
High Distortion at VF_RO and D_X	Timing mode programmed incorrectly. If the system uses Non Delayed Data timing and the device is programmed for Delayed Data timing, or vice versa, Rx PCM data will be read incorrectly at the D_R input, causing high distortion of the signal at the receive output. Also, D_X output data may be misread by the system. Program bit 3 of byte 2 of the Control Register instruction for the proper mode. Rx gain register incorrectly set for load. See section entitled ''Minimum Receive Attenuation vs. Output Loading''.
Incorrect Response to Control Instructions	Byte count synchronization has been lost in the control interface logic. Three solutions exist when the current state of the byte count is unknown: 1. Remove and reapply power to the device; 2. pulse the Master Reset (MR) pin momentarily HIGH; or 3. send the single byte power up/down instruction. Devices having the CI/O pin should not use option three.
Excessive Tx to Rx Crosstalk	High capacitive loading on D_X0 and/or D_X1 output(s). Minimize capacitive loading as much as possible, at least to 50 pF or less. If heavy capacitive loading cannot be avoided, place a 100Ω resistor in series with the D_X output(s) to reduce the magnitude of current spikes. Be sure to consider the effect of the added delay on timing if a series resistor is used. Inadequate or ineffective power supply decoupling. A 0.1 μF decoupling capacitor should be placed from V_{CC} to GND as close as possible to the device pins. Do not use sockets, as this increases the distance between capacitor and device pins. If sockets are necessary, use low profile sockets. Use the smaller packages (PLCC or 20-pin DIP) rather than the 28-pin DIP.

16.0 TROUBLESHOOTING GUIDE (Continued)

Trouble	Potential Cause
Device Gets Hot	Latch-up has occurred due to violation of Absolute Maximum Ratings when signal voltages instantaneously exceed power supply voltages, or supply voltage polarity reversals have occurred. These may occur when power is applied to the system or a board is plugged into a hot system. Solutions: prevent signals from reaching the device inputs before power supply voltages (sequence connector pins: Ground first, V_{BB}, then V_{CC}, signals last), or connect a Schottky diode from V_{BB} to Ground. If V_{CC} may go negative with respect to ground, a Schottky diode may also be required from V_{CC} to Ground. Eliminate excessive ringing on logic signals so supply voltages are not exceeded. Eliminate series decoupling resistors or inductors in V_{CC} and V_{BB} lines to COMBO device as this delays supply voltages with respect to signal voltages.
Other Improper Functioning	Register contents are scrambled. Reset device by removing and reapplying power or taking the Master Reset (MR) pin momentarily HIGH. Program all ten registers to desired states. Damaged device. Replace with good device. Violation of PCM or Control Interface timing specs. Verify with oscilloscope that all timing relationships at the device pins meet data sheet spec requirements. Wiring error. Inspect ALL device pins with oscilloscope for presence of correct signals and absence of incorrect signals. Inspection should be done directly on the device pins to ensure problems due to bad solder joints or socket connections are found.

17.0 REFERENCES

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APPENDIX I. COMBO II 0 dBm0 Levels vs. Gain Codes

TP3076 TX 0 dBm0		TX Gain, dB	TP3070/1 TX 0 dBm0		Decimal Code	Binary Code	Receive 0 dBm0		RX Atten, dB
dBm (600Ω)	Vrms		dBm (600Ω)	Vrms			dBm (600Ω)	Vrms	
5.0	1.375	0.0	6.4	1.619	255	1 1 1 1 1 1 1 1	8.1	1.964	0.0
4.9	1.359	0.1	6.3	1.600	254	1 1 1 1 1 1 1 0	8.0	1.941	0.1
4.8	1.344	0.2	6.2	1.582	253	1 1 1 1 1 1 0 1	7.9	1.919	0.2
4.7	1.328	0.3	6.1	1.564	252	1 1 1 1 1 1 0 0	7.8	1.897	0.3
4.6	1.313	0.4	6.0	1.546	251	1 1 1 1 1 0 1 1	7.7	1.875	0.4
4.5	1.298	0.5	5.9	1.528	250	1 1 1 1 1 0 1 0	7.6	1.854	0.5
4.4	1.283	0.6	5.8	1.511	249	1 1 1 1 1 0 0 1	7.5	1.833	0.6
4.3	1.269	0.7	5.7	1.494	248	1 1 1 1 1 0 0 0	7.4	1.812	0.7
4.2	1.254	0.8	5.6	1.477	247	1 1 1 1 0 1 1 1	7.3	1.791	0.8
4.1	1.240	0.9	5.5	1.460	246	1 1 1 1 0 1 1 0	7.2	1.770	0.9
4.0	1.225	1.0	5.4	1.443	245	1 1 1 1 0 1 0 1	7.1	1.750	1.0
3.9	1.211	1.1	5.3	1.426	244	1 1 1 1 0 1 0 0	7.0	1.730	1.1
3.8	1.198	1.2	5.2	1.410	243	1 1 1 1 0 0 1 1	6.9	1.710	1.2
3.7	1.184	1.3	5.1	1.394	242	1 1 1 1 0 0 1 0	6.8	1.691	1.3
3.6	1.170	1.4	5.0	1.378	241	1 1 1 1 0 0 0 1	6.7	1.671	1.4
3.5	1.157	1.5	4.9	1.362	240	1 1 1 1 0 0 0 0	6.6	1.652	1.5
3.4	1.144	1.6	4.8	1.347	239	1 1 1 0 1 1 1 1	6.5	1.633	1.6
3.3	1.131	1.7	4.7	1.331	238	1 1 1 0 1 1 1 0	6.4	1.615	1.7
3.2	1.118	1.8	4.6	1.316	237	1 1 1 0 1 1 0 1	6.3	1.596	1.8
3.1	1.105	1.9	4.5	1.301	236	1 1 1 0 1 1 0 0	6.2	1.578	1.9
3.0	1.092	2.0	4.4	1.286	235	1 1 1 0 1 0 1 1	6.1	1.560	2.0
2.9	1.080	2.1	4.3	1.271	234	1 1 1 0 1 0 1 0	6.0	1.542	2.1
2.8	1.067	2.2	4.2	1.257	233	1 1 1 0 1 0 0 1	5.9	1.524	2.2
2.7	1.055	2.3	4.1	1.242	232	1 1 1 0 1 0 0 0	5.8	1.507	2.3
2.6	1.043	2.4	4.0	1.228	231	1 1 1 0 0 1 1 1	5.7	1.490	2.4
2.5	1.031	2.5	3.9	1.214	230	1 1 1 0 0 1 1 0	5.6	1.472	2.5
2.4	1.019	2.6	3.8	1.200	229	1 1 1 0 0 1 0 1	5.5	1.456	2.6
2.3	1.008	2.7	3.7	1.186	228	1 1 1 0 0 1 0 0	5.4	1.439	2.7
2.2	0.996	2.8	3.6	1.173	227	1 1 1 0 0 0 1 1	5.3	1.423	2.8
2.1	0.985	2.9	3.5	1.159	226	1 1 1 0 0 0 1 0	5.2	1.406	2.9
2.0	0.973	3.0	3.4	1.146	225	1 1 1 0 0 0 0 1	5.1	1.390	3.0
1.9	0.962	3.1	3.3	1.133	224	1 1 1 0 0 0 0 0	5.0	1.374	3.1
1.8	0.951	3.2	3.2	1.120	223	1 1 0 1 1 1 1 1	4.9	1.358	3.2
1.7	0.940	3.3	3.1	1.107	222	1 1 0 1 1 1 1 0	4.8	1.343	3.3
1.6	0.930	3.4	3.0	1.095	221	1 1 0 1 1 1 0 1	4.7	1.328	3.4
1.5	0.919	3.5	2.9	1.082	220	1 1 0 1 1 1 0 0	4.6	1.312	3.5
1.4	0.908	3.6	2.8	1.070	219	1 1 0 1 1 0 1 1	4.5	1.297	3.6
1.3	0.898	3.7	2.7	1.057	218	1 1 0 1 1 0 1 0	4.4	1.282	3.7
1.2	0.888	3.8	2.6	1.045	217	1 1 0 1 1 0 0 1	4.3	1.268	3.8
1.1	0.878	3.9	2.5	1.033	216	1 1 0 1 1 0 0 0	4.2	1.253	3.9
1.0	0.868	4.0	2.4	1.022	215	1 1 0 1 0 1 1 1	4.1	1.239	4.0
0.9	0.858	4.1	2.3	1.010	214	1 1 0 1 0 1 1 0	4.0	1.225	4.1
0.8	0.848	4.2	2.2	0.998	213	1 1 0 1 0 1 0 1	3.9	1.211	4.2
0.7	0.838	4.3	2.1	0.987	212	1 1 0 1 0 1 0 0	3.8	1.197	4.3
0.6	0.829	4.4	2.0	0.976	211	1 1 0 1 0 0 1 1	3.7	1.183	4.4
0.5	0.819	4.5	1.9	0.964	210	1 1 0 1 0 0 1 0	3.6	1.170	4.5
0.4	0.810	4.6	1.8	0.953	209	1 1 0 1 0 0 0 1	3.5	1.156	4.6
0.3	0.800	4.7	1.7	0.942	208	1 1 0 1 0 0 0 0	3.4	1.143	4.7
0.2	0.791	4.8	1.6	0.932	207	1 1 0 0 1 1 1 1	3.3	1.130	4.8
0.1	0.782	4.9	1.5	0.921	206	1 1 0 0 1 1 1 0	3.2	1.117	4.9
0.0	0.773	5.0	1.4	0.910	205	1 1 0 0 1 1 0 1	3.1	1.104	5.0
−0.1	0.764	5.1	1.3	0.900	204	1 1 0 0 1 1 0 0	3.0	1.092	5.1
−0.2	0.756	5.2	1.2	0.890	203	1 1 0 0 1 0 1 1	2.9	1.079	5.2
−0.3	0.747	5.3	1.1	0.880	202	1 1 0 0 1 0 1 0	2.8	1.067	5.3
−0.4	0.738	5.4	1.0	0.869	201	1 1 0 0 1 0 0 1	2.7	1.055	5.4

APPENDIX I. COMBO II 0 dBm0 Levels vs. Gain Codes (Continued)

TP3076 TX 0 dBm0		TX Gain, dB	TP3070/1 TX 0 dBm0		Decimal Code	Binary Code	Receive 0 dBm0		RX Atten, dB
dBm (600Ω)	Vrms		dBm (600Ω)	Vrms			dBm (600Ω)	Vrms	
−0.5	0.730	5.5	0.9	0.860	200	1 1 0 0 1 0 0 0	2.6	1.042	5.5
−0.6	0.722	5.6	0.8	0.850	199	1 1 0 0 0 1 1 1	2.5	1.031	5.6
−0.7	0.713	5.7	0.7	0.840	198	1 1 0 0 0 1 1 0	2.4	1.019	5.7
−0.8	0.705	5.8	0.6	0.830	197	1 1 0 0 0 1 0 1	2.3	1.007	5.8
−0.9	0.697	5.9	0.5	0.821	196	1 1 0 0 0 1 0 0	2.2	0.996	5.9
−1.0	0.689	6.0	0.4	0.811	195	1 1 0 0 0 0 1 1	2.1	0.984	6.0
−1.1	0.681	6.1	0.3	0.802	194	1 1 0 0 0 0 1 0	2.0	0.973	6.1
−1.2	0.673	6.2	0.2	0.793	193	1 1 0 0 0 0 0 1	1.9	0.962	6.2
−1.3	0.666	6.3	0.1	0.784	192	1 1 0 0 0 0 0 0	1.8	0.951	6.3
−1.4	0.658	6.4	0.0	0.775	191	1 0 1 1 1 1 1 1	1.7	0.940	6.4
−1.5	0.651	6.5	−0.1	0.766	190	1 0 1 1 1 1 1 0	1.6	0.929	6.5
−1.6	0.643	6.6	−0.2	0.757	189	1 0 1 1 1 1 0 1	1.5	0.918	6.6
−1.7	0.636	6.7	−0.3	0.749	188	1 0 1 1 1 1 0 0	1.4	0.908	6.7
−1.8	0.628	6.8	−0.4	0.740	187	1 0 1 1 1 0 1 1	1.3	0.898	6.8
−1.9	0.621	6.9	−0.5	0.732	186	1 0 1 1 1 0 1 0	1.2	0.887	6.9
−2.0	0.614	7.0	−0.6	0.723	185	1 0 1 1 1 0 0 1	1.1	0.877	7.0
−2.1	0.607	7.1	−0.7	0.715	184	1 0 1 1 1 0 0 0	1.0	0.867	7.1
−2.2	0.600	7.2	−0.8	0.707	183	1 0 1 1 0 1 1 1	0.9	0.857	7.2
−2.3	0.593	7.3	−0.9	0.699	182	1 0 1 1 0 1 1 0	0.8	0.847	7.3
−2.4	0.587	7.4	−1.0	0.691	181	1 0 1 1 0 1 0 1	0.7	0.838	7.4
−2.5	0.580	7.5	−1.1	0.683	180	1 0 1 1 0 1 0 0	0.6	0.828	7.5
−2.6	0.573	7.6	−1.2	0.675	179	1 0 1 1 0 0 1 1	0.5	0.819	7.6
−2.7	0.567	7.7	−1.3	0.667	178	1 0 1 1 0 0 1 0	0.4	0.809	7.7
−2.8	0.560	7.8	−1.4	0.660	177	1 0 1 1 0 0 0 1	0.3	0.800	7.8
−2.9	0.554	7.9	−1.5	0.652	176	1 0 1 1 0 0 0 0	0.2	0.791	7.9
−3.0	0.547	8.0	−1.6	0.645	175	1 0 1 0 1 1 1 1	0.1	0.782	8.0
−3.1	0.541	8.1	−1.7	0.637	174	1 0 1 0 1 1 1 0	0.0	0.773	8.1
−3.2	0.535	8.2	−1.8	0.630	173	1 0 1 0 1 1 0 1	−0.1	0.764	8.2
−3.3	0.529	8.3	−1.9	0.623	172	1 0 1 0 1 1 0 0	−0.2	0.755	8.3
−3.4	0.523	8.4	−2.0	0.616	171	1 0 1 0 1 0 1 1	−0.3	0.747	8.4
−3.5	0.517	8.5	−2.1	0.608	170	1 0 1 0 1 0 1 0	−0.4	0.738	8.5
−3.6	0.511	8.6	−2.2	0.602	169	1 0 1 0 1 0 0 1	−0.5	0.730	8.6
−3.7	0.505	8.7	−2.3	0.595	168	1 0 1 0 1 0 0 0	−0.6	0.721	8.7
−3.8	0.499	8.8	−2.4	0.588	167	1 0 1 0 0 1 1 1	−0.7	0.713	8.8
−3.9	0.494	8.9	−2.5	0.581	166	1 0 1 0 0 1 1 0	−0.8	0.705	8.9
−4.0	0.488	9.0	−2.6	0.574	165	1 0 1 0 0 1 0 1	−0.9	0.697	9.0
−4.1	0.482	9.1	−2.7	0.568	164	1 0 1 0 0 1 0 0	−1.0	0.689	9.1
−4.2	0.477	9.2	−2.8	0.561	163	1 0 1 0 0 0 1 1	−1.1	0.681	9.2
−4.3	0.471	9.3	−2.9	0.555	162	1 0 1 0 0 0 1 0	−1.2	0.673	9.3
−4.4	0.466	9.4	−3.0	0.549	161	1 0 1 0 0 0 0 1	−1.3	0.665	9.4
−4.5	0.461	9.5	−3.1	0.542	160	1 0 1 0 0 0 0 0	−1.4	0.658	9.5
−4.6	0.455	9.6	−3.2	0.536	159	1 0 0 1 1 1 1 1	−1.5	0.650	9.6
−4.7	0.450	9.7	−3.3	0.530	158	1 0 0 1 1 1 1 0	−1.6	0.643	9.7
−4.8	0.445	9.8	−3.4	0.524	157	1 0 0 1 1 1 0 1	−1.7	0.635	9.8
−4.9	0.440	9.9	−3.5	0.518	156	1 0 0 1 1 1 0 0	−1.8	0.628	9.9
−5.0	0.435	10.0	−3.6	0.512	155	1 0 0 1 1 0 1 1	−1.9	0.621	10.0
−5.1	0.430	10.1	−3.7	0.506	154	1 0 0 1 1 0 1 0	−2.0	0.614	10.1
−5.2	0.425	10.2	−3.8	0.500	153	1 0 0 1 1 0 0 1	−2.1	0.607	10.2
−5.3	0.420	10.3	−3.9	0.495	152	1 0 0 1 1 0 0 0	−2.2	0.600	10.3
−5.4	0.415	10.4	−4.0	0.489	151	1 0 0 1 0 1 1 1	−2.3	0.593	10.4
−5.5	0.410	10.5	−4.1	0.483	150	1 0 0 1 0 1 1 0	−2.4	0.586	10.5
−5.6	0.406	10.6	−4.2	0.478	149	1 0 0 1 0 1 0 1	−2.5	0.579	10.6
−5.7	0.401	10.7	−4.3	0.472	148	1 0 0 1 0 1 0 0	−2.6	0.573	10.7
−5.8	0.397	10.8	−4.4	0.467	147	1 0 0 1 0 0 1 1	−2.7	0.566	10.8
−5.9	0.392	10.9	−4.5	0.462	146	1 0 0 1 0 0 1 0	−2.8	0.560	10.9

APPENDIX I. COMBO II 0 dBm0 Levels vs. Gain Codes (Continued)

TP3076 TX 0 dBm0		TX Gain, dB	TP3070/1 TX 0 dBm0		Decimal Code	Binary Code	Receive 0 dBm0		RX Atten, dB
dBm (600Ω)	Vrms		dBm (600Ω)	Vrms			dBm (600Ω)	Vrms	
−6.0	0.388	11.0	−4.6	0.456	145	1 0 0 1 0 0 0 1	−2.9	0.553	11.0
−6.1	0.383	11.1	−4.7	0.451	144	1 0 0 1 0 0 0 0	−3.0	0.547	11.1
−6.2	0.379	11.2	−4.8	0.446	143	1 0 0 0 1 1 1 1	−3.1	0.541	11.2
−6.3	0.374	11.3	−4.9	0.441	142	1 0 0 0 1 1 1 0	−3.2	0.535	11.3
−6.4	0.370	11.4	−5.0	0.436	141	1 0 0 0 1 1 0 1	−3.3	0.529	11.4
−6.5	0.366	11.5	−5.1	0.431	140	1 0 0 0 1 1 0 0	−3.4	0.522	11.5
−6.6	0.362	11.6	−5.2	0.426	139	1 0 0 0 1 0 1 1	−3.5	0.516	11.6
−6.7	0.358	11.7	−5.3	0.421	138	1 0 0 0 1 0 1 0	−3.6	0.511	11.7
−6.8	0.353	11.8	−5.4	0.416	137	1 0 0 0 1 0 0 1	−3.7	0.505	11.8
−6.9	0.349	11.9	−5.5	0.411	136	1 0 0 0 1 0 0 0	−3.8	0.499	11.9
−7.0	0.345	12.0	−5.6	0.407	135	1 0 0 0 0 1 1 1	−3.9	0.493	12.0
−7.1	0.341	12.1	−5.7	0.402	134	1 0 0 0 0 1 1 0	−4.0	0.488	12.1
−7.2	0.338	12.2	−5.8	0.397	133	1 0 0 0 0 1 0 1	−4.1	0.482	12.2
−7.3	0.334	12.3	−5.9	0.393	132	1 0 0 0 0 1 0 0	−4.2	0.476	12.3
−7.4	0.330	12.4	−6.0	0.388	131	1 0 0 0 0 0 1 1	−4.3	0.471	12.4
−7.5	0.326	12.5	−6.1	0.384	130	1 0 0 0 0 0 1 0	−4.4	0.466	12.5
−7.6	0.322	12.6	−6.2	0.380	129	1 0 0 0 0 0 0 1	−4.5	0.460	12.6
−7.7	0.319	12.7	−6.3	0.375	128	1 0 0 0 0 0 0 0	−4.6	0.455	12.7
−7.8	0.315	12.8	−6.4	0.371	127	0 1 1 1 1 1 1 1	−4.7	0.450	12.8
−7.9	0.311	12.9	−6.5	0.367	126	0 1 1 1 1 1 1 0	−4.8	0.445	12.9
−8.0	0.308	13.0	−6.6	0.362	125	0 1 1 1 1 1 0 1	−4.9	0.440	13.0
−8.1	0.304	13.1	−6.7	0.358	124	0 1 1 1 1 1 0 0	−5.0	0.435	13.1
−8.2	0.301	13.2	−6.8	0.354	123	0 1 1 1 1 0 1 1	−5.1	0.430	13.2
−8.3	0.297	13.3	−6.9	0.350	122	0 1 1 1 1 0 1 0	−5.2	0.425	13.3
−8.4	0.294	13.4	−7.0	0.346	121	0 1 1 1 1 0 0 1	−5.3	0.420	13.4
−8.5	0.291	13.5	−7.1	0.342	120	0 1 1 1 1 0 0 0	−5.4	0.415	13.5
−8.6	0.287	13.6	−7.2	0.338	119	0 1 1 1 0 1 1 1	−5.5	0.410	13.6
−8.7	0.284	13.7	−7.3	0.334	118	0 1 1 1 0 1 1 0	−5.6	0.406	13.7
−8.8	0.281	13.8	−7.4	0.331	117	0 1 1 1 0 1 0 1	−5.7	0.401	13.8
−8.9	0.278	13.9	−7.5	0.327	116	0 1 1 1 0 1 0 0	−5.8	0.396	13.9
−9.0	0.274	14.0	−7.6	0.323	115	0 1 1 1 0 0 1 1	−5.9	0.392	14.0
−9.1	0.271	14.1	−7.7	0.319	114	0 1 1 1 0 0 1 0	−6.0	0.387	14.1
−9.2	0.268	14.2	−7.8	0.316	113	0 1 1 1 0 0 0 1	−6.1	0.383	14.2
−9.3	0.265	14.3	−7.9	0.312	112	0 1 1 1 0 0 0 0	−6.2	0.378	14.3
−9.4	0.262	14.4	−8.0	0.308	111	0 1 1 0 1 1 1 1	−6.3	0.374	14.4
−9.5	0.259	14.5	−8.1	0.305	110	0 1 1 0 1 1 1 0	−6.4	0.370	14.5
−9.6	0.256	14.6	−8.2	0.301	109	0 1 1 0 1 1 0 1	−6.5	0.366	14.6
−9.7	0.253	14.7	−8.3	0.298	108	0 1 1 0 1 1 0 0	−6.6	0.361	14.7
−9.8	0.250	14.8	−8.4	0.295	107	0 1 1 0 1 0 1 1	−6.7	0.357	14.8
−9.9	0.247	14.9	−8.5	0.291	106	0 1 1 0 1 0 1 0	−6.8	0.353	14.9
−10.0	0.245	15.0	−8.6	0.288	105	0 1 1 0 1 0 0 1	−6.9	0.349	15.0
−10.1	0.242	15.1	−8.7	0.285	104	0 1 1 0 1 0 0 0	−7.0	0.345	15.1
−10.2	0.239	15.2	−8.8	0.281	103	0 1 1 0 0 1 1 1	−7.1	0.341	15.2
−10.3	0.236	15.3	−8.9	0.278	102	0 1 1 0 0 1 1 0	−7.2	0.337	15.3
−10.4	0.234	15.4	−9.0	0.275	101	0 1 1 0 0 1 0 1	−7.3	0.333	15.4
−10.5	0.231	15.5	−9.1	0.272	100	0 1 1 0 0 1 0 0	−7.4	0.330	15.5
−10.6	0.228	15.6	−9.2	0.269	99	0 1 1 0 0 0 1 1	−7.5	0.326	15.6
−10.7	0.226	15.7	−9.3	0.266	98	0 1 1 0 0 0 1 0	−7.6	0.322	15.7
−10.8	0.223	15.8	−9.4	0.263	97	0 1 1 0 0 0 0 1	−7.7	0.318	15.8
−10.9	0.220	15.9	−9.5	0.260	96	0 1 1 0 0 0 0 0	−7.8	0.315	15.9
−11.0	0.218	16.0	−9.6	0.257	95	0 1 0 1 1 1 1 1	−7.9	0.311	16.0
−11.1	0.215	16.1	−9.7	0.254	94	0 1 0 1 1 1 1 0	−8.0	0.308	16.1
−11.2	0.213	16.2	−9.8	0.251	93	0 1 0 1 1 1 0 1	−8.1	0.304	16.2
−11.3	0.211	16.3	−9.9	0.248	92	0 1 0 1 1 1 0 0	−8.2	0.301	16.3
−11.4	0.208	16.4	−10.0	0.245	91	0 1 0 1 1 0 1 1	−8.3	0.297	16.4

APPENDIX I. COMBO II 0 dBm0 Levels vs. Gain Codes (Continued)

TP3076 TX 0 dBm0		TX Gain, dB	TP3070/1 TX 0 dBm0		Decimal Code	Binary Code	Receive 0 dBm0		RX Atten, dB
dBm (600Ω)	Vrms		dBm (600Ω)	Vrms			dBm (600Ω)	Vrms	
−11.5	0.206	16.5	−10.1	0.242	90	0 1 0 1 1 0 1 0	−8.4	0.294	16.5
−11.6	0.203	16.6	−10.2	0.239	89	0 1 0 1 1 0 0 1	−8.5	0.290	16.6
−11.7	0.201	16.7	−10.3	0.237	88	0 1 0 1 1 0 0 0	−8.6	0.287	16.7
−11.8	0.199	16.8	−10.4	0.234	87	0 1 0 1 0 1 1 1	−8.7	0.284	16.8
−11.9	0.196	16.9	−10.5	0.231	86	0 1 0 1 0 1 1 0	−8.8	0.281	16.9
−12.0	0.194	17.0	−10.6	0.229	85	0 1 0 1 0 1 0 1	−8.9	0.277	17.0
−12.1	0.192	17.1	−10.7	0.226	84	0 1 0 1 0 1 0 0	−9.0	0.274	17.1
−12.2	0.190	17.2	−10.8	0.223	83	0 1 0 1 0 0 1 1	−9.1	0.271	17.2
−12.3	0.188	17.3	−10.9	0.221	82	0 1 0 1 0 0 1 0	−9.2	0.268	17.3
−12.4	0.185	17.4	−11.0	0.218	81	0 1 0 1 0 0 0 1	−9.3	0.265	17.4
−12.5	0.183	17.5	−11.1	0.216	80	0 1 0 1 0 0 0 0	−9.4	0.262	17.5
−12.6	0.181	17.6	−11.2	0.213	79	0 1 0 0 1 1 1 1	−9.5	0.259	17.6
−12.7	0.179	17.7	−11.3	0.211	78	0 1 0 0 1 1 1 0	−9.6	0.256	17.7
−12.8	0.177	17.8	−11.4	0.209	77	0 1 0 0 1 1 0 1	−9.7	0.253	17.8
−12.9	0.175	17.9	−11.5	0.206	76	0 1 0 0 1 1 0 0	−9.8	0.250	17.9
−13.0	0.173	18.0	−11.6	0.204	75	0 1 0 0 1 0 1 1	−9.9	0.247	18.0
−13.1	0.171	18.1	−11.7	0.201	74	0 1 0 0 1 0 1 0	−10.0	0.244	18.1
−13.2	0.169	18.2	−11.8	0.199	73	0 1 0 0 1 0 0 1	−10.1	0.242	18.2
−13.3	0.167	18.3	−11.9	0.197	72	0 1 0 0 1 0 0 0	−10.2	0.239	18.3
−13.4	0.165	18.4	−12.0	0.195	71	0 1 0 0 0 1 1 1	−10.3	0.236	18.4
−13.5	0.163	18.5	−12.1	0.192	70	0 1 0 0 0 1 1 0	−10.4	0.233	18.5
−13.6	0.162	18.6	−12.2	0.190	69	0 1 0 0 0 1 0 1	−10.5	0.231	18.6
−13.7	0.160	18.7	−12.3	0.188	68	0 1 0 0 0 1 0 0	−10.6	0.228	18.7
−13.8	0.158	18.8	−12.4	0.186	67	0 1 0 0 0 0 1 1	−10.7	0.225	18.8
−13.9	0.156	18.9	−12.5	0.184	66	0 1 0 0 0 0 1 0	−10.8	0.223	18.9
−14.0	0.154	19.0	−12.6	0.182	65	0 1 0 0 0 0 0 1	−10.9	0.220	19.0
−14.1	0.153	19.1	−12.7	0.180	64	0 1 0 0 0 0 0 0	−11.0	0.218	19.1
−14.2	0.151	19.2	−12.8	0.178	63	0 0 1 1 1 1 1 1	−11.1	0.215	19.2
−14.3	0.149	19.3	−12.9	0.175	62	0 0 1 1 1 1 1 0	−11.2	0.213	19.3
−14.4	0.147	19.4	−13.0	0.173	61	0 0 1 1 1 1 0 1	−11.3	0.210	19.4
−14.5	0.146	19.5	−13.1	0.171	60	0 0 1 1 1 1 0 0	−11.4	0.208	19.5
−14.6	0.144	19.6	−13.2	0.170	59	0 0 1 1 1 0 1 1	−11.5	0.206	19.6
−14.7	0.142	19.7	−13.3	0.168	58	0 0 1 1 1 0 1 0	−11.6	0.203	19.7
−14.8	0.141	19.8	−13.4	0.166	57	0 0 1 1 1 0 0 1	−11.7	0.201	19.8
−14.9	0.139	19.9	−13.5	0.164	56	0 0 1 1 1 0 0 0	−11.8	0.199	19.9
−15.0	0.138	20.0	−13.6	0.162	55	0 0 1 1 0 1 1 1	−11.9	0.196	20.0
−15.1	0.136	20.1	−13.7	0.160	54	0 0 1 1 0 1 1 0	−12.0	0.194	20.1
−15.2	0.134	20.2	−13.8	0.158	53	0 0 1 1 0 1 0 1	−12.1	0.192	20.2
−15.3	0.133	20.3	−13.9	0.156	52	0 0 1 1 0 1 0 0	−12.2	0.190	20.3
−15.4	0.131	20.4	−14.0	0.155	51	0 0 1 1 0 0 1 1	−12.3	0.188	20.4
−15.5	0.130	20.5	−14.1	0.153	50	0 0 1 1 0 0 1 0	−12.4	0.185	20.5
−15.6	0.128	20.6	−14.2	0.151	49	0 0 1 1 0 0 0 1	−12.5	0.183	20.6
−15.7	0.127	20.7	−14.3	0.149	48	0 0 1 1 0 0 0 0	−12.6	0.181	20.7
−15.8	0.125	20.8	−14.4	0.148	47	0 0 1 0 1 1 1 1	−12.7	0.179	20.8
−15.9	0.124	20.9	−14.5	0.146	46	0 0 1 0 1 1 1 0	−12.8	0.177	20.9
−16.0	0.123	21.0	−14.6	0.144	45	0 0 1 0 1 1 0 1	−12.9	0.175	21.0
−16.1	0.121	21.1	−14.7	0.143	44	0 0 1 0 1 1 0 0	−13.0	0.173	21.1
−16.2	0.120	21.2	−14.8	0.141	43	0 0 1 0 1 0 1 1	−13.1	0.171	21.2
−16.3	0.118	21.3	−14.9	0.139	42	0 0 1 0 1 0 1 0	−13.2	0.169	21.3
−16.4	0.117	21.4	−15.0	0.138	41	0 0 1 0 1 0 0 1	−13.3	0.167	21.4
−16.5	0.116	21.5	−15.1	0.136	40	0 0 1 0 1 0 0 0	−13.4	0.165	21.5
−16.6	0.114	21.6	−15.2	0.135	39	0 0 1 0 0 1 1 1	−13.5	0.163	21.6
−16.7	0.113	21.7	−15.3	0.133	38	0 0 1 0 0 1 1 0	−13.6	0.161	21.7
−16.8	0.112	21.8	−15.4	0.132	37	0 0 1 0 0 1 0 1	−13.7	0.160	21.8
−16.9	0.110	21.9	−15.5	0.130	36	0 0 1 0 0 1 0 0	−13.8	0.158	21.9

APPENDIX I. COMBO II 0 dBm0 Levels vs. Gain Codes (Continued)

TP3076 TX 0 dBm0		TX Gain, dB	TP3070/1 TX 0 dBm0		Decimal Code	Binary Code	Receive 0 dBm0		RX Atten, dB
dBm (600Ω)	Vrms		dBm (600Ω)	Vrms			dBm (600Ω)	Vrms	
−17.0	0.109	22.0	−15.6	0.129	35	0 0 1 0 0 0 1 1	−13.9	0.156	22.0
−17.1	0.108	22.1	−15.7	0.127	34	0 0 1 0 0 0 1 0	−14.0	0.154	22.1
−17.2	0.107	22.2	−15.8	0.126	33	0 0 1 0 0 0 0 1	−14.1	0.152	22.2
−17.3	0.106	22.3	−15.9	0.124	32	0 0 1 0 0 0 0 0	−14.2	0.151	22.3
−17.4	0.104	22.4	−16.0	0.123	31	0 0 0 1 1 1 1 1	−14.3	0.149	22.4
−17.5	0.103	22.5	−16.1	0.121	30	0 0 0 1 1 1 1 0	−14.4	0.147	22.5
−17.6	0.102	22.6	−16.2	0.120	29	0 0 0 1 1 1 0 1	−14.5	0.146	22.6
−17.7	0.101	22.7	−16.3	0.119	28	0 0 0 1 1 1 0 0	−14.6	0.144	22.7
−17.8	0.100	22.8	−16.4	0.117	27	0 0 0 1 1 0 1 1	−14.7	0.142	22.8
−17.9	0.098	22.9	−16.5	0.116	26	0 0 0 1 1 0 1 0	−14.8	0.141	22.9
−18.0	0.097	23.0	−16.6	0.115	25	0 0 0 1 1 0 0 1	−14.9	0.139	23.0
−18.1	0.096	23.1	−16.7	0.113	24	0 0 0 1 1 0 0 0	−15.0	0.137	23.1
−18.2	0.095	23.2	−16.8	0.112	23	0 0 0 1 0 1 1 1	−15.1	0.136	23.2
−18.3	0.094	23.3	−16.9	0.111	22	0 0 0 1 0 1 1 0	−15.2	0.134	23.3
−18.4	0.093	23.4	−17.0	0.109	21	0 0 0 1 0 1 0 1	−15.3	0.133	23.4
−18.5	0.092	23.5	−17.1	0.108	20	0 0 0 1 0 1 0 0	−15.4	0.131	23.5
−18.6	0.091	23.6	−17.2	0.107	19	0 0 0 1 0 0 1 1	−15.5	0.130	23.6
−18.7	0.090	23.7	−17.3	0.106	18	0 0 0 1 0 0 1 0	−15.6	0.128	23.7
−18.8	0.089	23.8	−17.4	0.105	17	0 0 0 1 0 0 0 1	−15.7	0.127	23.8
−18.9	0.088	23.9	−17.5	0.103	16	0 0 0 1 0 0 0 0	−15.8	0.125	23.9
−19.0	0.087	24.0	−17.6	0.102	15	0 0 0 0 1 1 1 1	−15.9	0.124	24.0
−19.1	0.086	24.1	−17.7	0.101	14	0 0 0 0 1 1 1 0	−16.0	0.122	24.1
−19.2	0.085	24.2	−17.8	0.100	13	0 0 0 0 1 1 0 1	−16.1	0.121	24.2
−19.3	0.084	24.3	−17.9	0.099	12	0 0 0 0 1 1 0 0	−16.2	0.120	24.3
−19.4	0.083	24.4	−18.0	0.098	11	0 0 0 0 1 0 1 1	−16.3	0.118	24.4
−19.5	0.082	24.5	−18.1	0.096	10	0 0 0 0 1 0 1 0	−16.4	0.117	24.5
−19.6	0.081	24.6	−18.2	0.095	9	0 0 0 0 1 0 0 1	−16.5	0.116	24.6
−19.7	0.080	24.7	−18.3	0.094	8	0 0 0 0 1 0 0 0	−16.6	0.114	24.7
−19.8	0.079	24.8	−18.4	0.093	7	0 0 0 0 0 1 1 1	−16.7	0.113	24.8
−19.9	0.078	24.9	−18.5	0.092	6	0 0 0 0 0 1 1 0	−16.8	0.112	24.9
−20.0	0.077	25.0	−18.6	0.091	5	0 0 0 0 0 1 0 1	−16.9	0.110	25.0
−20.1	0.076	25.1	−18.7	0.090	4	0 0 0 0 0 1 0 0	−17.0	0.109	25.1
−20.2	0.076	25.2	−18.8	0.089	3	0 0 0 0 0 0 1 1	−17.1	0.108	25.2
−20.3	0.075	25.3	−18.9	0.088	2	0 0 0 0 0 0 1 0	−17.2	0.107	25.3
−20.4	0.074	25.4	−19.0	0.087	1	0 0 0 0 0 0 0 1	−17.3	0.105	25.4
OFF	OFF	OFF	OFF	OFF	0	0 0 0 0 0 0 0 0	OFF	OFF	OFF

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National Semiconductor Corporation
Americas
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018
Email: support@nsc.com
http://www.national.com

National Semiconductor Europe
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 180-530 85 85
English Tel: +49 (0) 180-532 78 32
Français Tel: +49 (0) 180-532 93 58
Italiano Tel: +49 (0) 180-534 16 80

National Semiconductor Southeast Asia
Fax: (852) 2376 3901
Email: sea.support@nsc.com

National Semiconductor Japan Ltd.
Tel: 81-3-5620-7561
Fax: 81-3-5620-6179