Interfacing the NS32CG821 to the NS32CG16

National Semiconductor
Application Note 576
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INTRODUCTION

This application note explains how to interface the NS32CG821 to the NS32CG16 microprocessor. It is assumed that the reader is familiar with the NS32CG16 access cycles and operation of the NS32CG821.

DESIGN DESCRIPTION

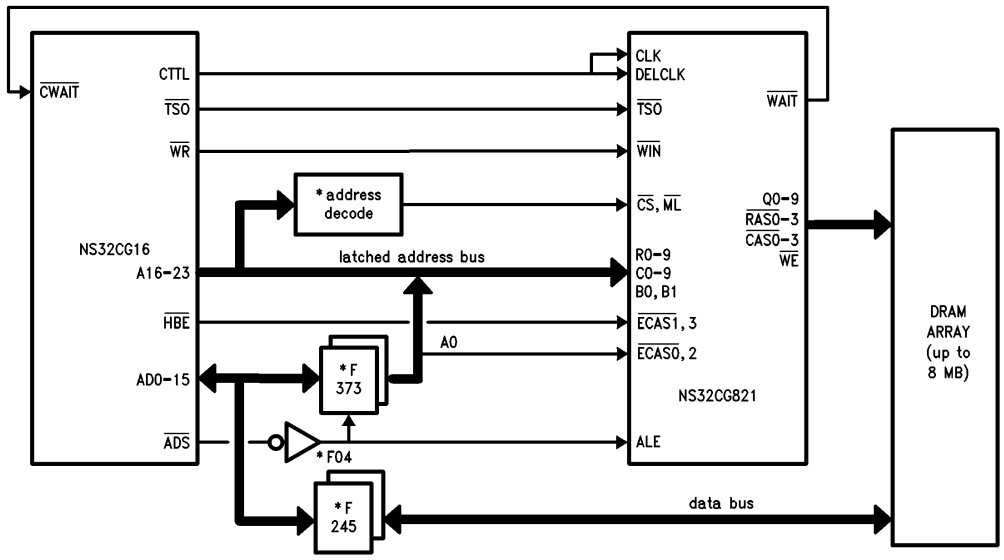
This design is a simple circuit to interface the NS32CG821 to the NS32CG16 and up to 8 Mbytes of DRAM. An access cycle begins when the NS32CG16 asserts the $\overline{ADS}$ signal and places a valid address on the bus. The $\overline{ADS}$ places a pair of 74F373 fall-through latches in fall-through mode and on the negating edge of $\overline{ADS}$ latches the address to guarantee that the address is valid throughout the entire access. The $\overline{ADS}$ signal is inverted to produce the signal ALE to the NS32CG821. On the next rising clock edge, after the ALE signal is asserted, the NS32CG821 will assert $\overline{RAS}$. After guaranteeing the row address hold time, t_{RAH}, the NS32CG821 will place the column address on the DRAM address bus, guarantee the column address setup time and assert $\overline{CAS}$. During read cycles, the DRAM will place valid data on the bus after the DRAM, t_{CAC}, timing has been met. During write cycles, $\overline{CAS}$ will be delayed until after T3re, to ensure that the CPU's write data is valid before $\overline{CAS}$ is asserted.

The N32CG821 will also take complete care of the DRAM's refresh needs. There is an internal 15 microsecond timer, and a refresh address counter. Refresh access arbitration will be controlled by an internal state machine. It will allow current cycles to complete before starting the refresh cycle. If a refresh cycle is in progress the NS32CG16 will be held off completing the access by asserting the $\overline{CWAIT}$ signal to the NS32CG16.

During programming of the chip, it is recommended that the user gate $\overline{ML}$ (Mode Load) and ($\overline{TSO}$) (Timing State Output) for the connection onto the $\overline{ML}$ pin of the NS32CG821. This is to ensure that the chip will be programmed while a valid access address is present.

Timing parameters are referenced to the numbers shown in the NS32CG821 data sheet, and are included in each equation in *italics* to indicate the target specifications that need to be satisfied. Times that begin with a "$" refer to the NS32CG821 data sheet unless otherwise stated times use "NS32CG821-20" part's parameters with heavy loading; these times are generally worse than the "NS32CG821-25" part. Times that begin with a "#" refer to the NS32CG16 data sheet. Equations are provided so that the user can calculate timing based on their frequency and application.

NS32CG16-NS32CG821 Connection Diagram



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*Standard components in any NS32CG16 design.

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DESIGN TIMING PARAMETERS

Timing diagrams are supplied further on in this document.

Clock Period = $T_{cp}10$ = 100 ns @ 10 MHz
= $T_{cp}15$ = 66 ns @ 15 MHz

$300: $\overline{CS}$ Asserted to CLK High (only A20−A23 are used for decode)

14 ns Min @ NS32CG821-20, 13 ns Min @ NS32CG821-25

= T1 − (CTTL to address valid + B-PAL delay)
= T_{cp} − #t_{AHv} − t_{Bpal}
= 100 ns − 40 ns − 15 ns

= **45 ns @ 10 MHz**

= 66 ns − 30 ns − 15 ns

= **21 ns @ 15 MHz**

$301a: ALE Setup to CLK High

16 ns Min @ NS32CG821-20,
15 ns Min @ NS32CG821-25

= T1 − Inverter Max − CTTL to $\overline{ADS}$
= T_{cp} − t_{plh} − #t_{ADSa}
= 100 ns − 5 ns − 35 ns

= **60 ns @ 10 MHz**

= 66 ns − 5 ns − 26 ns

= **35 ns @ 15 MHz**

$302: ALE Pulse Width

18 ns Min @ NS32CG821-20,
13 ns Min @ NS32CG821-25

= #t_{ADSw}

= **30 ns @ 10 MHz**
= **25 ns @ 15 MHz**

$303 & $304: Address Setup to CLK

20 ns Min @ NS32CG821-20,
18 ns Min @ NS32CG821-25

= T1 − CTTL to Address − F373 In to Out
= T_{cp} − t_{AHv} − t_{phl}
= 100 ns − 40 ns − 6 ns

= **54 ns @ 10 MHz**

= 66 ns − 30 ns − 6 ns

= **30 ns @ 15 MHz**

$310: $\overline{WIN}$ Setup to CLK High that starts the access $\overline{RAS}$ (to guarantee $\overline{CAS}$ is delayed)

−21 ns Min @ NS32CG821-20 &
−16 ns Min @ NS32CG821-25

= T1 − (time until $\overline{WR}$ active)
= T_{cp} − (T_{cp} + t_{WRa}
= 100 ns − (100 ns + 20 ns)

= **−20 ns @ 10 MHz**

= 66 ns − (66 ns + 15 ns)

= **−15 ns @ 15 MHz**

Timing parameter to guarantee $\overline{RAS}$ Precharge with 2 Clock Precharge

$29b: $\overline{TSO}$ negated Setup to CLK High with > 1 Period of Precharge

19 ns Min @ NS32CG821-20,
15 ns Min @ NS32CG821-25

= T4 − CTTL to $\overline{TSO}$ Inactive
= T_{cp} − #TSO_{ia}
= 100 ns −12 ns

= **88 ns @ 10 MHz**

= 66 ns −10 ns

= **56 ns @ 15 MHz**

$\overline{CWAIT}$: Setup for Wait States, before T3re

#tCWs, 20 ns Min @ 10 MHz
& 15 MHz for NS32CG16

= T1 + T2 − (Time in T1 until $\overline{CS}$ Asserted + $\overline{CS}$ to $\overline{WAIT}$ Asserted)
= 2T_{cp} − (#T_{AHv} + t_{Bpal} + $311)
= 200 ns − (40 ns + 15 ns + 26 ns)

= **119 ns @ 10 MHz**

= 133 ns − (30 ns + 15 ns + 22 ns)

= **66 ns @ 15 MHz**

$\overline{CWAIT}$: Hold, after T3re

#tCWh, 5 ns Min @ 10 MHz
& 15 MHz for NS32CG16

= T3re to $\overline{WAIT}$ Negated
= $17 Min

= **7 ns @ NS32CG821-20**
= **7 ns @ NS32CG821-25**

$\overline{CWAIT}$: Setup for Termination of Access

#tCWs, 20 ns Min
@ 10 MHz & 15 MHz
for NS32CG16

= T3 − CLK to $\overline{WAIT}$ Negated
= T_{cp} − $17 Max
= 100 ns − 39 ns

= **61 ns @ 10 MHz** **NS32CG821-20 Part**

= 66 ns − 39 ns

= **27 ns @ 15 MHz** **NS32CG821-20 Part**

DRAM SPECIFIC TIMING WHEN USING THE NS32CG16 @ 10 MHz

Since systems and DRAM times vary, the user is encouraged to change the following equations to match their system requirements. Timing has been supplied for systems with 0 or 1 wait states. The times assume worst case load. As such, the time will improve with lower circuit loads.

Zero Wait States Analysis for a 10 MHz NS32CG16

t_{RAC} = T2 + T3 − CLK to $\overline{RAS}$ − Transceiver Delay − Data Setup
= $2T_{cp}$ − \$307 − t_{phl} − #t_{Dls}
= 200 ns − 32 ns − 7 ns − 18 ns
= 143 ns @ 10 MHz **NS32CG821-20 Part**

t_{AA} = T2 + T3 − CLK to Column Address Valid − Transceiver Delay − Data Setup
= $2T_{cp}$ − \$316act − t_{phl} − #t_{Dls}
= 200 ns − 87 ns − 7 ns − 18 ns
= 88 ns @ 10 MHz **NS32CG821-20 Part**

t_{CAC} = T2 + T3 − CLK to $\overline{CAS}$ − Transceiver Delay − Data Setup
= $2T_{cp}$ − \$308act − t_{phl} − #t_{Dls}
= 200 ns − 89 ns − 7 ns − 18 ns
= 86 ns @ 10 MHz **NS32CG821-20 Part**

One Wait State Analysis for a 10 MHz NS32CG16

t_{RAC} = T2 + T_w + T3 − CLK to $\overline{RAS}$ − Transceiver Delay − Data Setup
= $3T_{cp}$ − \$307 − t_{phl} − #t_{Dls}
= 300 ns − 32 ns − 7 ns − 18 ns
= 243 ns @ 10 MHz **NS32CG821-20 Part**

t_{AA} = T2 + T_w + T3 − CLK to ColumnAddress Valid − Transceiver Delay − Data Setup
= $3T_{cp}$ − \$316act − t_{phl} − #t_{Dls}
= 300 ns − 87 ns − 7 ns − 18 ns
= 188 ns @ 10 MHz **NS32CG821-20 Part**

t_{CAC} = T2 + T_w + T3 − CLK to $\overline{CAS}$ − Transceiver Delay − Data Setup
= $3T_{cp}$ − \$308act − t_{phl} − #t_{Dls}
= 300 ns − 89 ns − 7 ns − 18 ns
= 186 ns @ 10 MHz **NS32CG821-20 Part**

$\overline{RAS}$ Precharge Parameter (for both zero and one wait state)

t_{RP} $\overline{RAS}$ Precharge Time
see DRAM data sheet (usually < 100 ns)
= T4 + T1 − CTTL to $\overline{TSO}$ inactive + [(CLK high to $\overline{RAS}$ asserted) − ($\overline{TSO}$ negated to $\overline{RAS}$ negated)]
= $2T_{cp}$ − #t_{TSOia} + \$53
= 200 ns − 12 ns + 4 ns
= 192 ns @ 10 MHz **for NS32CG16**

$\overline{RAS}$ Low During Refresh (for both zero and one wait state)

t_{RAS} = Programmed Clocks − [(CLK High to Refresh $\overline{RAS}$ asserted) − (CLK High to Refresh $\overline{RAS}$ negated)]
= $2T_{cp}$ − \$55
= 200 ns − 5 ns
= 195 ns @ 10 MHz **for NS32CG16**

DRAM SPECIFIC TIMING WHEN USING THE NS32CG16 @ 15 MHz

The input DELCLK controls the internal delay line and should be a multiple of 2 MHz. Since DELCLK is 15 MHz (when directly connected to CTTL) and is not a multiple of 2 MHz, t_{RAH} and t_{ASC} will vary from the programmed times according to the equations listed below.

In addition, please note the following pertaining to the timing equations:

1. Times for t_{RAH} and t_{ASC} at light loads are specified 2 ns longer than for normal−heavy loads. (See data sheet specifications.)
2. Light load is defined as 4 banks of four x 4 DRAMs
3. When using normal−heavy loads at 15 MHz a DELCLK divisor of 8 is used and when using light loads at 15 MHz a DELCLK divisor of 7 is used.

t_{RAHact} = 30 * [(DELCLK divisor * 2 MHz/DELCLK freq) − 1] ns + 15 ns (+2 ns for light load only)
= 30 * [(8 * 2 MHz/15 MHz) − 1]ns + 15 ns
= 17 ns @ 15 MHz Normal−Heavy Loads
= 30 * [(7 * 2 MHz/15 MHz) − 1]ns + 15 ns + 2 ns
= 15 ns @ 15 MHz Light Loads

t_{ASCact} = 15 * [DELCLK Divisor * 2 MHz/DELCLK Freq]ns − 15 ns (+2 ns for light load only)
= 15 * [8 * 2 MHz/15 MHz]ns − 15 ns
= 1 ns @ 15 MHz Normal−Heavy Loads
= 15 * [(7 * 2 MHz/15 MHz] ns − 15 ns + 2 ns
= 1 ns @ 15 MHz Light Loads

PARAMETER ADJUSTMENTS FOR 15 MHz DELCLK DUE TO CHANGED t_{RAH} and t_{ASC}

\$308act CLK High to $\overline{CAS}$ = Data Sheet Spec + (Actual t_{RAH} − Spec t_{RAH}) + (Actual t_{ASC} − Spec t_{ASC})
= 79 ns + (17 ns − 15 ns) + (1 ns − 0 ns)
= 82 ns @ 15 MHz Heavy Load **NS32CG821-25 Part**
= 89 ns + (17 ns − 15 ns) + (1 ns − 0 ns)
= 92 ns @ 15 MHz Heavy Load **NS32CG821-20 Part**
= 72 ns + (15 ns − 17 ns) + (1 ns − 2 ns)
= 69 ns @ 15 MHz Light Load **NS32CG821-25 Part**
= 81 ns + (15 ns − 17 ns) + (1 ns − 2 ns)
= 78 ns @ 15 MHz Light Load **NS32CG821-20 Part**

$316act CLK High to Column Address Valid

= Data sheet Spec + (Actual t_{RAH} − Specified t_{RAH})

= 75 ns + (17 ns − 15 ns)

= 77 ns @ 15 MHz Normal−Heavy Load **NS32CG821-20 Part**

= 87 ns + (17 ns − 15 ns)

= 89 ns @ 15 MHz Normal−Heavy Load **NS32CG821-20 Part**

= 66 ns + (15 ns − 17 ns)

= 64 ns @ 15 MHz Light Load **NS32CG821-25 Part**

= 78 ns + (15 ns − 17 ns)

= 76 ns @ 15 MHz Light Load **NS32CG821-20 Part**

ZERO WAIT STATES ANALYSIS FOR A 15 MHz NS32CG16

t_{RAC} = T2 + T3 − CLK to $\overline{RAS}$ − Transceiver Delay − Data Setup

= $2T_{cp}$ − $307 − t_{phl} − #t_{Dls}

= 133 ns − 26 ns − 7 ns − 15 ns

= 85 ns Normal−Heavy Load **NS32CG821-25 Part**

= 133 ns − 22 ns − 7 ns − 15 ns

= 89 ns Light Load **NS32CG821-25 Part**

t_{AA} = T2 + T3 − CLK to Column Address Valid − Transceiver Delay − Data Setup

= $2T_{cp}$ − $316act − t_{phl} − #t_{Dls}

= 133 ns − 77 ns − 7 ns − 15 ns

= 34 ns Normal−Heavy Load **NS32CG821-25 Part**

= 133 ns − 64 ns − 7 ns − 15 ns

= 47 ns Light Load **NS32CG821-25 Part**

t_{CAC} = T2 + T3 − CLK to $\overline{CAS}$ − Transceiver Delay − Data Setup

= $2T_{cp}$ − $308act − t_{phl} − #t_{Dls}

= 133 ns − 82 ns − 7 ns − 15 ns

= 29 ns Normal−Heavy Load **NS32CG821-25 Part**

= 133 ns − 69 ns − 7 ns − 15 ns

= 42 ns Light Load **NS32CG821-25 Part**

ONE WAIT STATE ANALYSIS FOR A 15 MHz NS32CG16

t_{RAC} = T2 + T_w + T3 − CLK to $\overline{RAS}$ − Transceiver Delay − Delay Setup

= $3T_{cp}$ − $307 − t_{phl} − #t_{Dls}

= 200 ns − 26 ns − 7 ns − 15 ns

= 152 ns Normal−Heavy Load **NS32CG821-25 Part**

= 200 ns − 22 ns − 7 ns − 15 ns

= 156 ns Light Load **NS32CG821-25 Part**

t_{AA} = T2 + T_w + T3 − CLK to Column Address Valid − Transceiver Delay − Data Setup

= $3T_{cp}$ − $316act − t_{phl} − #t_{Dls}

= 200 ns − 77 ns − 7 ns − 15 ns

= 101 ns Normal−Heavy Load **NS32CG821-25 Part**

= 200 ns − 64 ns − 7 ns − 15 ns

= 114 ns, Light Load **NS32CG821-25 Part**

t_{CAC} = T2 + T_w + T3 − CLK to $\overline{CAS}$ − Transceiver Delay − Data Setup $3T_{cp}$ − $308act − t_{phl} − #t_{Dls}

= 200 ns − 82 ns − 7 ns − 15 ns

= 96 ns Normal−Heavy Load **NS32CG821-25 Part**

= 200 ns − 69 ns − 7 ns − 15 ns

= 109 ns Light Load **NS32CG821-25 Part**

$\overline{RAS}$ PRECHARGE PARAMETER (FOR BOTH ZERO AND ONE WAIT STATE)

t_{RP} $\overline{RAS}$ Precharge Time

see DRAM data sheet (usually < 100 ns)

= T4 + T1 − CTTL to $\overline{TSO}$ Inactive + [(CLK High to $\overline{RAS}$ Asserted) − ($\overline{TSO}$ Negated to $\overline{RAS}$ Negated)]

= $2T_{cp}$ − t_{TSOia} + $53

= 133 ns − 10 ns + 4 ns

= 127 ns @ 15 MHz for NS32CG16

$\overline{RAS}$ LOW DURING REFRESH (FOR BOTH ZERO AND ONE WAIT STATE)

t_{RAS} = Programmed Clocks − [(CLK High to Refresh $\overline{RAS}$ Asserted) − (CKL High to Refresh $\overline{RAS}$ Negated)]

= $2T_{cp}$ − $55

= 133 ns − 6 ns

= 127 ns @ 15 MHz for NS32CG16

Programming Bits*

Bit	Value	Description
R1, R0	1, 0	$\overline{RAS}$ Low during Refresh = 2T $\overline{RAS}$ Precharge Time = 2T
R3, R2	0, 0 1, 1	No Wait States during Non-Delayed Access One Wait State during Non-Delayed Access
R5, R4	0, 0	No Wait States during Burst
R6	User Defined	Add Wait States with $\overline{WAITIN}$
R9	User Defined	Staggered or all $\overline{RAS}$ Refresh
C0, C1, C2	**	Divisor for DELCLK
C3	***	Time between Refreshes
C6, C5, C4	User Defined	Depends on User's DRAM Configurations
C7	1	Choose t_{ASC} = 0 ns
C8	1	Choose t_{RAH} = 15 ns
C9	1	Delay $\overline{CAS}$ for Write Accesses
B0	1	Address Latches are Fall Through

* $\overline{ECASO}$, B1, and R7 must be programmed low and R8 must be programmed high for operation of chip.

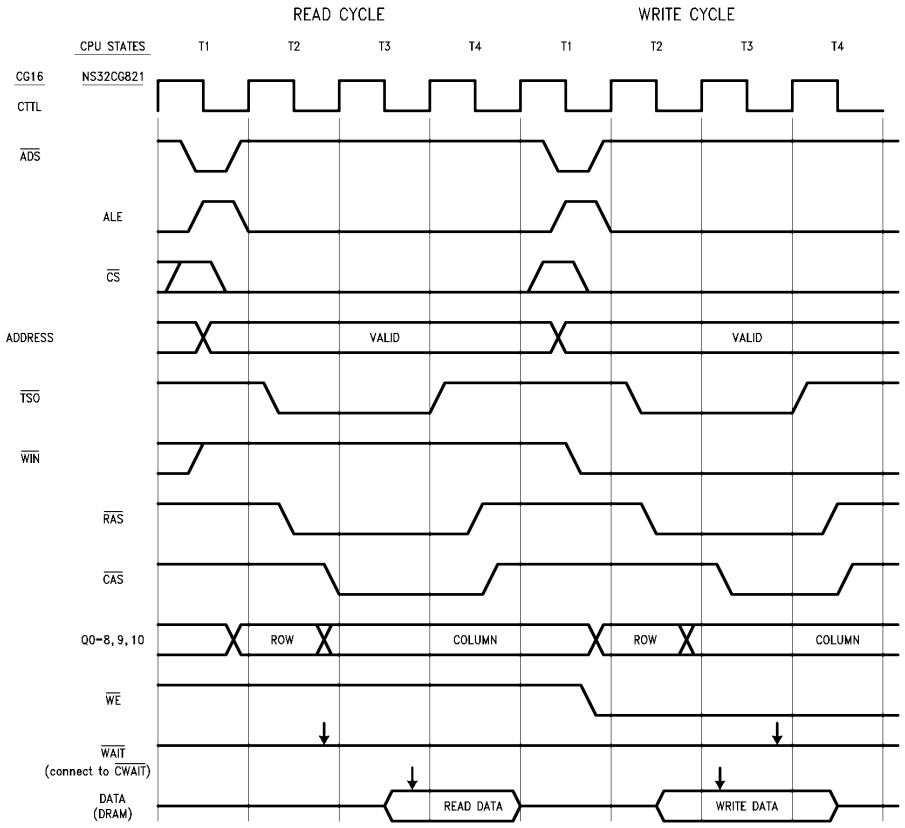
**Choose C2, C1, C0 =

1, 0, 1 for NS32CG16 @ 10 MHz
0, 1, 0 for NS32CG16 @ 15 MHz, w/Heavy Load
0, 1, 1 for NS32CG16 @ 15 MHz, w/Light Load

*** Choose C3 =

0 for NS32CGG16 @ 10 MHz
1 for NS32CG16 @ 15 MHz Normal−Heavy Load
0 for NS32CG16 @ 15 MHz Light Load

NS32CG16–NS32CG821 Dram Timing for 0 Wait States



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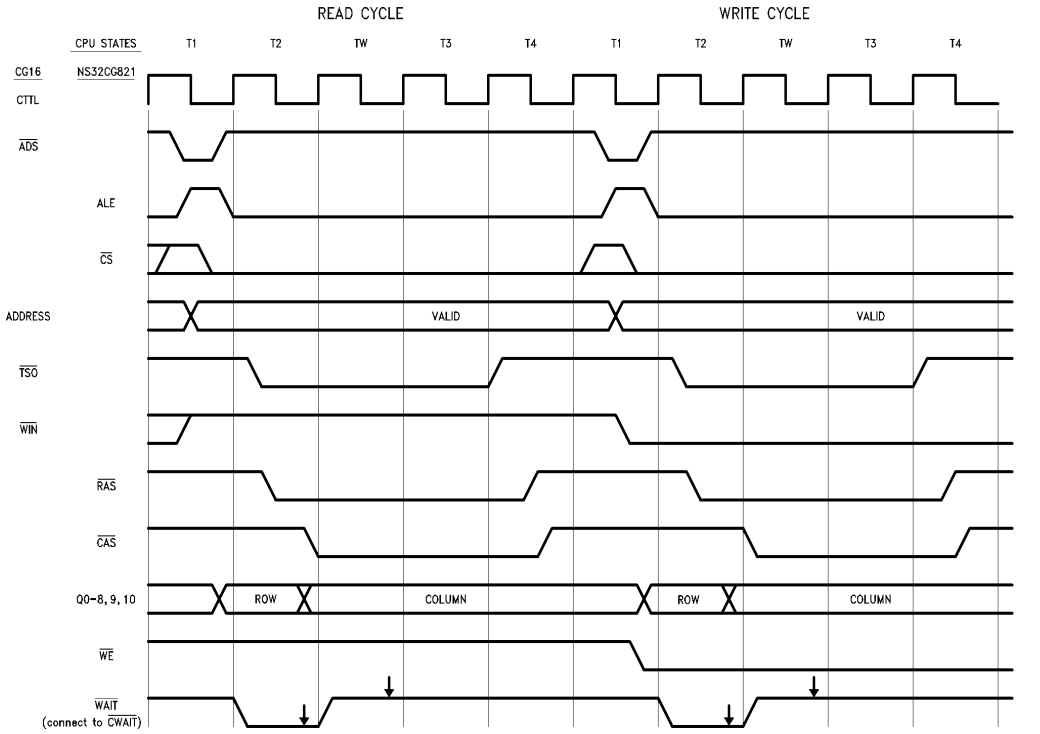
NS32CG16–NS32CG821 DRAM Timing with One Wait State



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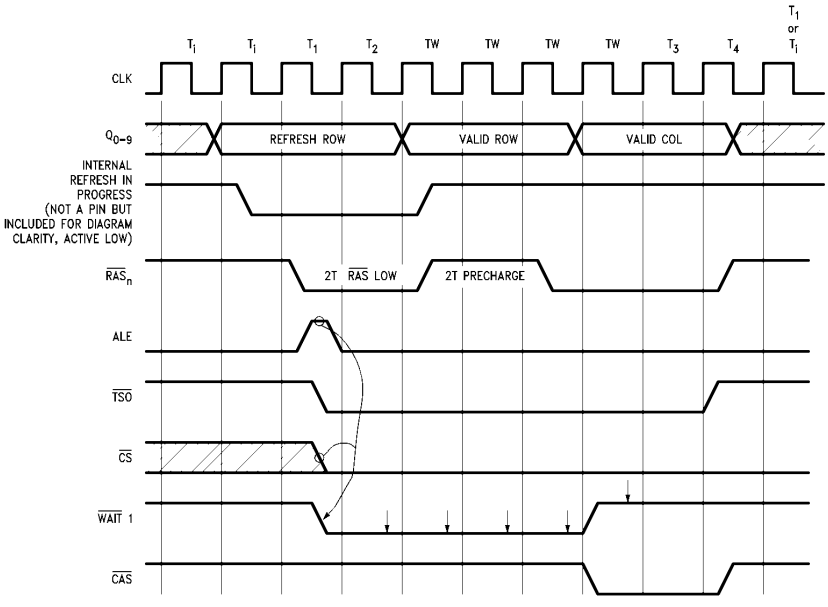
Access Request during an Internal Refresh Cycle (for One Wait State during Access)



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