DP8490: E.A.S.I. Does It!

National Semiconductor
Application Note 562
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National's Enhanced Asynchronous SCSI Interface (EASI) offers features that can yield increases in system performance over designs incorporating a 5380 type device.

When looking for a low cost Small Computer Systems Interface (SCSI) controller many users adopt the 5380 Asynchronous SCSI Interface (ASI) despite its many documented flaws and undocumented difficulties in operation, familiar to any past user. This device tended to be selected due to the lack of an alternative, but the DP8490 EASI from National Semiconductor will change this. The EASI is pin compatible with the ASI, and software compatible until an enhanced mode bit is set. This enhanced mode offers features which can increase the performance of a system currently using a 5380 type device. This is achieved through improvements to speed and architecture, while eliminating the 5380's inherent bugs.

SYSTEM OVERVIEW

The DP8490 and DP5380 support selection, reselection arbitration and all other bus phases as detailed in the ANS X3.131–1986 SCSI standard defined by the ANSI X3T9.2 committee. As the devices can act as both TARGET and INITIATOR they are suitable for any SCSI bus application. A typical application will look like *Figure 1*.

The C.P.U. controls all operations by reading and writing registers in the I/O devices; to achieve a high performance a member of the HPC16000 microcontroller family can be used. For optimum performance a DMA controller handles data transfers between the EASI and memory. The memory is used as a data cache for the final destination, which may be a hard disk, RAM disk, printer etc. *Figure 1* shows the basic system but not the hardware required to interface to such a peripheral. The EASI has high-current open-drain drivers which interface directly to the SCSI bus.

SPEED AND POWER IMPROVEMENTS

National's DP8490, and DP5380, are implemented in low voltage silicon gate microCMOS, which gives power and speed improvements over existing NMOS 5380 parts. The National devices have a maximum supply current of 4 mA, compared to the NCR5380 145 mA, and DMA rates of over 3 Mbytes/second, compared to 1.5 Mbytes/second. National's EASI device has reduced timing parameters; read access times are reduced from 130 ns to 50 ns, write data hold times, from 30 ns to 10 ns and all other parameters correspondingly improved.

ENHANCED INTERRUPTS

The DP8490 enhanced mode interrupt structure is considerably different to that of the 5380. The source of interrupt is available by reading one register, the Interrupt Status Register (ISR). In order to find the source of interrupt in the 5380 two registers must be read. In addition all interrupts are flagged in enhanced mode. With the 5380 a selection interrupt has to be determined by the absence of other flags while the select line is active. Since selection is the means of establishing contact with other devices on the SCSI bus it is a common occurrence. The DP8490 supplies an interrupt flag for this and all other interrupts. This enhanced interrupt structure should simplify system software, thus increasing the speed of interrupt servicing. Simplified code is easier to understand, and therefore easier to adapt or repair.

All interrupts are maskable, using the Interrupt Mask Register (IMR), but interrupts cannot be lost since resetting the interrupts only resets those bits that were active on the last read of the ISR. This achieves a greater error tolerance.

INTERRUPT DRIVEN ARBITRATION

An enhancement which will have a great effect on many system's performance is the addition of an arbitration interrupt. In the 5380, arbitration is polled. On a busy SCSI bus, arbitration will take typically many milliseconds, and potentially many seconds. Therefore, time which could have been spent doing overlapped seeks, or filling a data buffer is instead used reading a 5380 register waiting for a flag to go active. The enhanced mode of the DP8490 offers interrupt driven arbitration, allowing the user to utilize this time in data cacheing, data manipulation, etc., thus increasing the system throughput. This increase in system performance can become particularly effective in low priority devices which will typically have to arbitrate for the bus the longest.

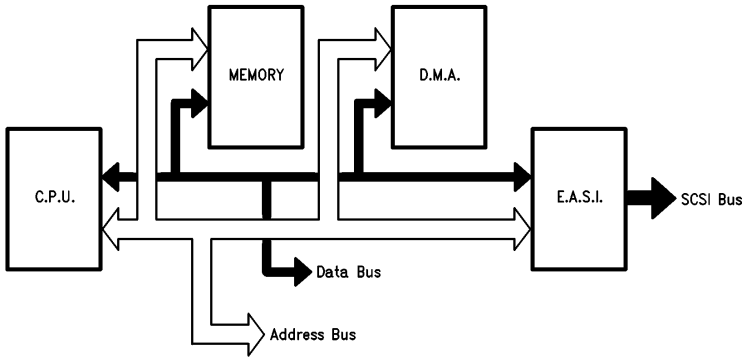

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FIGURE 1

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INCREASED TESTABILITY

The enhanced mode is set using a register bit which, in the 5380 initiates the 'Test Mode'. In Test Mode all output drivers on the device are disabled, so although the device can still be written, no data can be read. This makes it unsuitable for any application. In addition, DMA and interrupt requests are tri-stated, which may cause system problems.

In contrast, the enhanced mode of the DP8490 offers a loopback facility, where the SCSI drivers are disabled, and the SCSI I/O's loop back inside the EASI. This loopback test mode allows all device signals to be fully tested, including a DMA transfer. Using this, a system can perform a full self diagnostic test, without affecting the SCSI bus. Good diagnostic testing simplifies system error detection and checking.

TRUE END OF DMA DETECTION

Another interrupt improvement in the enhanced mode is seen during DMA operation. The 5380 will generate an end of DMA interrupt when it sees a concurrent EOP, DACK and IOR or IOW, even though the SCSI bus transfer may not be complete. To overcome this the user must examine REQ and ACK, to determine a true end of transfer. Consider *Figure 2*:

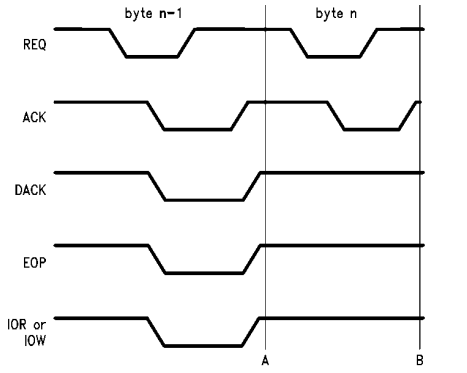

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FIGURE 2

If an initiator is slow in removing the ACK, the processor could sample REQ and ACK after the EOP interrupt, at point A. At this point REQ and ACK are both inactive, although there is still one byte to transfer. The user must see REQ and ACK inactive on three successive transfers to be confident the transfer is complete (point B). Thus a great deal of time is wasted ensuring the last byte of every DMA transfer is successful. The EASI eliminates this inefficiency by detecting, and interrupting on, true end of DMA, when ACK goes inactive.

TIMING ENHANCEMENTS

Some of the major bugs in the 5380 are experienced in DMA mode. In initiator receive mode, if a REQ is received, after a valid EOP, an ACK will be generated although no valid data exists. This could be a particular problem for users who have to split a block transfer into two, perhaps to prevent crossing a page boundary. Part of the second block of data could be lost by the generation of these spurious ACK's. Another problem experienced by an initiator in DMA mode is ACK being left asserted after receipt of a valid EOP. After receiving the end of DMA interrupt the processor must 'manually' deassert ACK by writing to the relevant register.

These problems make the DMA mode in a 5380 extremely difficult to use. Extra software is required to ensure correct operation, making boards incorporating a 5380 run slower. **None of these problems exist in the enhanced mode of the DP8490**.

BUS TERMINATION

The most common SCSI bus is a 50 way ribbon cable, of up to six meters long, with SCSI devices daisy chained along it. The devices at either end of the bus should terminate all SCSI lines with a 330Ω resistor to ground and a 220Ω to power. To ensure the bus can operate correctly, even if the device at one end is not powered up, the power to these terminators can be made available on the SCSI bus. This allows the terminators to always receive power. The bus configuration is shown in *Figure 3*. Terminator power is fed through a Schottky diode to prevent a backflow of power into either of the devices.

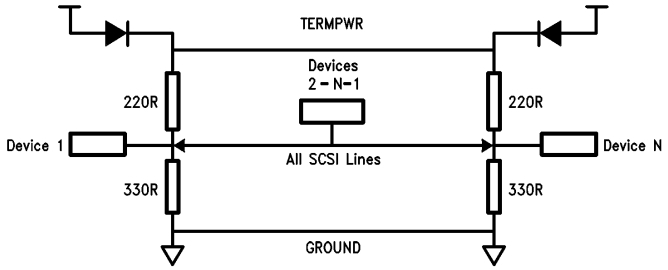

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FIGURE 3

Some manufacturers' CMOS devices will not work in this configuration, since when not receiving power they pull the SCSI line low. Therefore all devices on the bus must be powered up. Both National's DP5380 and DP8490 have a special input protection which makes this configuration acceptable.

EXTENDED FEATURES

The DP5380 and DP8490 are available in a standard 40 pin DIP, or in a 44 pin PLCC, which is pin compatible with existing 5380 PLCCs. The DP8490 PLCC has a microprocessor parity pin. In the enhanced mode, microprocessor bus parity checking can be enabled, with parity polarity optional. Since parity checking is optional, the PLCC DP8490 can still be used in a system where the microprocessor does not support parity. However, use of this feature will help the confirmation of data validity throughout the system.

Enhanced mode (for both types of packaging) offers other features, including programmable SCSI parity polarity. Although the specified SCSI polarity is ODD, by enabling EVEN parity bus diagnostics can be carried out. In this way the error detection and error handling capabilities of other devices on the bus can be determined.

The enhanced mode also has a general phase mismatch interrupt. The 5380 only checks phase mismatch during DMA. This means that an initiator following the phase set by a target must poll the device to determine when it changes. Only a change during DMA produces an interrupt. In the enhanced mode, an option available gives an interrupt on any phase mismatch. This allows for quicker detection of a change of phase, thus decreasing the dead time on the SCSI bus.

The wide range of new features available in the DP8490 makes this part a first choice in any new SCSI designs, or upgrades requiring increased performance. For users not wishing to make the software changes, required to utilize the enhanced features of the DP8490, the DP5380 is available, offering speed and power improvements over existing parts, at a highly competitive cost. Every user that has tried replacing existing NMOS 5380s with either the DP5380 or DP8490, at both ends of their existing application, have experienced data transfer speed improvements of between 10% and 15%. That is with no other changes!

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