Interfacing Memory to the NS32532

National Semiconductor
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The overall throughput of microprocessor systems often depends on the performance of the memory subsystem. To achieve optimum throughput with a high-performance microprocessor such as the NS32532, memory should operate with few or no wait states. The processor's clock frequency and the speed of memory components determine the number of wait states. This Application Note discusses design considerations for interfacing DRAM and SRAM to the NS32532. It covers four topics:

- An overview of NS32532 memory interface requirements
- A simple SRAM interface
- An interleaved SRAM interface
- A simple DRAM interface

BACKGROUND

The NS32532 microprocessor communicates with its environment via parallel busses and signals. These include a 32-bit data bus, a 32-bit address bus, a number of control signals, and five bus status pins.

The processor has instruction and data caches as well as an on-chip Memory Management Unit (MMU) to reduce bus utilization, thereby increasing throughput. The MMU uses page tables in external memory to perform logical-to-physical address translation. In order to minimize page table accesses, the NS32532 maintains a Translation Look-aside Buffer (TLB) containing information about frequently-used addresses. When the TLB does not contain needed information, the NS32532 fetches it from the external page tables. The on-chip caches duplicate a subset of external memory. The contents of an on-chip cache are acquired in one clock cycle, while it takes a minimum of two clocks to fetch data from external memory. Therefore, on-chip caches substantially reduce average memory access time when they contain the code and data the processor needs.

On each memory access, the processor initiates a memory access cycle while searching the internal cache. This reduces access time, since the memory cycle is already in process when the cache does not contain the needed information. During a read that fails to find the data in the cache (a cache miss), the memory cycle continues and the processor fetches the data from external memory. Unless declared non-cacheable, the information is placed in the internal instruction or data cache for future reference. Conversely, when the instruction or data cache contains the sought information (a cache hit), the processor cancels the memory access cycle.

A memory write is always treated as a cache miss, so that external memory is updated; this is a ''write through'' cache policy. When an internal cache contains a copy of the memory location being updated, the processor also updates the cache using a ''write allocate'' cache policy, thus ensuring that both copies of the data are the same.

MEMORY ORGANIZATION

The 32-bit address bus of the NS32532 provides up to 4 Gbytes of memory in a uniform linear address space starting at zero and ending at $2^{32}-1$. Each memory location contains an eight-bit byte. Two contiguous bytes form a word, and two contiguous words are a double-word. A word or double-word can start at any address, since there are no memory alignment requirements with the Series 32000® processors. Although addressable as bytes, memory is organized as double-words, where the address of a double-word is the address of its least significant byte.

While the NS32532 has no address alignment requirements, alignment affects the time to access a word or double-word. The processor more quickly accesses a double-word whose address is a multiple of four than one whose address is otherwise; it takes two memory cycles to fetch non-double-word aligned data.

The NS32532 supports the memory mapping of peripheral devices and coprocessors. Such devices can be located anywhere in the address space except for the upper 8 MB (addresses $FF800000_{16}$ through $FFFFFFFF_{16}$), which are reserved. The following section describes the bus signals required for memory or I/O interfacing.

BUS INTERFACE

The NS32532 performs six types of bus operations:

1. Instruction fetch
2. Memory or I/O read
3. Memory or I/O write
4. Read or update page table entries
5. Acknowledge interrupt or completion of interrupt service routine
6. Transfer information to/from Slave Processor

Cases 1 through 5 have identical bus timing characteristics and are discussed below. The only external difference among these cases is a six-bit code placed on the bus status pins (ST_0–ST_5) during bus cycles for the purpose of identifying which operation is occurring. Case 6 has separate control signals; Slave Processor operation is not relevant to this Application Note and is not discussed here.

The NS32532 can ''burst read'' up to four consecutive double-words from memory. This feature reduces the amount of time the processor spends on the memory bus while increasing the hit rate of internal caches. Details of burst operation appear later in this document.

The I/O signals of the NS32532 support interfacing to memory, memory-mapped devices, slave processors, and external caches. The following control signals implement RAM interfacing on any system without the external cache:

- D_0–D_{31}: Bidirectional data bus. Either 8, 16, or 32 bits of data are transferred at a time. D_0 is the least significant bit.
- A_0–A_{31}: Address bus. A_0 is the least significant bit.
- $\overline{ADS}$: Address strobe. Indicates that a bus cycle has begun and a valid address is on the bus. This signal is the earliest indication of a bus cycle in progress. The bus cycle may potentially be cancelled in event of an internal cache hit.
- $\overline{BE}_0$–$\overline{BE}_3$: Byte enable. These signals indicate which bytes should be selected for transfer. During write cycles, $\overline{BE}_0$–$\overline{BE}_3$ enable the memory banks for writing. During reads, they select the appropriate banks of an I/O device

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that may exhibit undesired effects of reading intended only for some banks. During cacheable read cycles, the processor reads all bytes regardless of how the byte enable signals are encoded. Thus all memory banks should be selected for a cacheable read cycle, disregarding $\overline{BE}_0$–$\overline{BE}_3$.

- $\overline{BMT}$: Begin memory transaction. This signal indicates that a bus cycle has begun. The processor may cancel the bus cycle and negate $\overline{BMT}$ if there is an internal cache hit. This signal cannot be used as a strobe in read cycles. However, in a write cycle due to ''write through'' implementation of the internal caches, this signal can be used as a strobe to start a bus cycle.
- $\overline{CONF}$: Confirmation. Indicates that a bus cycle initiated by $\overline{ADS}$ is valid and has not been cancelled. This signal should be used to start a memory transfer or proceed with a memory transfer that has already been initiated.
- ST_0–ST_5: Bus status. These six bits indicate the type of bus cycle currently in progress. If the processor is idle on the bus, these outputs indicate why.
- U/$\overline{S}$: User or supervisor. Specifies the address space (user or supervisor) of the current bus cycle.
- $\overline{DDIN}$: Data direction in. Indicating the direction of data transfer, this signal is used to generate read and write strobes.
- $\overline{BOUT}$: Burst out. The processor asserts this signal to request a burst cycle. Due to the timing of $\overline{BOUT}$ activation, it should not be used as a burst request or to generate the $\overline{BIN}$ signal (described next). Instead, it should be monitored to continue or terminate a burst that has already been initiated.
- $\overline{BIN}$: Burst in. Notifies the processor if the memory supports burst cycles. The memory controller should not wait for $\overline{BOUT}$ before asserting this signal. The address decoder should determine whether or not to assert $\overline{BIN}$.
- $\overline{RDY}$: Ready. Notifies the processor when memory or a peripheral device is ready to transfer data. If this signal is not active, the processor inserts wait states to extend the current bus cycle, thus supporting slow memory and peripheral devices.
- $\overline{BER}$: Bus error. Indicates that an error has occurred during the bus cycle. The processor treats $\overline{BER}$ as the highest priority exception after reset, and executes the $\overline{BER}$ exception routine.
- $\overline{BRT}$: Bus retry. Indicates that the current bus cycle should be retried. The processor will reexecute the bus cycle.
- CLK: Input clock signal. The 32000 series requires a single-phase clock signal running at a frequency twice that of the processor's operating speed in MHz. CLK is internally divided to generate two non-overlapping clock signals, BCLK and $\overline{BCLK}$.
- BCLK: Bus clock. One of the clock output signals derived from CLK.
- $\overline{BCLK}$: Complementary bus clock. This signal should be used for timing reference and for synchronization of external devices with the processor.

Figure 1 is the timing diagram for a read cycle, and *Figure 2* for a write. Both figures assume that the selected memory or peripheral device is capable of communicating with the processor at full speed.

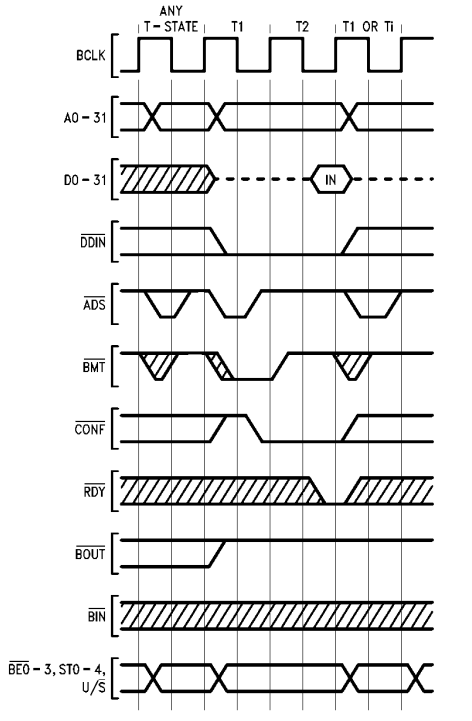

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FIGURE 1. Basic Read Cycle

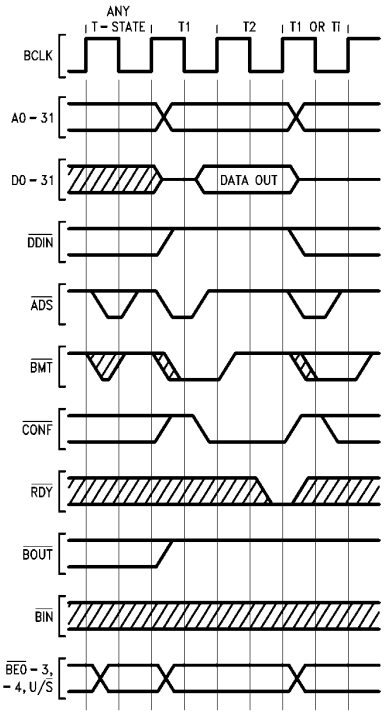

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FIGURE 2. Basic Write Cycle

A full-speed bus access occurs during two cycles of BCLK, T1 and T2. The processor asserts $\overline{ADS}$ during the first half of T1 to indicate the start of a bus cycle for both reads and writes. From the beginning of T1 until completion of the bus cycle, the processor drives the address bus and other relevant control signals as the timing diagrams indicate. The processor asserts $\overline{CONF}$ in the middle of T1 if the bus cycle is not cancelled and T2 will be entered with the next clock cycle. $\overline{BMT}$ may be asserted at the start of the cycle and then deasserted before the time it is guaranteed valid. This is caused by an internal cache hit, which cancels the initiated bus cycle. A confirmed bus cycle completes at the end of T2 unless $\overline{RDY}$ is high, in which case the processor inserts additional T2 (wait) states.

For write bus cycles, valid data is output from the middle of T1 until the end of the cycle (T2). Due to write-through implementation of the internal caches, write cycles are not cancelled. When one write cycle immediately follows another, the processor continues driving the bus with data from the previous operation until the middle of state T1 of the second bus cycle.

Following state T2 is either state T1 of the next bus cycle or an idle T-state if the processor has no bus cycle to perform.

BURST CYCLES

The NS32532 is capable of performing burst transfers, which increase bus efficiency and tend to raise the internal cache hit rate. Burst is only available in instruction fetch and data read cycles from 32-bit memories. *Figure 3* is the burst cycle timing diagram, which assumes no wait states.

A burst cycle consists of two parts. The first is a regular (opening) cycle, in which the processor outputs its status and asserts the relevant control signals. The processor asserts $\overline{BOUT}$ to indicate that it wants to perform burst cycles. If the selected memory supports burst mode, it notifies the processor via $\overline{BIN}$ low. If the memory does not allow burst ($\overline{BIN}$ high) and the cycle extension has not been requested via $\overline{RDY}$, the memory cycle terminates at the end of T2 and the processor deasserts $\overline{BOUT}$. If the memory supports burst and the processor has not deasserted $\overline{BOUT}$, the second part of the burst cycle occurs and $\overline{BOUT}$ remains active until termination of the operation.

The second part of the burst consists of up to three nibbles in state T2B. In each of these nibbles, the processor reads a 32-bit data item. After each data read, address bits A_0–A_1 go to zero and A_2–A_3 increment, and all byte enable out-

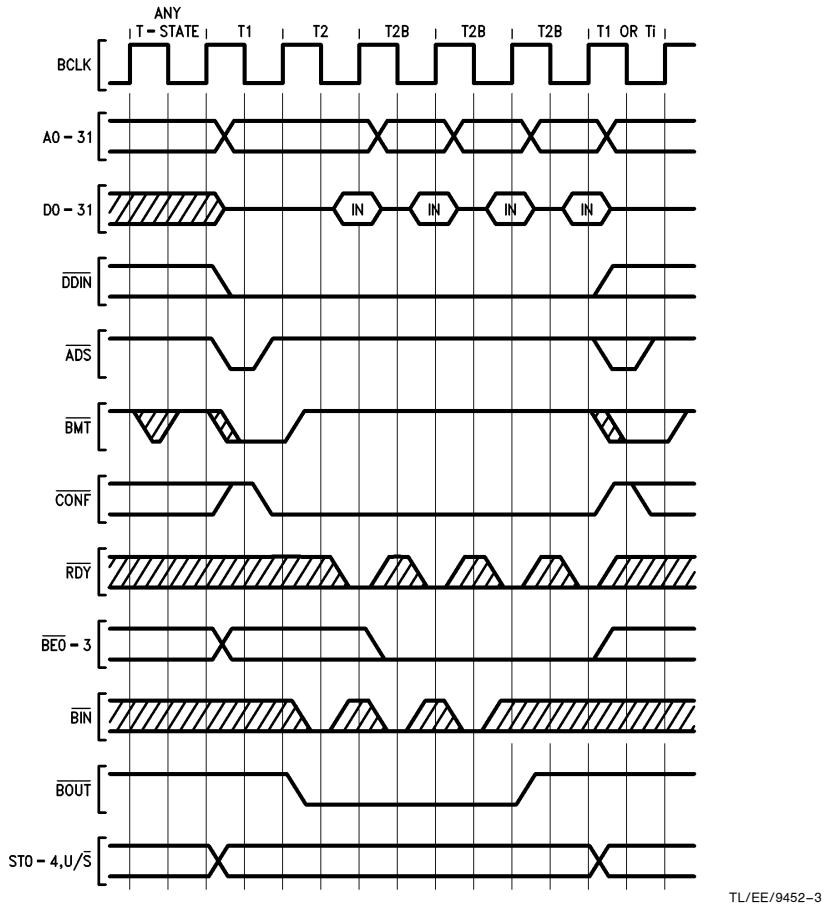

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FIGURE 3. Burst Read Cycle

puts $\overline{BE}_0$–$\overline{BE}_3$ are activated. If the $\overline{RDY}$ pin is high at the end of each T2B, the processor inserts additional T2B states to allow slow memories to work with the burst cycle.

The following sections discuss three simple designs. The first two work at up to 30 MHz, and the third at 30 MHz. The first design is a simple SRAM interface that requires no wait states on regular memory cycles. However, it requires one wait state in each nibble access at speeds higher than 20 MHz. The second design shows an interleaved memory implementation on burst access cycles, eliminating the single wait state of the first design and thus operating with memory at full speed. The third design shows a simple DRAM interface to the NS32532. This design inserts three wait states in a regular memory cycle, but only one wait state in each nibble transfer at 30 MHz.

All three designs use PAL® devices for address decoding. Standard driver, 74AS1034, are used to increase drive where the processor address bus lacks the necessary drive capability. High speed 8-bit transceivers, 74PCT245, provide isolation and additional drive capability for the data bus.

SIMPLE SRAM MEMORY INTERFACE TO THE NS32532

This section presents the results of a timing analysis and describes an SRAM interface for the NS32532 optimized for simplicity and cost. The interface does not utilize the processor's Bus Error and Bus Retry features.

This design allows all memory writes and the opening cycle of memory reads to proceed without wait states at any frequency up to 30 MHz. It also supports the NS32532's burst mode without wait states at up to 20 MHz. For burst transfers at 25 MHz and 30 MHz, one wait state is inserted in each nibble via jumper W1. *Figure 4* shows the timing diagram of the interface.

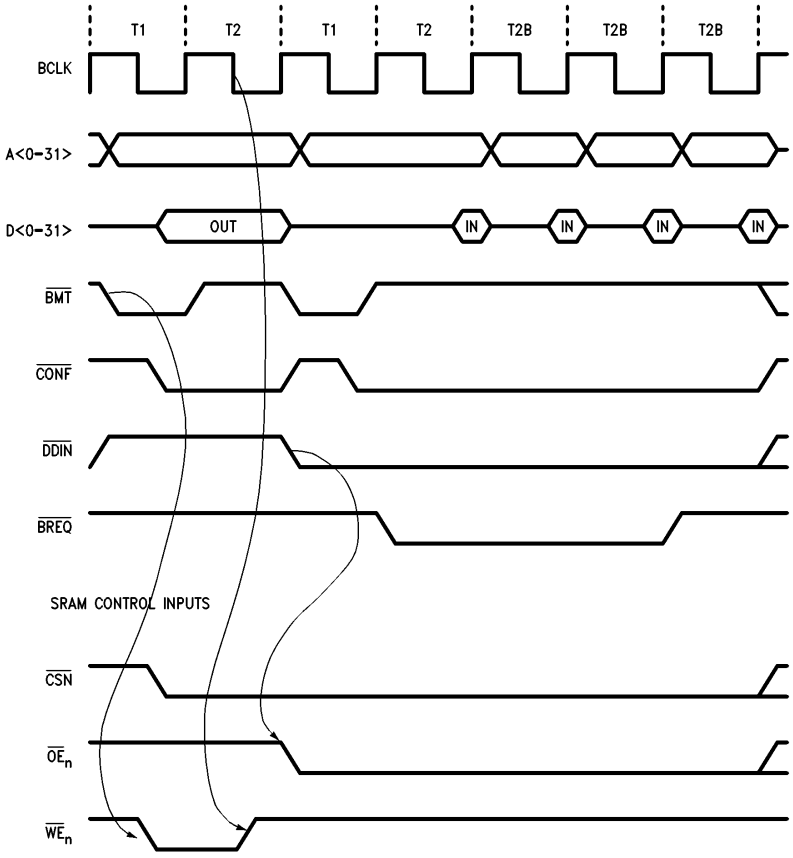

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FIGURE 4. Timing Diagram of the Simple SRAM Interface

The basis of the design is a state machine implemented by PAL16R4D (see Appendix A for state diagram PAL equations and schematics). This PAL keeps track of the processor state and drives the $\overline{RDY}$ signal high if a wait state needs to be inserted in the nibble transfer. The processor increments A_2–A_3 during burst access cycles.

Another PAL (16L8D) generates the write strobe for memory banks. The memory write strobe is generated by $\overline{BMT}$ during write cycles (DDIN high) and terminated by the rising edge of BCLK during T2. The memory write strobe is qualified with $\overline{BE}_0$–$\overline{BE}_3$ before being routed to the memory banks. A second PAL16L8D provides address decoding, generating the $\overline{MEMRD}$ signal when the memory is addressed in a read cycle with burst allowed.

This SRAM interface uses 25 ns static RAMs, Fast or Advanced Schottky TTL gates, and D type PALs to achieve no wait state operation during regular memory cycles. During burst memory transfers at processor speeds over 20 MHz, one wait state is required in each nibble cycle for correct operation. This wait state causes only a 3% performance degradation on average.

INTERLEAVED SRAM MEMORY INTERFACE TO THE NS32532

This section presents the results of a timing analysis and describes an NS32532 SRAM interface optimized for speed and simplicity. The interface does not utilize the processor's Bus Error and Bus Retry features. Memory banks are accessed concurrently and the data is read in an interleaved fashion during burst transfers, thus eliminating the need for wait states during nibble cycles.

This design provides for operation of the NS32532 at up to 30 MHz without wait states during regular and burst memory accesses. The latched A_2 bit of the processor enables memory banks for read or write. Reads from memory banks are interleaved during burst access cycles. This way the address setup for one bank overlaps with the data read from another. *Figure 5* shows the interface's timing diagram.

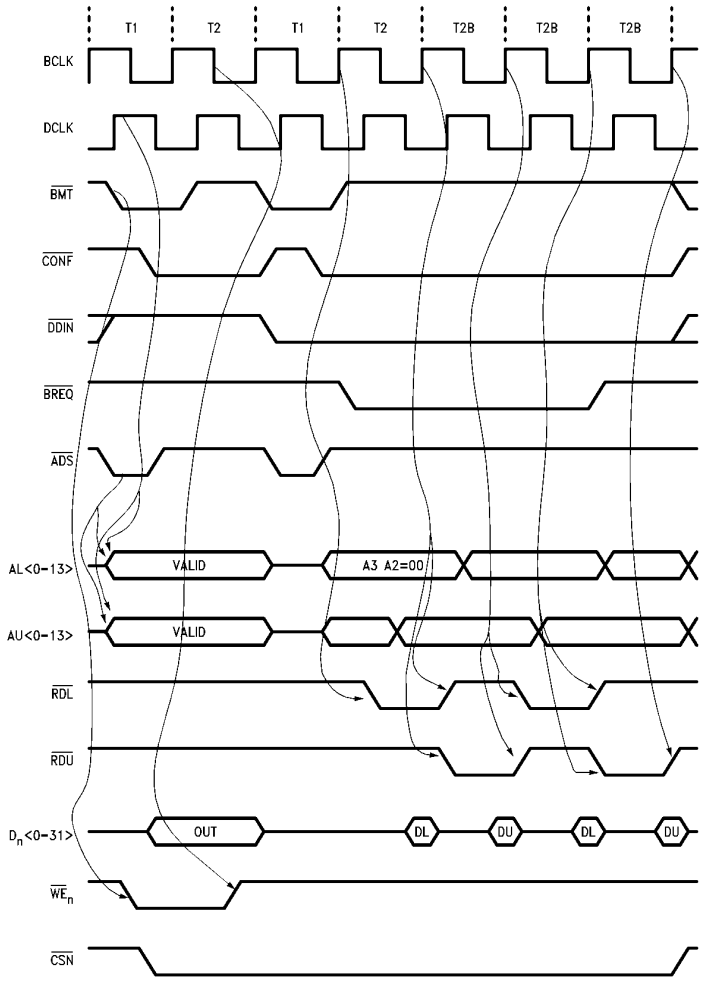

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FIGURE 5. Timing Diagram of the Interleaved SRAM Interface

Four PALs implement the design: two for the processor state machine and specific memory control signals, one for generating write strobes, and one for address decoding (see Appendix B for state diagram PAL equations and schematics). PAL16R4D implements the state machine. It uses the latched A_2–A_3 bits to control the selection of memory banks during a burst access, alternating the assertion of $\overline{RDL}$ and $\overline{RDU}$ in successive cycles. The A_3 value is set up in a given cycle, for a bank that will be enabled in the subsequent cycle via $\overline{RDL}$ or $\overline{RDU}$ inputs. A_3 should fall through the D flip-flops in order to meet the address setup time for the SRAM in the opening cycle. To do this, a pulse is generated by qualifying a skewed clock (DCLK) with $\overline{ADS}$. This pulse clocks A_3 in the D flip-flops. For proper operation at different processor frequencies, the jumpers should be installed as follows:

- 1–2 for 30 MHz
- 3–4 for 25 MHz
- 5–6 for 20 MHz

After the opening cycle, the Set and Clear inputs of the D flip-flops change the A_3 value under control of the state machine PAL.

PAL16L8D generates the memory write strobe from $\overline{BMT}$ during write cycles (DDIN high) and terminates it on the rising edge of BCLK during T2. The memory strobe is qualified with $\overline{BE}_0$–$\overline{BE}_3$ before being routed to the memory banks.

The third PAL (16L8D) is the address decoder. It generates $\overline{MEMRD}$ when the memory is addressed in read cycles and burst is allowed. 74AS1034 is used as the buffer driver where the processor output pins lack the necessary drive capability.

This SRAM interface uses 25 ns static RAMs, Fast or Advanced Schottky TTL gates, and type D PALs to achieve no wait state operation during regular memory cycles. During burst transfers, the interleaving of memory banks allows no wait state operation of the processor up to 30 MHz.

SIMPLE DRAM INTERFACE TO THE NS32532

This section presents the results of a timing analysis and describes a DRAM interface to the NS32532 optimized for speed and simplicity. The interface, which operates at 30 MHz and does not utilize the Bus Error and Bus Retry features of the processor, uses 80 ns DRAMs to minimize the number of wait states. All $\overline{RAS}$ signals are activated during a normal DRAM access and refresh cycle. During write cycles, only the $\overline{CAS}$ signals corresponding to the enabled bytes are active, while all $\overline{CAS}$ signals are active during reads. *Figure 6* shows the interface timing diagram.

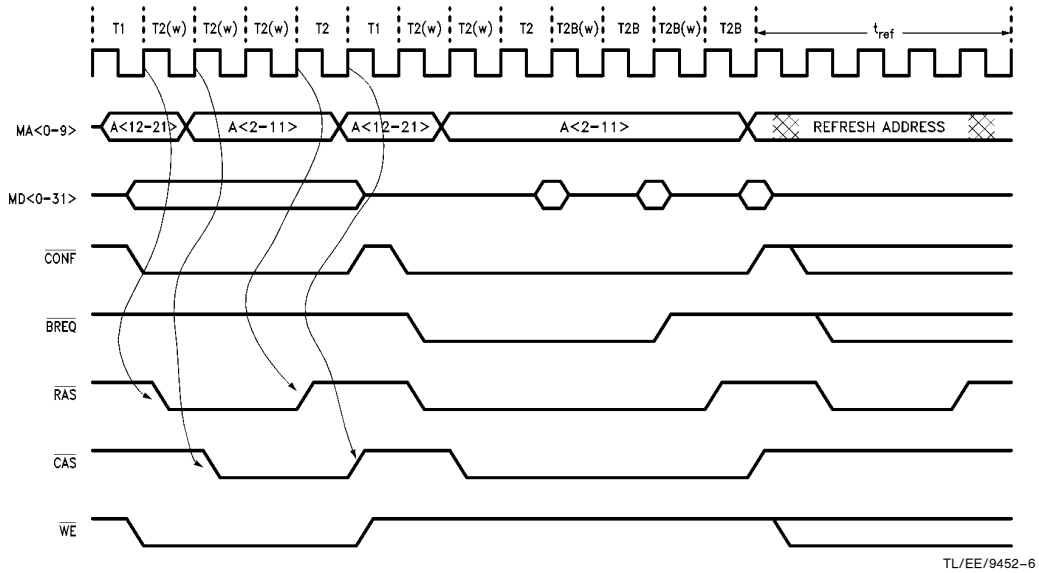

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FIGURE 6. Timing Diagram of the Simple DRAM Interface

The design uses five PALs: two for generating refresh address and refresh request, one for the state machine, one for generating $\overline{CAS}$ strobes, and one for address decoding (see Appendix C for state diagram PAL equations and schematics).

PAL16R8D implements the state machine. It keeps track of the processor state and drives the $\overline{RDY}$ signals high when wait states are inserted into bus cycles. This design uses static column DRAM, although it could use nibble mode DRAM with a simple modification to the state machine. Static column DRAM simplifies the design since the processor drives and increments A_2–A_3 during burst access cycles without the need to toggle $\overline{CAS}$. With nibble mode DRAM, the $\overline{CAS}$ lines must be toggled during nibble cycles.

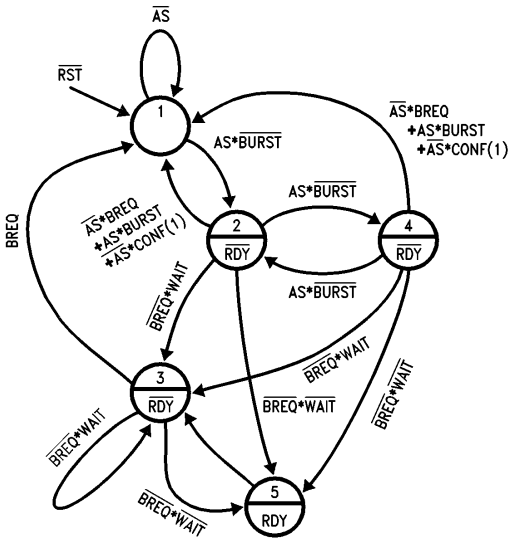
Two PAL20X10s generate the refresh address and refresh request. One PAL is the refresh address counter, which increments at the end of each refresh period. Its outputs drive the address lines of the DRAMs (row address) during the refresh period. The other PAL is the refresh interval counter, generating a refresh request ($\overline{RFRQ}$) approximately every eight μs. Clocked by BCLK, it must be modified if this interface operates at speeds other than 30 MHz. To make the PAL accommodate different speeds, a load term can be used in the PAL equations, with PAL inputs jumpered to ground or V_{CC}.

PAL16L8D generates the $\overline{CAS}$ strobes for the memory banks. In read cycles, all $\overline{CAS}$ strobes are asserted on the assumption that memory is cacheable, whereas in write cycles, the $\overline{CAS}$ strobes are qualified with $\overline{BE_0}$–$\overline{BE_3}$ before being routed to the memory banks. The memory write strobe is derived from DDIN. The data transceivers establish their direction from DDIN and are enabled by $\overline{CONF}$. The data transceivers are recommended, but not necessary to have this interface operating.

This DRAM interface uses 80 ns column DRAMs, Fast or Advanced Schottky TTL gates, and type D PALs. It achieves regular memory transfers in five cycles and burst nibbles in two cycles. It is possible to operate the NS32532 with fewer wait states by employing RAS prediction. A future Application Note will discuss features such as RAS prediction and error detection and correction.

Appendix A

State Diagram of the Simple SRAM Interface



TL/EE/9452–7

Note 1: This condition is a subset of /AS*BREQ condition.

```
PAL16R4D
STATE MACHINE PAL
STATE MACHINE PAL, WAIT STATE GENERATOR
NATIONAL SEMICONDUCTOR CORP, SANTA CLARA, CALIFORNIA
CLK NC NC WAIT RST BURST NC AS BREQ GND
OE NC A B C D NC NC NC VCC
A := A * B * /D * /BREQ * /WAIT * RST + A * C * /D * /BREQ * /WAIT * RST
B := A * B * /D * /BREQ * WAIT * RST + A * C * /D * /BREQ * WAIT * RST
     + /A * B * C * D * RST
C := A * B * C * /D * AS * /BURST * RST
D := A * B * C * AS * /BURST * RST + A * B * /D * AS * /BURST * RST
     + A * B * /D * /BREQ * WAIT * RST + A * C * /D * /BREQ * WAIT * RST
     + /A * B * C * D * RST
```

```
PAL16L8D
WRITE STROBE GENERATOR
WRITE STROBE GENERATOR FOR SRAM BANKS
NATIONAL SEMICONDUCTOR, SANTA CLARA, CALIFORNIA
BE0 BE1 BE2 BE3 BDDIN A16 CONF BMT NC GND
BCLK WL0 WL2 WL3 WU0 WU1 WU2 WU3 WL1 VCC
/WL0  =  /BMT * BDDIN * /BE0 * /A16 + BCLK * /CONF * BDDIN * /BE0 * /A16
/WL1  =  /BMT * BDDIN * /BE1 * /A16 + BCLK * /CONF * BDDIN * /BE1 * /A16
/WL2  =  /BMT * BDDIN * /BE2 * /A16 + BCLK * /CONF * BDDIN * /BE2 * /A16
/WL3  =  /BMT * BDDIN * /BE3 * /A16 + BCLK * /CONF * BDDIN * /BE3 * /A16
/WU0  =  /BMT * BDDIN * /BE0 * A16 + BCLK * /CONF * BDDIN * /BE0 * A16
/WU1  =  /BMT * BDDIN * /BE1 * A16 + BCLK * /CONF * BDDIN * /BE1 * A16
/WU2  =  /BMT * BDDIN * /BE2 * A16 + BCLK * /CONF * BDDIN * /BE2 * A16
/WU3  =  /BMT * BDDIN * /BE3 * A16 + BCLK * /CONF * BDDIN * /BE3 * A16

PAL16L8D
ADDRESS DECODE PAL
ADDRESS DECODER FOR THE SRAM BANKS
NATIONAL SEMICONDUCTOR, SANTA CLARA, CALIFORNIA
F1 F2 F3 A17 A16 NC NC NC NC GND
BDDIN NC CSL CSU NC NC NC BURST NC VCC
/CSL    =  F1 * F2 * F3 * /A16 * /A17
/CSU    =  F1 * F2 * F3 * A16 * /A17
/BURST  =  F1 * F2 * F3 * /A17 * /BDDIN
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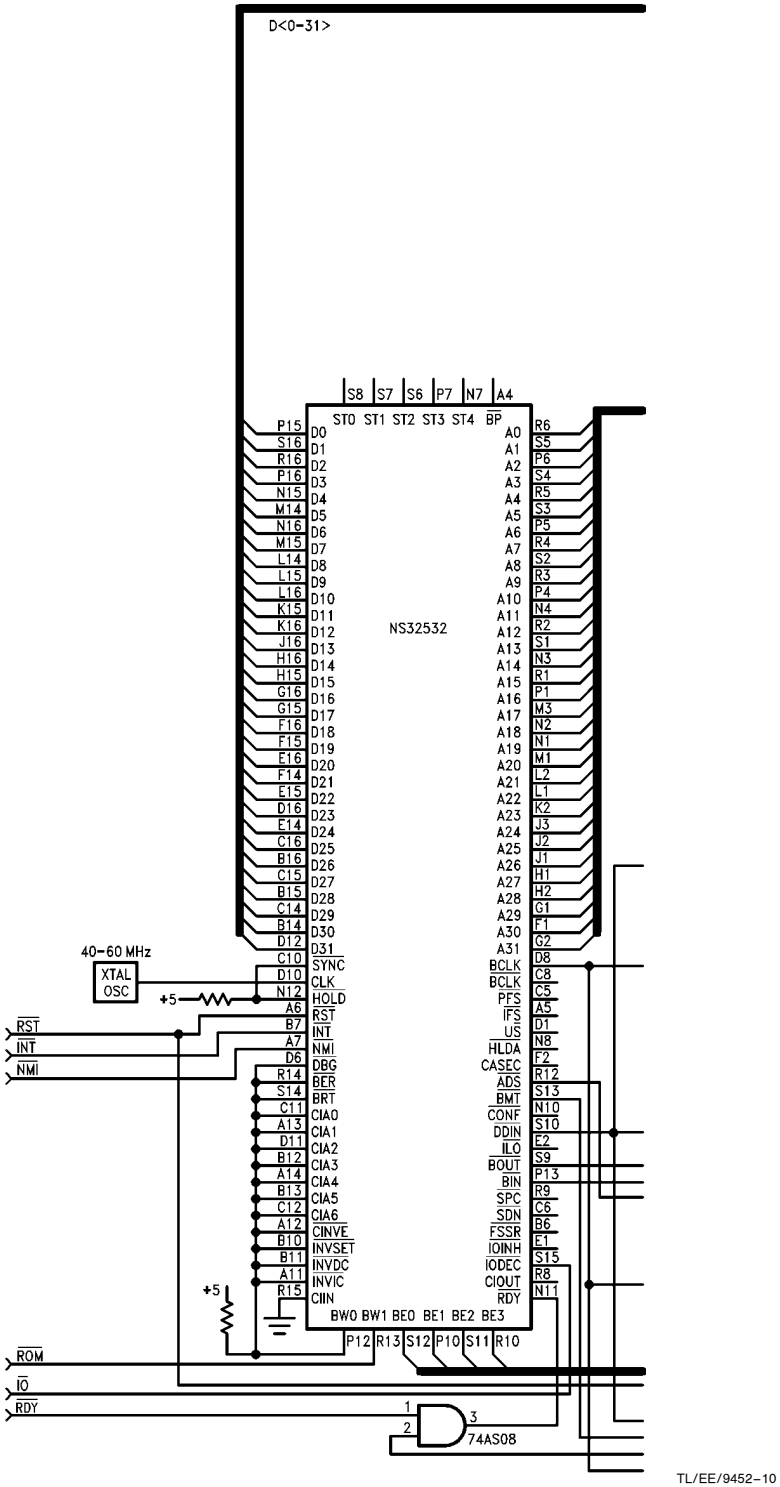
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NS32532
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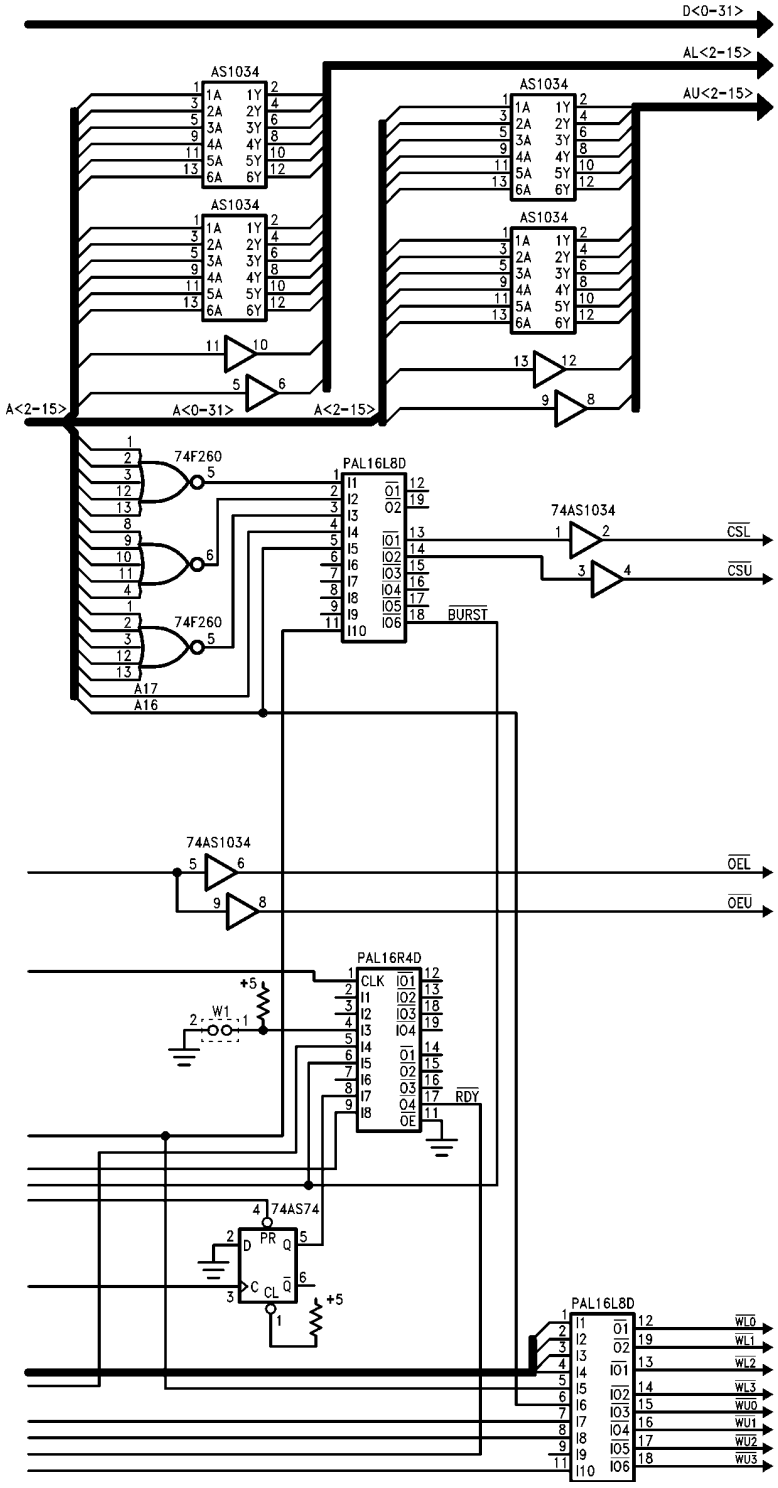
40-60 MHz
XTAL OSC
+5
+5
RST
INT
NMI
ROM
IO
RDY
74AS08
TL/EE/9452-10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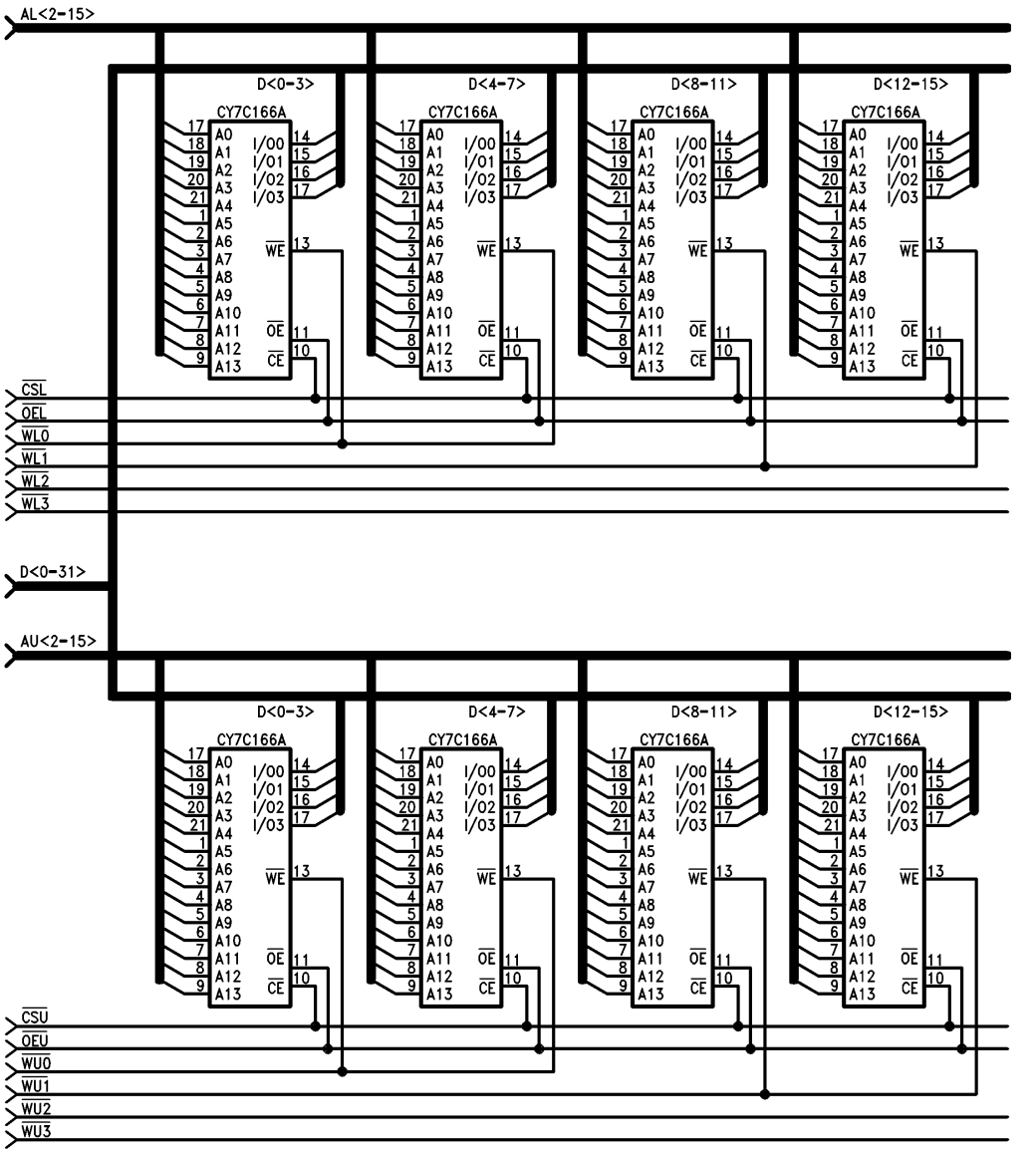
TL/EE/9452–11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WL2
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OEU
WU0
WU1
WU2
WU3

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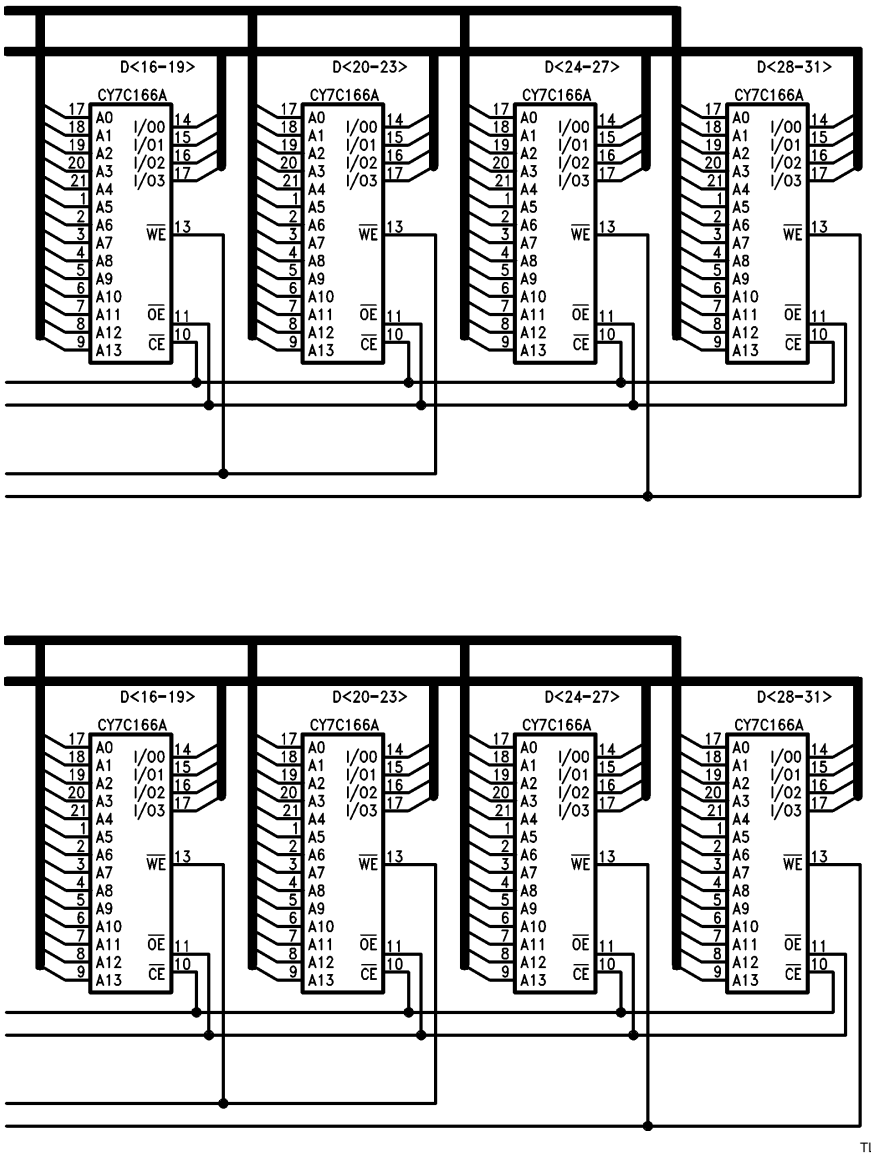
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A9
A10
A11
A12
A13
I/O0
I/O1
I/O2
I/O3
WE
OE
CE

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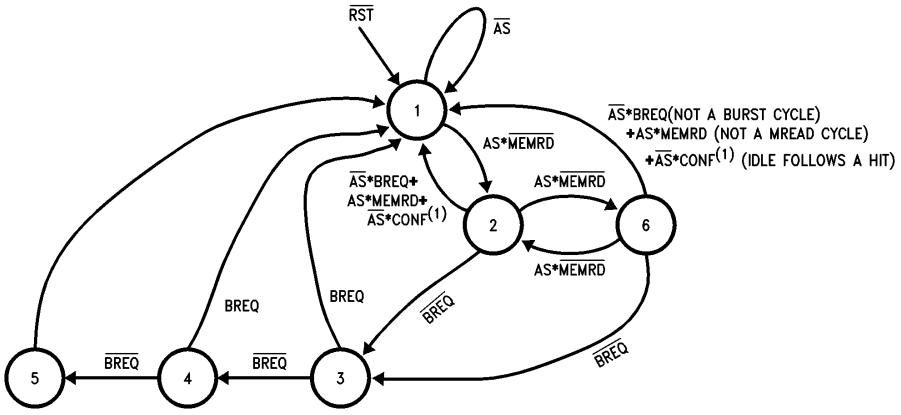
Appendix B

State Diagram of the Interleaved SRAM Interface



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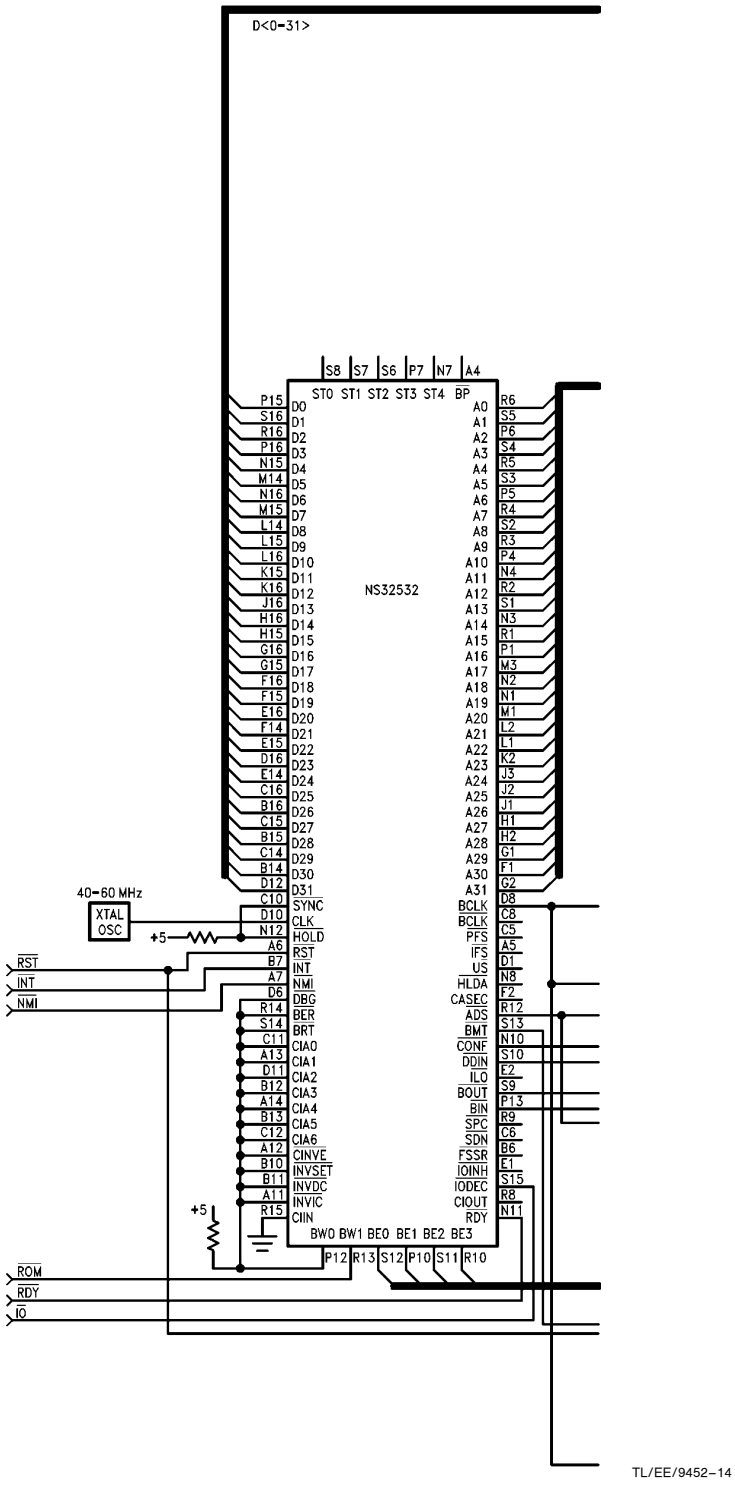
Note 1: This condition is a subset of /AS * BREQ condition.

```
PAL16R4D
STATE MACHINE PAL
STATE MACHINE ENCODING TO CONTROL SRAM BANKS
NATIONAL SEMICONDUCTOR, SANTA CLARA, CALIFORNIA
CLK LA3 LA2 NC RST /MEMRD CONF AS BREQ GND
OE RA30 RA31 A B C D OE1 OE0 VCC
/A     := A * B * C * /D * AS */MEMRD * RST + A * B * /C * D * /BREQ * RST
/B     := B * C * /D * RST
/C     := A * /B * C * D * /BREQ * RST
/D     := A * B * C * AS * /MEMRD * RST + B * C * /D * AS * /MEMRD * RST
/OE0   := B * C * /D * /LA2 * /CONF * RST + A * B * /C * D * /LA2 * RST + A * /B * C * D * LA2 * RST
          + /A * B * C * D * LA2 * RST
/OE1   := A * /B * C * D * /LA2 * RST + /A * B * C * D * /LA2 * RST + B * C * /D * LA2 * /CONF * RST
          + A * B * /C * D * LA2 * RST
/RA30  := /LA3 * LA2 * A * B * /C * D * RST + LA3 * /LA2 * A * /B * C * D * RST
          + LA3 * LA2 * B * C * /D * RST
/RA31  := /LA3 * /LA2 * A * B * /C * D * RST + LA3 * LA2 * A+ /B * C * D * RST

PAL16L8D
ADDENDUM TO STATE MACHINE
NATIONAL SEMICONDUCTOR, SANTA CLARA, CALIFORNIA
LA2 LA3 NC NC NC A B C D GND
RST SA30 NC NC NC NC NC SA31 VCC
/SA30  = /LA3 * /LA2 * A * /B * C * D * RST + /LA3 * LA2 * B * C * /D * RST
         + LA3 * LA2 * A * B * /C * D * RST
/SA31  = /LA3 * /LA2 * A * B * /C * D * RST + /LA3 * LA2 * A * /B * C * D * RST

PAL16L8D
WRITE STROBE PAL
WRITE STROBE GENERATOR FOR SRAM BANKS
NATIONAL SEMICONDUCTOR, SANTA CLARA, CALIFORNIA
BE0 BE1 BE2 BE3 BDDIN LA2 CONF BMT EBMT GND
BCLK WL0 WL2 WL3 WU0 WU1 WU2 WU3 WL1 VCC
/WL0  = /BMT * BDDIN * /BE0 * /LA2 * + EMBT * /CONF * BDDIN * /BE0 * /LA2
        + BCLK * /CONF * BDDIN * /BE0 * /LA2
/WL1  = /BMT * BDDIN * /BE1 * /LA2 + EBMT * /CONF * BDDIN * /BE1 * /LA2
        + BCLK * /CONF * BDDIN * /BE1 * /LA2
/WL2  = /BMT * BDDIN * /BE2 * /LA2 + EBMT * /CONF * BDDIN * /BE2 * /LA2
        + BCLK * /CONF * BDDIN * /BE2 * /LA2
/WL3  = /BMT * BDDIN * /BE3 * /LA2 + EBMT * /CONF * BDDIN * /BE3 * /LA2
        + BCLK * /CONF * BDDIN * /BE3 * /LA2
/WU0  = /BMT * BDDIN * /BE0 * LA2 + EBMT * /CONF * BDDIN * /BE0 * LA2
        + BCLK * /CONF * BDDIN * /BE0 * LA2
/WU1  = /BMT * BDDIN * /BE1 * LA2 + EBMT * /CONF * BDDIN * /BE1 * LA2
        + BCLK * /CONF * BDDIN * /BE1 * LA2
/WU2  = /BMT * BDDIN * /BE2 * LA2 + EBMT * /CONF * BDDIN * /BE2 * LA2
        + BCLK * /CONF * BDDIN * /BE2 * LA2
/WU3  = /BMT * BDDIN * /BE3 * LA2 + EBMT * /CONF * BDDIN * /BE3 * LA2
        + BCLK * /CONF * BDDIN * /BE3 * LA2

PAL16L8D
ADDRESS DECODE PAL
ADDRESS DECODE PAL
NATIONAL SEMICONDUCTOR, SANTA CLARA, CALIFORNIA
F1 F2 F3 A17 NC NC NC NC NC GND
BDDIN NC CS NC NC NC NC MEMRD NC VCC
/CS      = F1 * F2 * F3 * /A17
/MEMRD   = F1 * F2 * F3 * /BDDIN
```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NS32532
BW0 BW1 BE0 BE1 BE2 BE3
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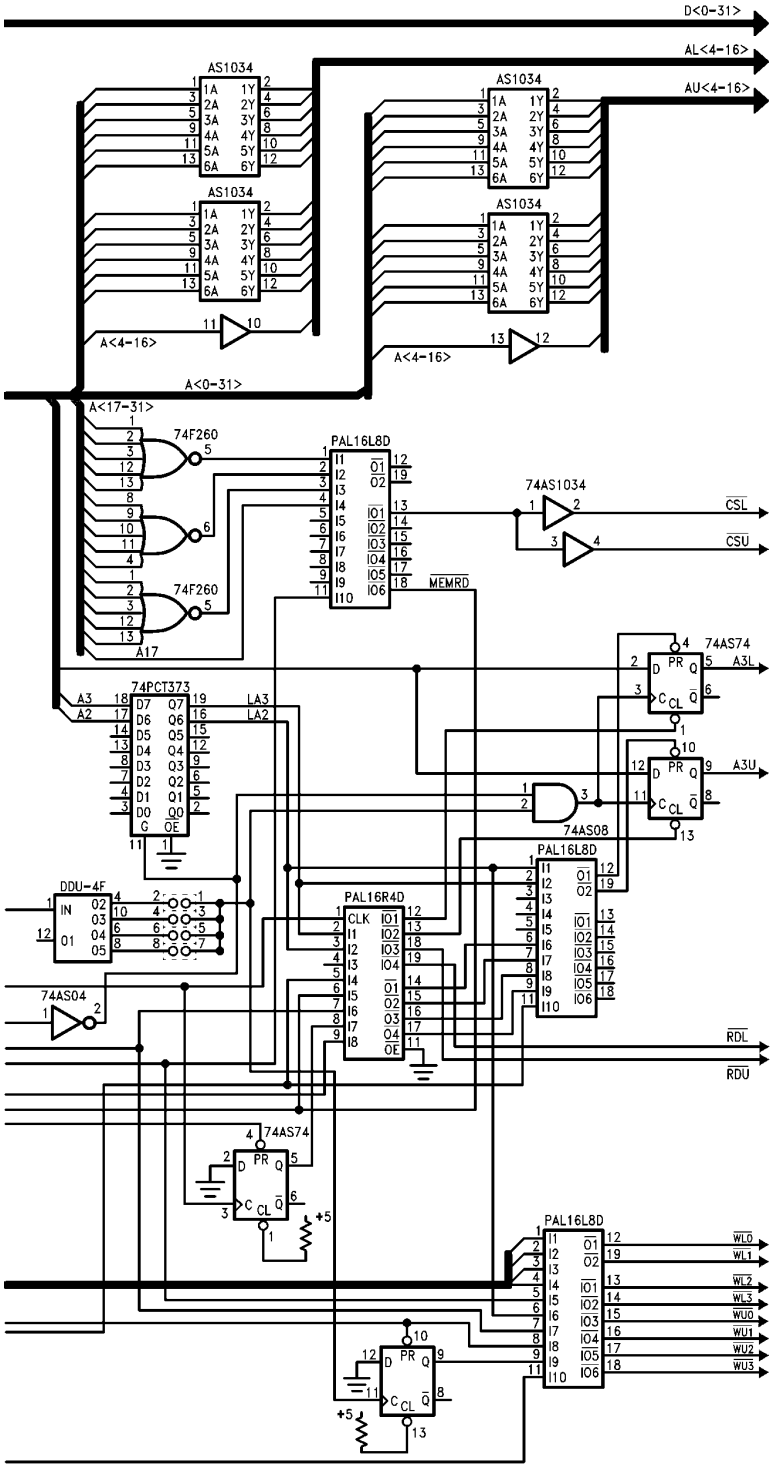
XTAL
OSC
+5
RST
INT
NMI
ROM
RDY
IO
TL/EE/9452-14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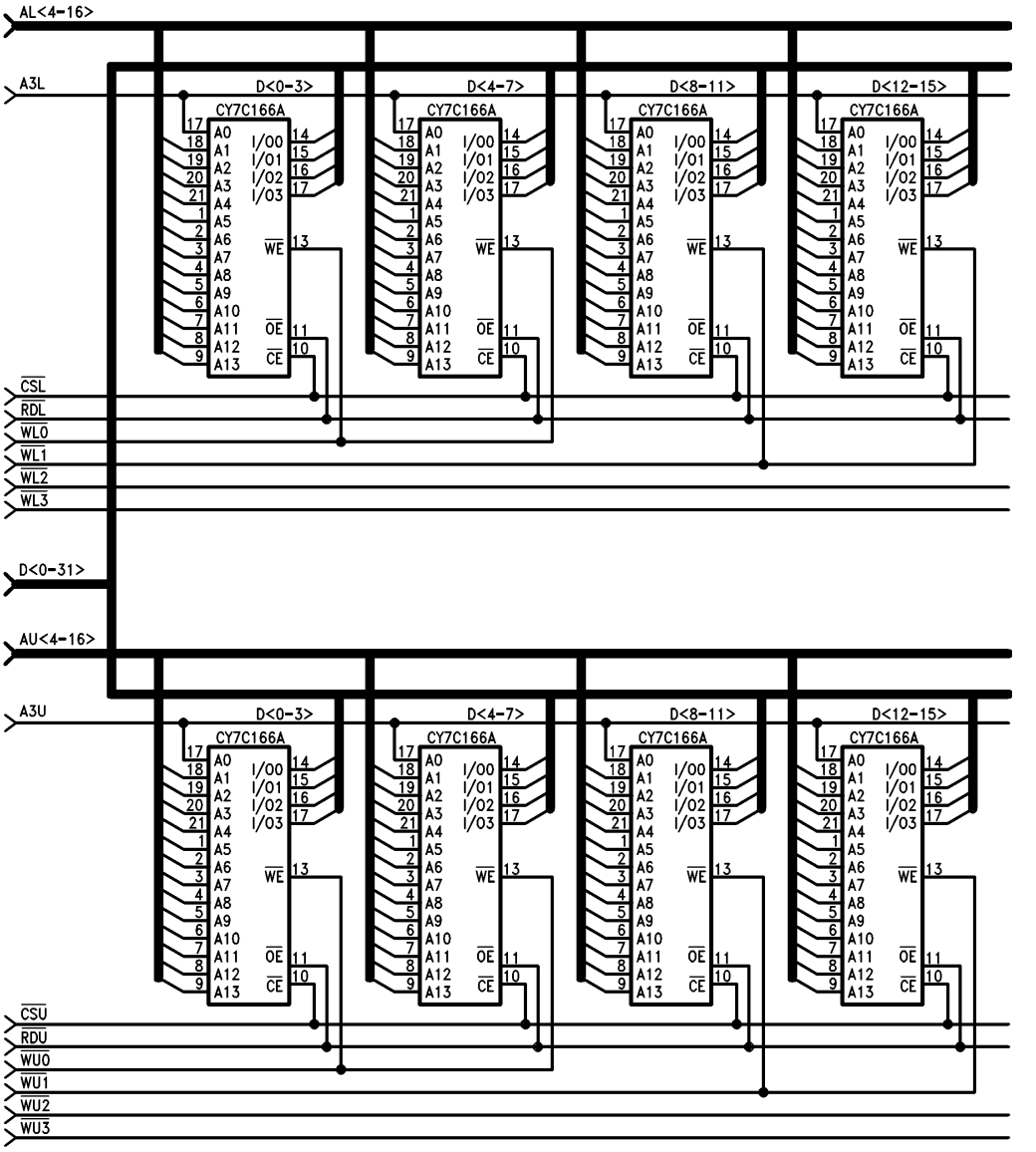
PAL16L8D
74AS1034
CSL
CSU
MEMRD
A17
74AS74
A3L
A3U
74PCT373
A3
A2
LA3
LA2
74AS08
DDU-4F
PAL16R4D
74AS04
RDL
RDU
+5
WL0
WL1
WL2
WL3
WU0
WU1
WU2
WU3

TL/EE/9452–15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WL0
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WL2
WL3
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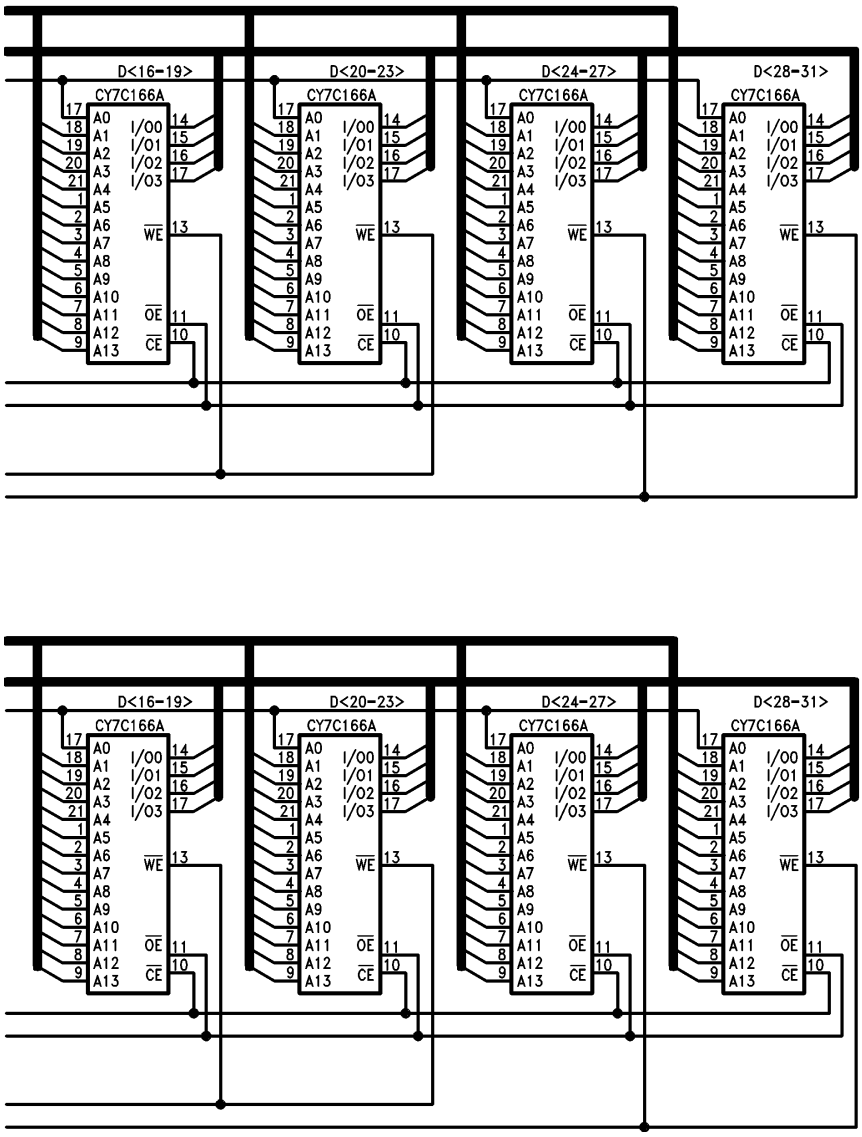
CSU
RDU
WU0
WU1
WU2
WU3

TL/EE/9452–16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D<20-23>
D<24-27>
D<28-31>
CY7C166A
A0
A1
A2
A3
A4
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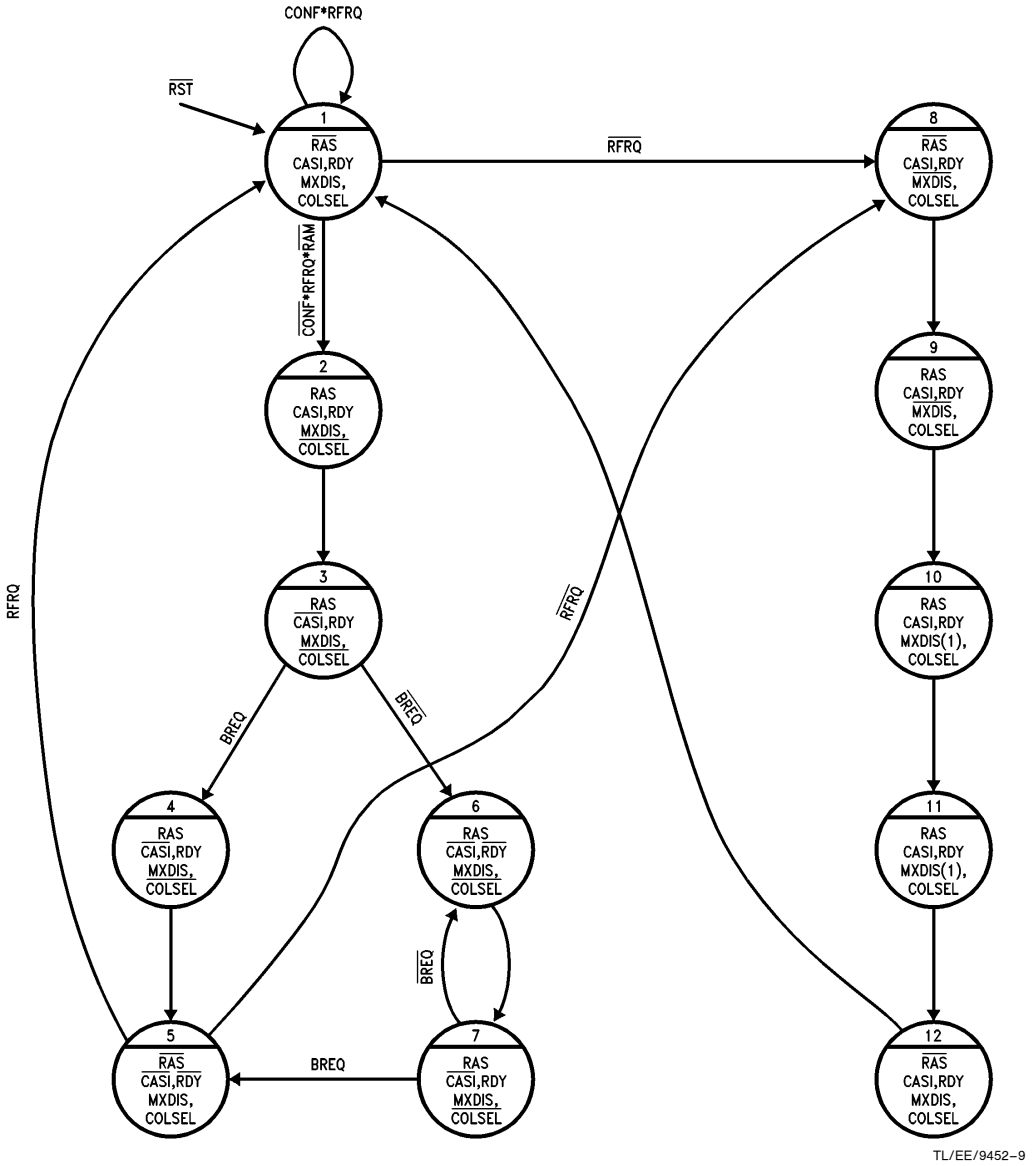
A6
A7
A8
A9
A10
A11
A12
A13
I/O0
I/O1
I/O2
I/O3
WE
OE
CE

TL/EE/9452–17

Appendix C

State Diagram of the Simple DRAM Interface



TL/EE/9452–9

Note 1: MXDIS and COLSEL are Don't Care in these states.

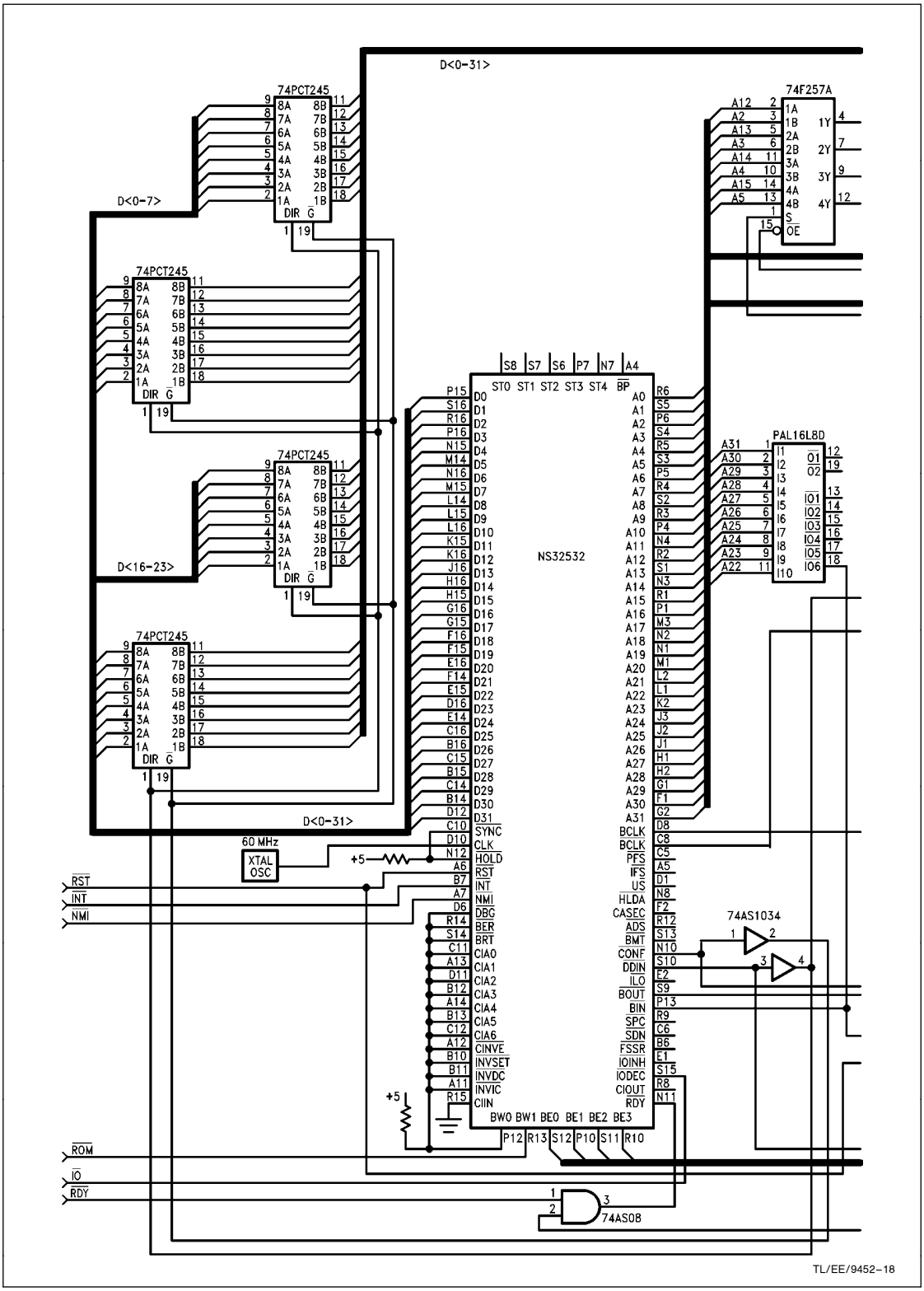
```
PAL16R8D
STATE MACHINE PAL
STATE MACHINE FOR DRAM CONTROLLER
NATIONAL SEMICONDUCTOR, SANTA CLARA, CALIFORNIA
CLK RFRQ CONF BREQ RAM NC IRST NC NC GND
OE A B NC C D E F G VCC
/A  :=  A * B * /C * D * E * F * G * /RFRQ + A * B * /C * D * E * /F * /G * /RFRQ
        + /A * B * /C * D * E * F * G + /A * B * C * /D * E * F * G
/B  :=  A * B * /C * D * E * F * G * /CONF * RFRQ * /RAM + A * /B * C * /D * E * /F * G * BREQ
        + A * /B * C * D * E * F * G + A * /B * C * D * E * /F * /G + A * /B * C * /D * /F * G * /BREQ
/C  :=  A * B * /C * D * E * /F * /G * RFRQ + A * B * /C * D * E * F * G * CONF * RFRQ + /RST
        + A * B * /D * E * F * G + A * /B * C * D * /E * /F * G + A * /B * C * /D * /E * /F * G * BREQ
        + A * B * /C * D * E * F * G * /RFRQ + A * B * /C * D * E * /F * /G * /RFRQ
/D  :=  A * /B * C * D * E * F * G + A * /B * C * D * E * /F * /G + /A * B * /C * D * E * F * G
        + /A * B * C * D * /E * F * G + A * B * C * /D * E * F * G
/E  :=  A * /B * C * /D * E * /F * G * BREQ + A * /B * C * D * E * /F * /G + /A * B * C * /D * E * F * G
/F  :=  A * /B * C * D * E * F * G + A * /B * C * /E * /F * G + A * /B * C * D * E * /F * /G
        + A * /B * C * /D * /F * G
/G  :=  A * /B * C * /E * /F * G + A * /B * C * /D * /F * G * /BREQ


PAL16L8D
/CASn PAL
GENERATES /CASn FOR DRAM BANKS
NATIONAL SEMICONDUCTOR, SANTA CLARA, CALIFORNIA
NC CASI DDIN NC BE0 BE1 BE2 BE3 NC GND
NC NC CAS0 CAS1 CAS2 CAS3 NC NC NC VCC
/CAS0  =  /CASI * /DDIN + /CASI * /BE0 * DDIN
/CAS1  =  /CASI * /DDIN + /CASI * /BE1 * DDIN
/CAS2  =  /CASI * /DDIN + /CASI * /BE2 * DDIN
/CAS3  =  /CASI * /DDIN + /CASI * /BE3 * DDIN


PAL16L8D
ADDRESS DECODE PAL
ADDRESS DECODER FOR DRAM INTERFACE
NATIONAL SEMICONDUCTOR, SANTA CLARA, CALIFORNIA
A31 A30 A29 A28 A27 A26 A25 A24 A23 GND
A22 RAM RAML RAMU NC NC NC NC NC VCC
/RAM   =  /A31 * /A30 * /A29 * /A28 * /A27 * /A26 * /A25 * /A24 * /A23
/RAML  =  /A31 * /A30 * /A29 * /A28 * /A27 * /A26 * /A25 * /A24 * /A23 * /A22
/RAMU  =  /A31 * /A30 * /A29 * /A28 * /A27 * /A26 * /A25 * /A24 * /A23 * /A22
```

```
PAL20X10A
REFRESH INTERVAL COUNTER
30 MHZ REFRESH INTERVAL COUNTER PAL
NATIONAL SEMICONDUCTOR, SANTA CLARA, CALIFORNIA
BCLK NC NC NC NC NC NC NC NC RFACK GND
OE Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 NC RFRQ VCC
/Q0     :=  /Q0 + /Q7 * /Q6 * /Q5
            :+: VCC
/Q1     :=  /Q1 + /Q7 * /Q6 * /Q5
            :+: /Q7 * /Q6 * /Q5 + /Q0
/Q2     :=  /Q2 + /Q7 * /Q6 * /Q5
            :+: /Q7 * /Q6 * /Q5 + /Q1 + /Q0
/Q3     :=  /Q3 + /Q7 * /Q6 * /Q5
            :+: /Q7 * /Q6 * /Q5 + /Q2 * /Q1 * /Q0
/Q4     :=  /Q4 + /Q7 * /Q6 * /Q5
            :+: /Q7 * /Q6 * /Q5 + /Q3 * /Q2 * /Q1 * /Q0
/Q5     :=  /Q5 + /Q7 * /Q6 * /Q5
            :+: /Q7 * /Q6 * /Q5 + /Q4 * /Q3 * /Q2 * /Q1 * /Q0
/Q6     :=  /Q6 + /Q7 * /Q6 * /Q5
            :+: /Q7 * /Q6 * /Q5 + /Q5 * /Q4 * /Q3 * /Q2 * /Q1 * /Q0
/Q7     :=  /Q7 + /Q7 * /Q6 * /Q5
            :+: /Q7 * /Q6 * /Q5 + /Q6 * /Q5 * /Q4 * /Q3 * /Q2 * /Q1 * /Q0
/RFRQ   :=  RFRQ * Q7 * Q6 * Q5 * Q4 * Q3 * Q2 * Q1 * Q0 + /RFRQ * /RFACK
            :+: /RFRQ

PAL20X10A
REFRESH ADDRESS COUNTER
REFRESH ADDRESS GENERATOR FOR DRAM BANKS
NATIONAL SEMICONDUCTOR, SANTA CLARA, CALIFORNIA
CLK NC NC NC NC NC NC NC NC NC GND
OE A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 VCC
/A0  :=  /A0  :+:  VCC
/A1  :=  /A1  :+:  A0
/A2  :=  /A2  :+:  A1 * A0
/A3  :=  /A3  :+:  A2 * A1 * A0
/A4  :=  /A4  :+:  A3 * A2 * A1 * A0
/A5  :=  /A5  :+:  A4 * A3 * A2 * A1 * A0
/A6  :=  /A6  :+:  A5 * A4 * A3 * A2 * A1 * A0
/A7  :=  /A7  :+:  A6 * A5 * A4 * A3 * A2 * A1 * A0
/A8  :=  /A8  :+:  A7 * A6 * A5 * A4 * A3 * A2 * A1 * A0
/A9  :=  /A9  :+:  A8 * A7 * A6 * A5 * A4 * A3 * A2 * A1 * A0
```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D<0-7>
74PCT245
74PCT245
D<16-23>
74PCT245
D<0-31>
74F257A
PAL16L8D
NS32532
ST0 ST1 ST2 ST3 ST4 BP
S8 S7 S6 P7 N7 A4
BW0 BW1 BE0 BE1 BE2 BE3
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XTAL OSC
+5
74AS1034
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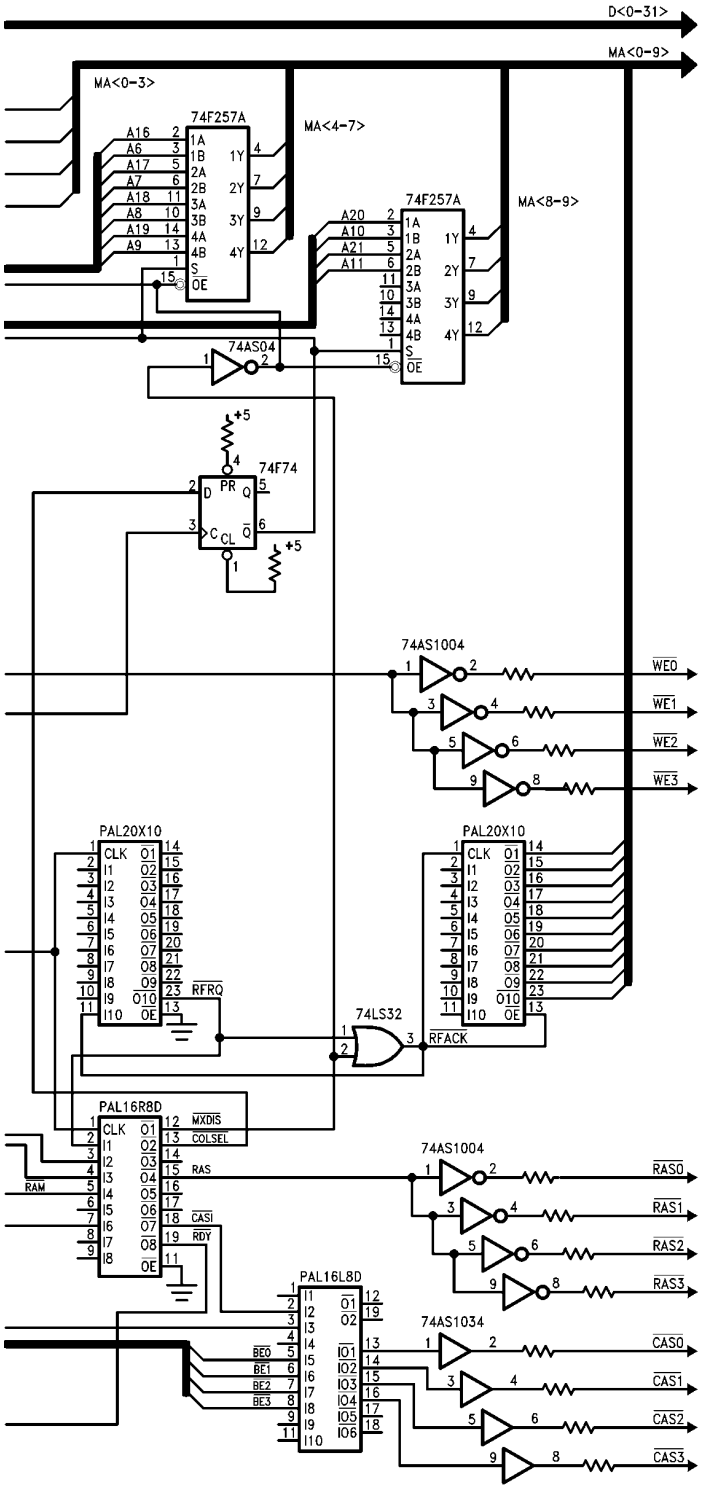
INT
NMI
ROM
IO
RDY
TL/EE/9452–18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MA<8-9>
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74F257A
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+5
74F74
74AS1004
74AS1004
74AS1034
WE0
WE1
WE2
WE3
RAS0
RAS1
RAS2
RAS3
CAS0
CAS1
CAS2
CAS3
PAL20X10
PAL20X10
PAL16R8D
PAL16L8D
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RFACK
MXDIS
COLSEL
RAS
CASI
RDY
RAM
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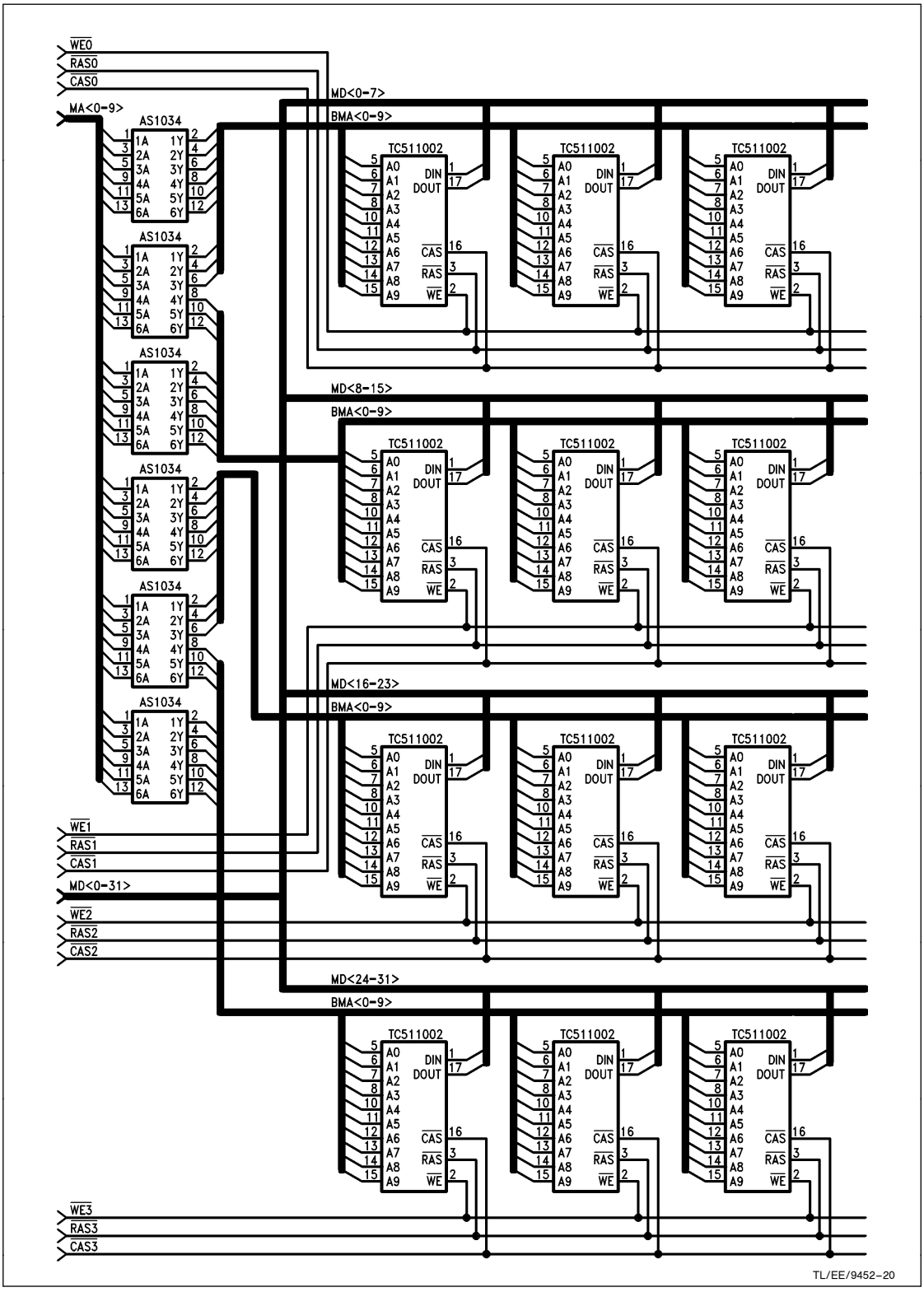
BE1
BE2
BE3
TL/EE/9452–19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TC511002
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DOUT
CAS
RAS
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BMA<0-9>
MD<16-23>
BMA<0-9>
WE1
RAS1
CAS1
MD<0-31>
WE2
RAS2
CAS2
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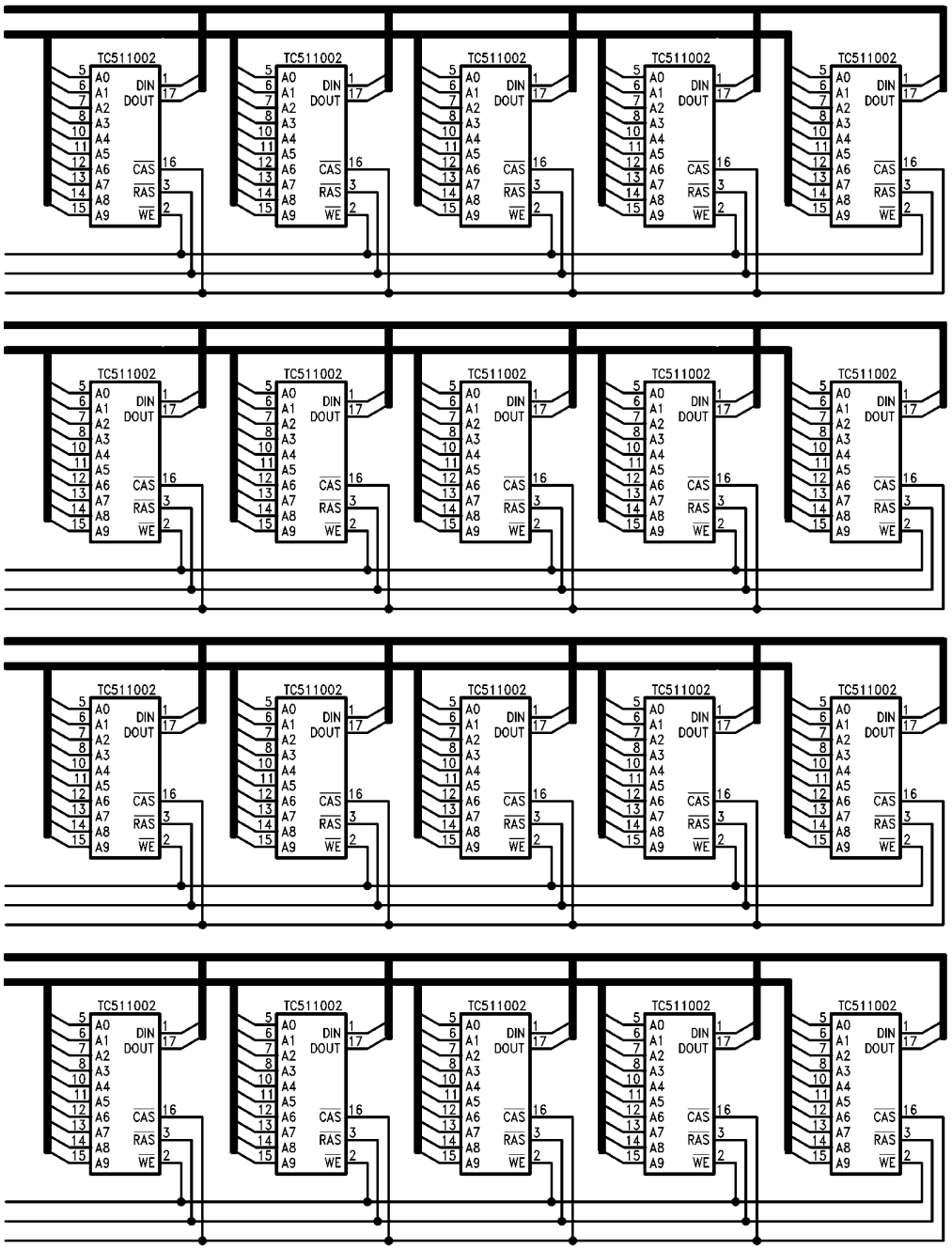
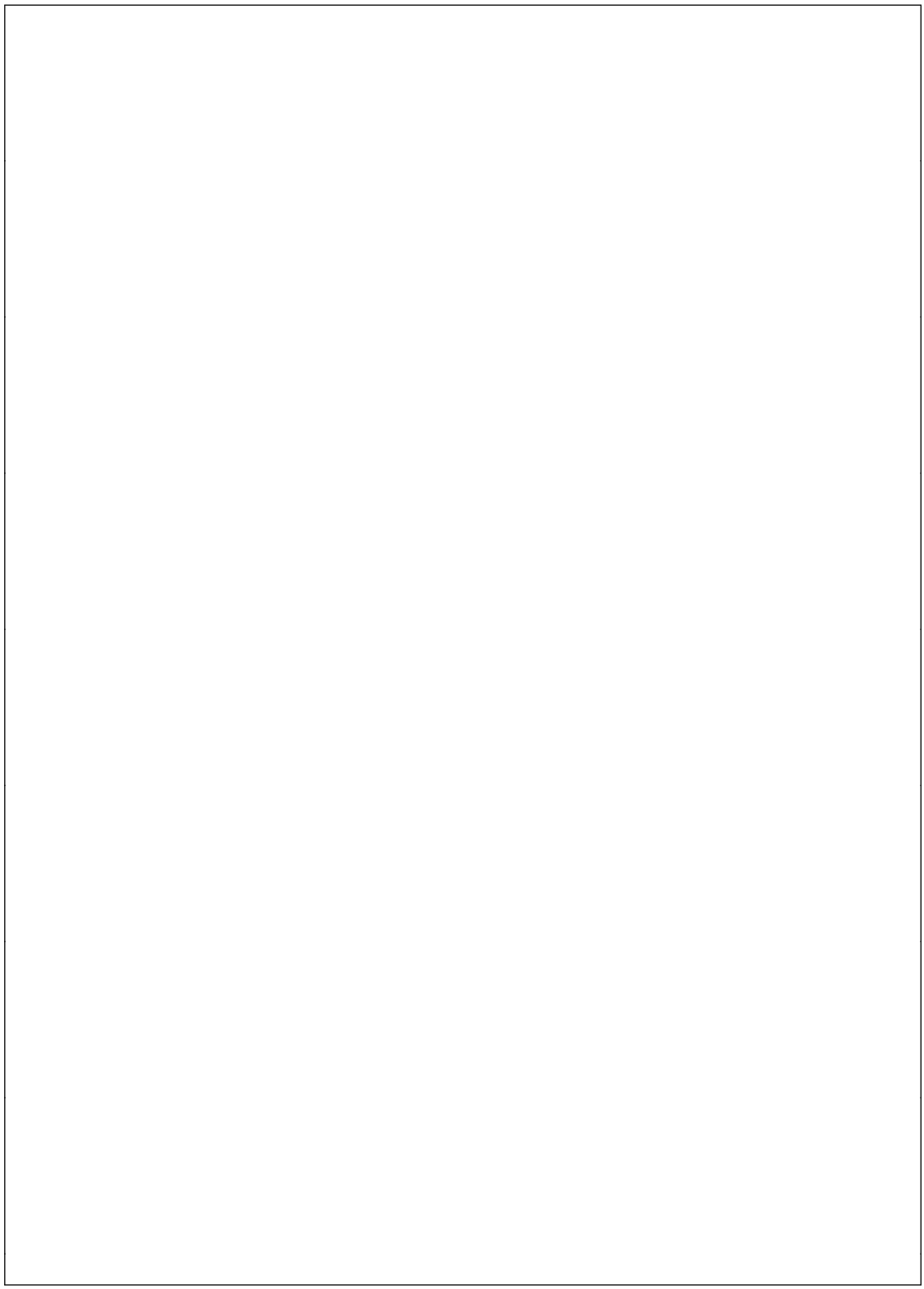
WE3
RAS3
CAS3

TL/EE/9452–20



TL/EE/9452–21



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