Improving The Performance Of A High Speed PBX Backplane

National Semiconductor
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ABSTRACT

This article will provide solutions to performance problems associated with PBX backplanes. Some of these problems are: long settling time, excessive propagation delay, low impedance bus lines, crosstalk, and electromagnetic radiation (EMR). These problems are caused by high output capacitance drivers that use TTL signal levels. National's solution to these problems is the Backplane Transceiver Logic (BTL) family of devices.

INTRODUCTION

To be able to meet the bandwidth and high system reliability requirements of the next generation PBXs, the industry must use parallel, high speed Pulse Code Modulation (PCM) highways. This article will deal with the following problems encountered by these high speed PCM highways.

- Crosstalk
- Power Consumption
- Noise Margin
- Bus Impedance
- Signal Settling Time
- Propagation Delays
- Propagation Delay Skew
- Live Insertion
- Extending A Bus Beyond The Rack
- Bus Termination
- Pin Layout

I. REDUCING CROSSTALK

Crosstalk can reduce the data integrity of the system or even cause a total shutdown. Crosstalk amplitude is proportional to the slew rate, signal swing, and physical layout of the board. To reduce crosstalk, the DS3890/92/98: shrink the standard TTL three volt swing to the Backplane Transceiver Logic (BTL) one volt swing; slow down the rise and fall time to 6 ns; use low pass filters and precision thresholds on the receivers.

II. REDUCING POWER CONSUMPTION

Because of excessive heat dissipation and a mandatory battery backup, power consumption must be kept to a minimum. Low impedance, open collector busses that use TTL signal levels need drivers capable of sinking approximately 300 mA. By using the BTL one volt signal swing, the drivers need only sink 50 mA. Refer to the section **Signal Settling Time** for more details. The reduction in power consumption will enable PBXs to coexist with other office equipment in ''normal'' office environments.

III. NOISE MARGIN

Noise margins protect the system from crosstalk, ground noise, and external EMR. The magnitude of the absolute noise margin is a good measure of how well protected the system is against external electro magnetic interference (EMI) and ground noise. The relative noise margin is a good measure as to how well protected the system is against crosstalk, assuming most signals within the system have the

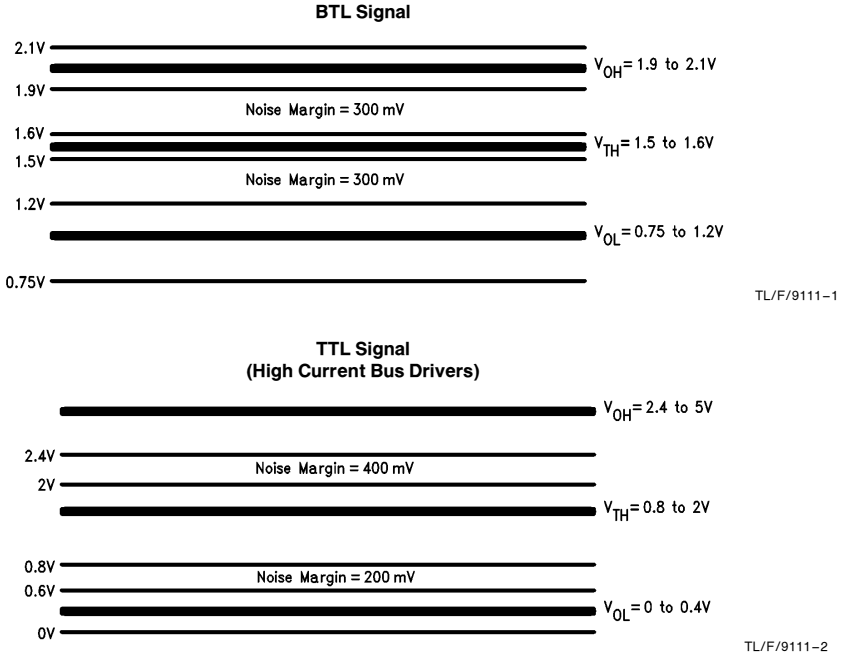

FIGURE 1

same voltage swing. As shown below, BTL signals improve both the absolute and relative noise margins

- Absolute Noise Margin

Despite the smaller signal swing, BTL signals have a 300 mV noise margin, as compared to the 200 or 400 mV guaranteed noise margin in TTL signals (see *Figure 1*). The absolute noise margin is usually not very critical since PBXs are usually well protected from external EMR by the metallic racks.

- Relative Noise Margin

Based on the data sheet guaranteed limits, BTL signals have a 30% [(300 mV absolute noise margin)/(1V signal swing)] relative noise margin, as compared to 7% [(200 mV absolute noise margin)/(3V swing)] in standard TTL signals.

IV. IMPROVING BUS IMPEDANCE

Standard TTL drivers do not have sufficient drive current to drive a heavily loaded backplane. A larger output transistor is needed to increase the drive current. The large TTL output transistor, however, increases the capacitance loading, which decreases the bus impedance, which in turn requires more drive current. The BTL drivers have a Schottky diode in series with the driver transistor's collector. When the driver transistor is off, the diode is reverse biased, which reduces the output capacitance to only 1–2 pF. As shown below, the reduced output capacitance greatly improves the overall bus impedance.

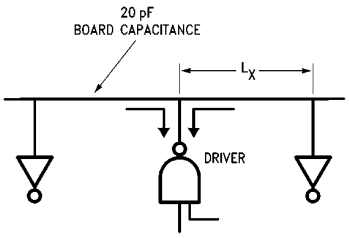

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FIGURE 2

L_X = Board Spacing = 0.6 in

L_{foot} = 20 loads per foot

$C_{x\text{-}TTL}$ = Capacitance per TTL Driver
= Transceiver Capacitance + PC Trace and Connector Capacitance
= 15 pF + 5 pF
= 20 pF per load

$C_{x\text{-}BTL}$ = Capacitance per BTL Driver
= Driver Capacitance + Receiver Capacitance + PC Trace and Connector Capacitance
= 2 pF + 2 pF + 1 pF + 5 pF
= 10 pF per load

$C_{L\text{-}TTL}$ = (20 load per foot) × (20 pF per load)
= 400 pF per Foot

$C_{L\text{-}BTL}$ = (20 load per foot) × (10 pF per load)
= 200 pF per Foot

- Unloaded Bus Impedance

L = Standard PC Board Inductance Per Foot
= 0.2 μH per foot

C = Standard PC Board Capacitance Per Foot
= 20 pF per foot

$Z_O = (L/C)^{1/2}$
$= (0.2\ \mu H/20\ pF)^{1/2} = 100\Omega$

- Loaded Bus Impedance (for a uniform capacitive loading C_X spaced at equal intervals)

$Z_L = Z_O/(1 + C_L/C)^{1/2}$

$Z_{L\text{-}TTL} = 100/(1 + 400/20)^{1/2} = 22\Omega$

$Z_{L\text{-}BTL} = 100/(1 + 200/20)^{1/2} = 30\Omega$

Note that each driver sees TWO loaded line impedances in parallel (see *Figure 2*). This reduces the bus impedance by half.

V. PROPAGATION DELAYS (related to excessive capacitance loading)

Since the DS3890 reduces the backplane capacitance loading, the propagation delay through the bus lines is improved by 28%, as shown below.

- Unloaded Bus Propagation Delay (data based on a single strip line PC board)

$T_P = (LC)^{1/2} = [(0.2\ \mu H/ft) \times (20\ pF/ft)]^{1/2}$
$= 2$ ns per foot

- Loaded Bus Propagation Delay (data based on a single strip line PC board)

$T_{PL} = (T_P) \times (1 + C_L/C)^{1/2}$

$T_{PL\text{-}TTL} = (2\ ns) \times [1 + (400\ pF\ per\ Foot)(20\ pF)]^{1/2}$
$= 9.2$ ns/ft

$T_{PL\text{-}BTL} = T_P \times (1 + C_L/C)^{1/2} = (2\ ns) \times [1 + (200\ pF\ per\ Foot)/(20\ pF)]^{1/2} = 6.6$ ns/ft

Improvement = (6.6 ns per foot)/(9.2 ns per foot) × (100)
= 28%

VI. SIGNAL SETTLING TIME

The signal settling time refers to the amount of time the signal takes to cross the threshold. In low impedance busses, the signaling settling time depends NOT ONLY on the slew rate, but more importantly, on the current driving capability of the driver, bus impedance, reflections, and bus length.

For example, in a fully loaded open collector TTL bus ($Z_{O\text{-}TTL} = 22\Omega$) with 50 mA drivers, the first output transition is [$V_1 = (I_L) \times (Z_O \| Z_O) = (50\ mA) \times (11\Omega)$] 0.55V. This means that the signal does NOT cross the threshold region (V_{TH} = 0.8 to 2V) on the first signal transition (see *Figure 3*). The second transition appears after a round trip prop delay [R.T.D. = (2) × ($T_{L\text{-}TTL}$)]. In a one foot fully loaded bus, the delay can be 18.4 ns [R.T.D. = (2) × (9.2 ns per foot)]. If it takes several signal transitions to cross the threshold, the ACTUAL signal settling time consists of several round trip prop delays. Also note that the signal crosses the threshold in a staircase fashion, which may cause false triggering.

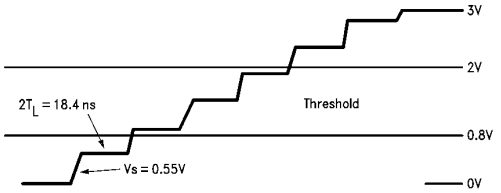

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FIGURE 3

$V_{I\text{-}TTL}$ = (50 mA) × (11Ω) = 0.55V

Round Trip Prop Delay of the Bus = (2) × ($T_{L\text{-}TTL}$)

= (2) × (2 ns per foot)

= 4 ns/ft (unloaded bus)

= (2) × (9.2 ns per foot)

= 18.4 ns/ft (loaded bus)

In a fully loaded BTL bus ($Z_{O\text{-}BTL}$ = 30Ω), the first output transition is 0.75V [V1 = (50 mA) × (15Ω)]. Since V_{TH} is between 1.5V and 1.6V, the FIRST output transition crosses the threshold (see *Figure 4*). The actual settling time consists of ONLY the slew rate. The danger of false triggering is eliminated because the reflections are not seen as the signal crosses the threshold.

$V_{I\text{-}BTL}$ = (50 mA)* (15Ω) = 0.75V

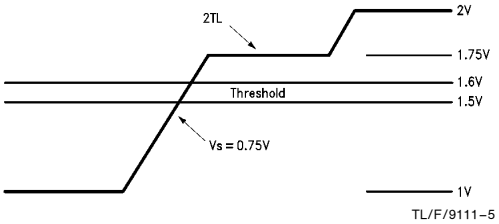

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FIGURE 4

Therefore, despite the slower slew rate, the BTL devices have a much shorter settling time due to the lower output capacitance, one volt signal swing, and precision threshold. This improves the data integrity and speed of the bus.

VII. PROPAGATION DELAY SKEW

The propagation delay consists of the delays through the driver, receiver, and transmission medium (PC strip). These delays can vary if the ICs have differences in their process, temperature, V_{CC}, or PC board layout. In parallel address/data lines, propagation delay skews are very critical. If the signals arrive at their destination at different times, the system must delay all signals to assume for a worst case delay. Therefore, if the propagation delay skew is small, the worst case delay is also small. It is safe to assume that ICs on a single board or system have the same temperature, same V_{CC}, and similar PC board layout configurations. This reduces the propagation delay skew to only the variations in the process.

VIII. LIVE INSERTION GUIDELINES

Live insertion of line cards is a must for PBX maintenance without interrupting customer service. The DS3890/92/98 support live insertion by guaranteeing glitch-free power up/down. However, uncharged by-pass capacitors and board static can bring the system down when plugging in a line card. One way of avoiding these problems is to use an umbilical cord (temporary power line) to discharge static and slowly charge by-pass capacitors. This method will set the line card V_{CC} and GND equal to the levels of the system before it is plugged in.

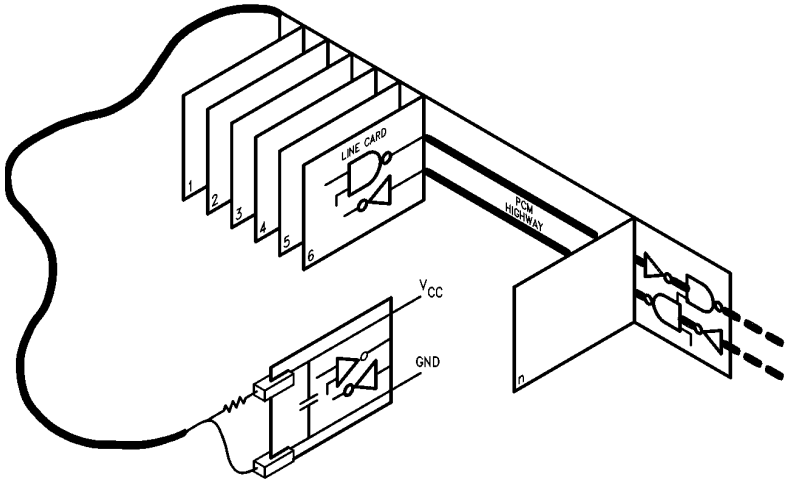

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FIGURE 5. Temporary Power Cord

IX. EXTENDING A BUS BEYOND THE RACK

The DS3898 (BTL repeater) is ideal for cases where the system bus must be extended. If the bus is of considerable length, the repeaters regenerate the signal levels. The repeaters also isolate, or separate, different electrical environments. For example, if a ribbon cable is used to connect one rack to another, the repeaters will isolate the different impedance and noise levels present in a ribbon cable from the bus on the rack.

X. USING THE PROPER BUS TERMINATION

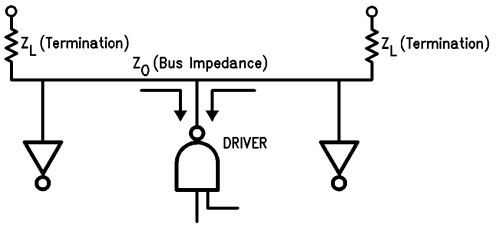

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FIGURE 6

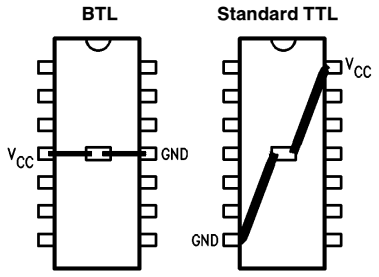
An ideal termination (Z_L) should match the bus impedance (Z_O) in order to eliminate reflections. If the termination matches the impedance of a fully loaded bus, then $Z_L = Z_O = 30\Omega$. With the 30Ω terminations, the driver is required to drive a ($Z_L \| Z_L = 30 \| 30$) 15Ω load. However, the lowest load that a standard TTL driver will guarantee is (5V/50 mA) 100Ω. If the designer uses the ($Z_L \| Z_L = 200 \| 200 = 100\Omega$ load) 200Ω terminations on the 30Ω bus, the reflections will be very large. On the other hand, BTL drivers can guarantee a (1V/50 mA) 20Ω load. In this case, the ($Z_L \| Z_L = 40 \| 40 = 20\Omega$ load) 40Ω terminations will have small reflections. Note that the improvement of the guaranteed load (from 100Ω to 20Ω) was achieved by reducing the voltage swing and driver output capacitance, NOT by increasing the current capabilities of the drivers.

XI. TWO VOLT RAIL

There are many ways of supplying the two volt rail needed for the 90/92/98. Four possibilities are: a separate two volt power supply; a voltage divider; a voltage regulator; and a high current voltage follower. The two volt power supply is very expensive to implement and does not track the five volt supply voltage, thereby reducing the effectiveness of the precision threshold. However, it is very efficient in terms of power consumption, making it appropriate for very large systems. The voltage divider is inexpensive, tracks the five volt supply voltage, but consumes too much current when the line is high. The voltage regulator is moderately efficient with current consumption, but does not track the five volt supply voltage. Finally, the high current voltage follower does not waste current when the line is high; is inexpensive to implement; and tracks the five volt supply voltage. Therefore, the high current voltage follower seems to be the best choice for small systems where cost is a major consideration.

XII. NOISE REDUCTION THROUGH IMPROVED PIN LAYOUT

In order to reduce ground noise caused by long lead inductance, one must make V_{CC} and GND lead lengths as short as possible. The packaging of National's BTL circuits contributes to shorter V_{CC} and GND lead inductance by placing the power pins in the center of the IC package, instead of the corners.



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Top View

FIGURE 7

XIII. OVERVIEW OF THE BTL TRAPEZOIDAL PRODUCT LINE

The BTL Trapezoidal products have low output capacitance (5 pF max), one volt signal swing, and noise immunity features which make them ideal for driving parallel, low impedance bus lines with minimum power dissipation.

- DS3890

The DS3890 is an octal BTL driver. It is designed specifically to overcome problems associated with driving densely populated backplanes. The trapezoidal wave forms and the one volt swing reduces noise coupling to adjacent lines. The open collector driver output allows for wired-OR connections.

- DS3892

The DS3892 is an octal receiver. The receivers have precision thresholds to increase the noise margins, and low pass filters to filter out crosstalk.

- DS3898

The DS3898 is an octal repeater. It combines the BTL characteristics of the DS3890 and DS3892. The part is ideal for extending backplanes.

- DS3896

The DS3896 is an octal high speed schottky bus transceiver with common control signals. It provides high package density for data/address lines.

- DS3897

The DS3897 is a quad transceiver with independent driver input and receiver output pins. It has a separate driver disable for each driver.

- DS3893

The DS3893 is the newest member of the family. It is designed to drive and receive signals at data rates of up to 100 MBaud. The trapezoidal feature has been removed to reduce the propagation delay down to 15 ns for the driver and receiver combination.

National's BTL drivers, receivers, and transceivers offer the most complete approach for operating high speed parallel backplanes.

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