An Easy/Low Cost Serial EEPROM Interface

National Semiconductor
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INTRODUCTION

Designers have resisted using a low cost serial EEPROM because of the uncommon interface required. The added components and circuitry have caused many engineers to resort to a larger parallel EEPROM, even when only a few bytes of non-volatile memory were required.

National Semiconductor has a design that is low in support components and takes advantage of a UART with a 1× external clock. This circuit is useful for DIP switch replacement as well as for a permanent record of the UART's communications activity. It can also be used as a security lock. Ease of interface offers the engineer a low cost solution.

THEORY OF OPERATION

Ordinarily small EEPROMs have been used to replace the DIP switch commonly found in microprocessor circuits. Just as common in such designs are UARTs, and the given application takes advantage of this for ease of interface. Because address decoding and microprocessor bus interfacing have already been accomplished, the UART is an ideal support interface for a serial EEPROM. The only true requirements for a serial EEPROM are the serial data path, clock timing, and chip select signal. All of these signals are derived from a UART in this application.

The Data In for the EEPROM is the transmitted data of the UART. Data Out of the EEPROM is directed to the receive data line of the UART. The chip select required by the EEPROM is a modem control line whose level is used to select either the modem device or the EEPROM. Finally, the serial clock required by the EEPROM can be a 1× clock provided by the UART.

THE WRITE CYCLE

When a write cycle is desired, the UART must be set up for an external 1× clock, 8 data bits, 1 stop bit, no parity and RTS must be programmed for a high output prior to data transmissions. It is also necessary to insure that the transmit buffer has been completely emptied of all prior bytes.

Before data can be written, an erase cycle to the desired address must first take place. This can be accomplished by loading the UART transmit register with an A0, A1, A2, A3, XX11 (e.g., an 03_H would result in location 0 being erased). After the transmit shift register has emptied, RTS should be returned to a low state and an erase/write programming time of 30 ms must elapse.

To write data requires that an address-op byte and two data bytes be loaded in the transmit holding register as soon as the holding register becomes empty. Table I shows the relationship of bits as they travel from the micro to the UART and finally to the EEPROM. The MSB 4 bits of the last byte written will not be saved by the EEPROM due to the 16-bit storage ability of the part. As the UART inserts start and stop bits, a total of 4 bits is saved in the EEPROM that are not usable by the microprocessor but are required by the UART.

THE READ CYCLE

As was true for the write cycle, the UART must be set up for 8 data bits, 1 stop bit, and an external 1× clock. To start the read cycle, a byte with read op and address must be written to the UART. An example of read location 0 would be 01_H. After the transmit shift register has emptied, the receiver shift register will begin to accumulate the data that was written and two reads will be required before the operation can be considered complete.

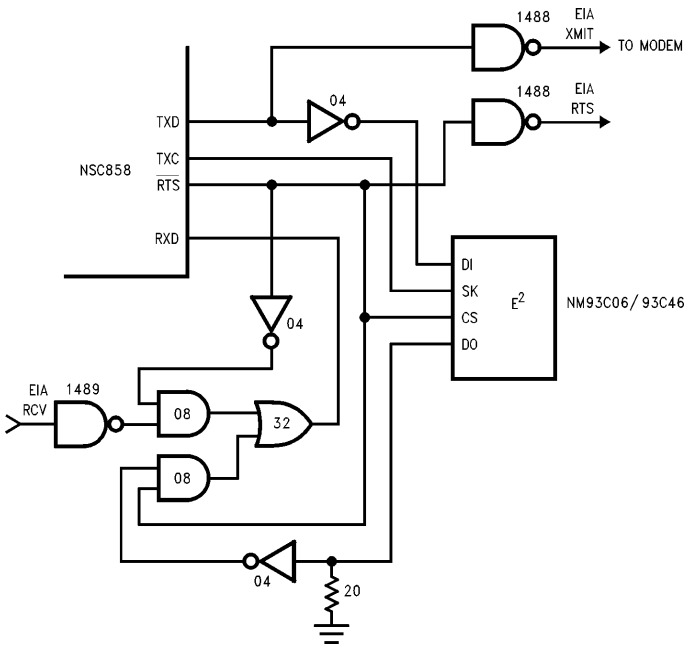
CONCLUSION

For a further understanding of this interface, refer to the NM93C06/93C46 and the NSC858 data sheets. Parity could be added for data integrity with further sacrifice of usable data bits in the EEPROM and the possibility of the second byte read being in parity error.

 TL/D/8642

RRD-B30M105/Printed in U. S. A.

UART/EEPROM Interface



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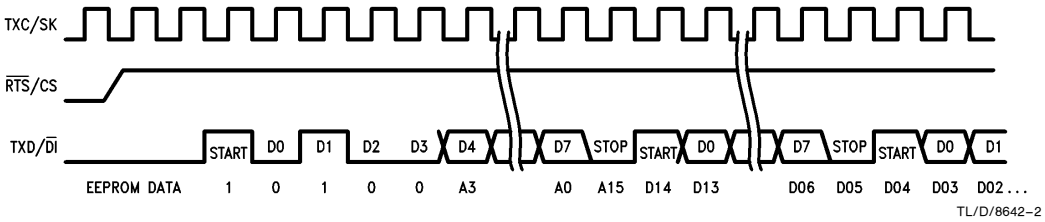
UART/EEPROM Timing

Write Cycle (93C06)



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Read Cycle

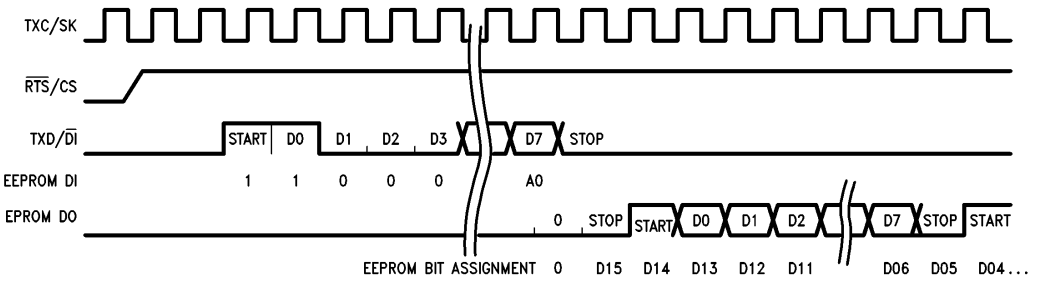

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Table I

	Micro Data	UART XMIT Data		EEPROM
	—	Start-Bit		1
1st Byte	D0	0	Command (Write)	0
	D1	1		1
	D2	0		0
	D3	0		0
	D4	A3		A3
	D5	A2		A2
	D6	A1		A1
	D7	A0		A0
	—	Stop-Bit		D15
	—	Start-Bit		D14
2nd Byte	D0	*ED0		D13
	D1	ED1		D12
	D2	ED2		D11
	D3	ED3		D10
	D4	ED4		D09
	D5	ED5		D08
	D6	ED6		D07
	D7	ED7		D06
	—	Stop-Bit		D05
	—	Start-Bit		D04
	D0	ED8		D03
	D1	ED9		D02
	D2	ED10		D01
	D3	ED11		D00
	D4	N/A		N/A
	D5	N/A		N/A
	D6	N/A		N/A
	D7	N/A		N/A
	—	Stop-Bit		N/A

*EDXX = Usable EEPROM Data

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