Debugging a 32032 Based System with an ISE/16™

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An ISE/16 can be successfully used to debug a 32032-based system by using it in conjunction with a simple adapter. The adapter makes the 32032-based system look like a 32016-based system, as far as the ISE/16 is concerned. A debugging configuration using the adapter is shown in *Figure 1*; *Figure 2* shows the adapter block diagram. As can be seen, the adapter consists of address/data buffers that map the 32032's 32-bit wide data path into a 16-bit wide data path, and logic to generate the necessary control signals including the byte enable signals $\overline{BE0}$,...,$\overline{BE3}$.

Whenever a 32032-based system is being debugged via the ISE/16 and the adapter, a certain performance degradation should be expected. This is due to two factors. First, all memory accesses are limited to either 8 or 16 bits; if a double-word-aligned 32-bit quantity is referenced, two memory cycles are required instead of one. Second, the clock frequency has to be reduced because of the extra level of buffering and cables interposed between the target system and the ISE/16.

CIRCUIT SOLUTIONS

Two circuit solutions are shown in *Figures 4* and *5*. They differ in the way they handle FPU or other slave processors. The first circuit, shown in *Figure 4*, allows any slave in the target system to be accessed. The one in *Figure 5* does not allow slave accesses to the target system; if an FPU is needed, it must be placed in the adapter board. This second solution has the advantage of being simpler than the first one. In the case of *Figure 4*, some extra logic, including a PAL, is needed to check the slave ID byte during an ID broadcast cycle to decide whether or not to enable the data buffers during slave read cycles.

Note that, during MMU slave read cycles the data buffers must not be enabled since the MMU will drive the bus. This extra logic must also prevent the address/data buffers from getting enabled during either slave access cycles or idle cycles. The delays shown in the circuit diagrams are used to avoid possible bus contentions. The one marked 'D1' is used in both circuits and its function is to delay the buffer enable signals during memory write cycles.

Note that the address buffer (74AS244) used to output the address signals A16,...,A23, is disabled at the beginning of the CPU state T2. This could cause signal contentions if the data swap-buffer that handles the signal lines AD16,...,AD23 were enabled at the same time.

The second delay is present only in the first circuit and is used to delay the $\overline{SPC}$ pulse until the $\overline{DDIN}$ signal from the CPU is valid. This is to eliminate spurious signals on the enable pins of the low-order-word data buffers during slave transfers, thus avoiding possible conflicts between these buffers and either the CPU or the slave. Neither of the above delays needs to be accurate and each can be implemented by cascading some spare gates. *Figure 3* shows the PAL® equations in PALASM™ format for the PAL that controls the slave accesses. *Figure 6* provides a timing diagram for memory access cycles.

As shown in *Figures 4* and *5*, several signal lines from the adapter to the target system are not buffered since the target cables are assumed to be very short. If longer cables are needed, these signals should be buffered.

The address/data buffers are Advanced Schottky devices with propagation delays of approximately 8 ns. These delays must be added to the ISE/16 buffer and cable propagation delays, and to the adapter cable delays, to determine the resulting timing at the 32032 socket on the target system. This is needed to determine the clock frequency to be used during debugging.

See Chapter 6 of the ISE/16 User Manual for more details.

JUMPER SETTINGS

The jumpers on the adapter board should be configured according to the user requirements. There are three basic cases to consider.

1. The target system does not use the MMU. In this case neither the MMU target cable from the ISE/16 nor the MMU cable from the adapter to the user system are needed. Jumpers W1 (1-3, 2-4), W2, W3 and W4 (1-2) must be installed.
2. The MMU is used on the target system, but the signals A24 and $\overline{INT}$ from the MMU are not used. In this case the MMU target cable from the ISE/16 is required but the MMU cable from the adapter to the target system is not needed. The $\overline{PAV}$ and $\overline{HLDAO}$ signals from the MMU can be routed to the $\overline{ADS}$ and $\overline{HLDA}$ lines of the CPU cable, by installing jumpers W1 (1-2) and W4 (1-2). Jumpers W2 and W3 must be removed. In addition, on the target system, the signals $\overline{ADS}$ and $\overline{HLDA}$ must be connected to $\overline{PAV}$ and $\overline{HLDAO}$ respectively.
3. The MMU is used on the target system, and so are A24 and $\overline{INT}$. In this case both the MMU target cable from the ISE/16 and the MMU cable from the adapter to the target system are required. The jumpers W1 (1-3) and W4 (1-3) on the adapter must be installed while W2 and W3 must be removed.

The setting of jumper W5 is only relevant if either the clock from the target system is required during debugging or a 32016 CPU together with a TCU and MMU is used instead of the ISE/16. If the ISE/16 internal clock is used during debugging the setting of W5 is irrelevant.

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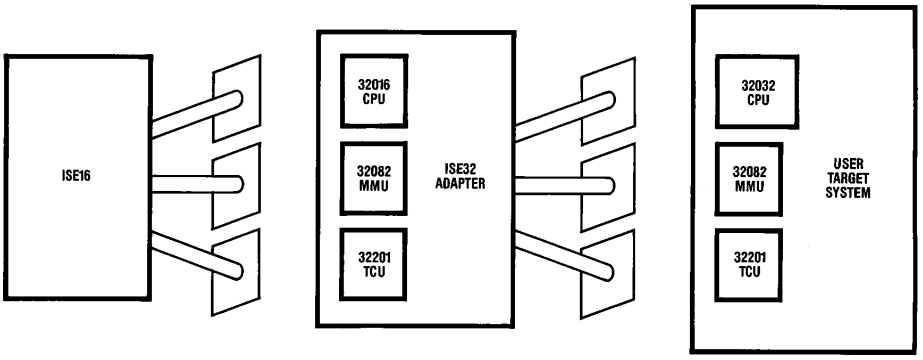

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FIGURE 1. ISE/32 Adapter General Configuration

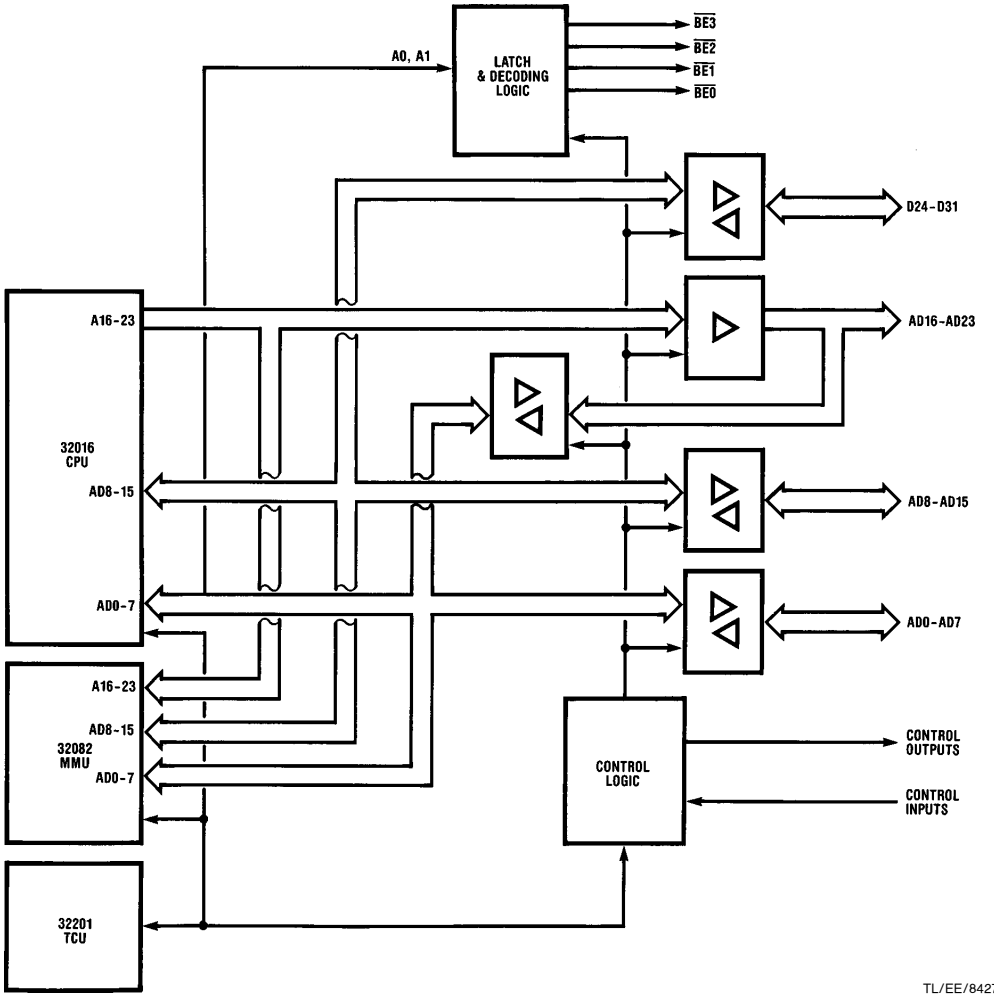

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FIGURE 2. ISE/32 Adapter Block Diagram

```
PAL16L8A
PART#
SLAVE ACCESS CONTROL
NATIONAL SEMICONDUCTOR
A  B  C  D  E  F  G  H  L  GND
M  O1  N  P  Q  O2  NC  NC  O3  VCC
/O1 = /E*/F*/G*H*L*M*N*/P
/O2 = A*B*C*D*Q
/O3 = A*B*C + A*B*/C*D + /A*/B*D
DESC
```

FIGURE 3. PAL Equations in 'PALASM' Format

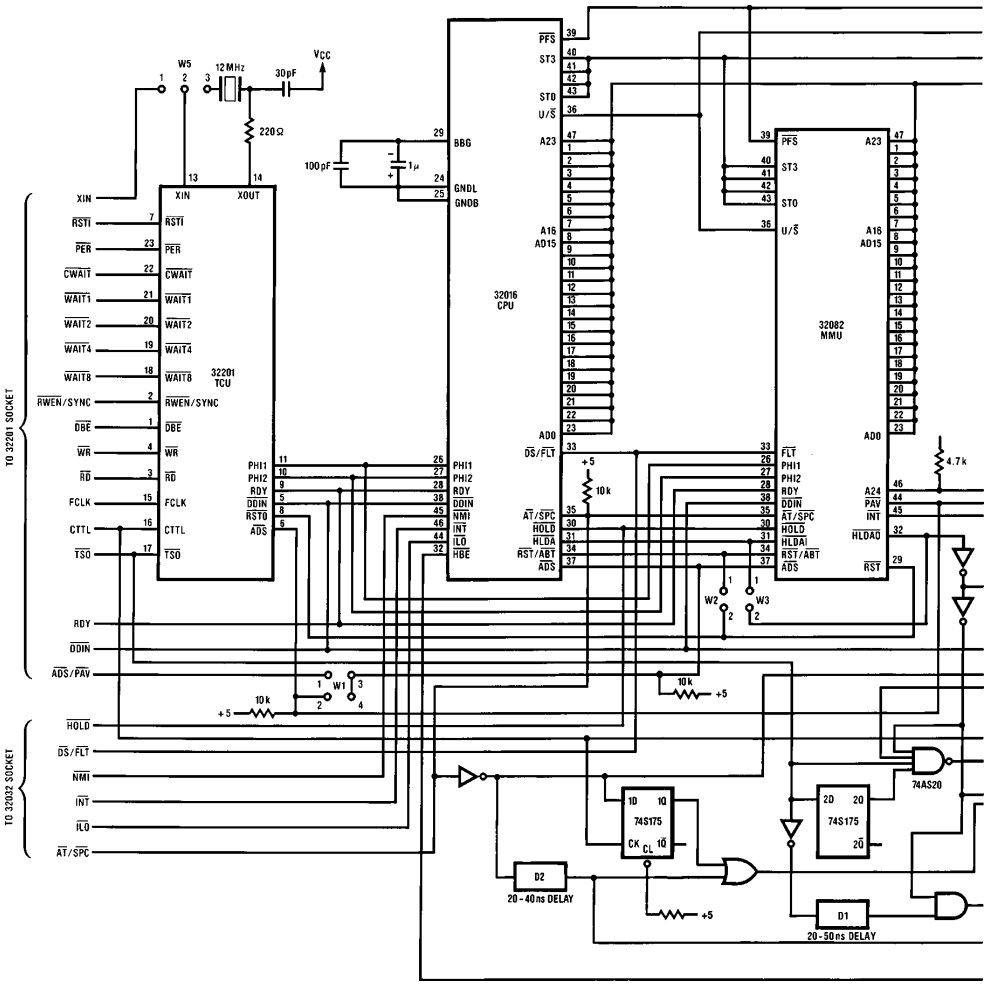

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FIGURE 4. ISE/32 adapter circuit diagram. Slave accesses to the target system are allowed.

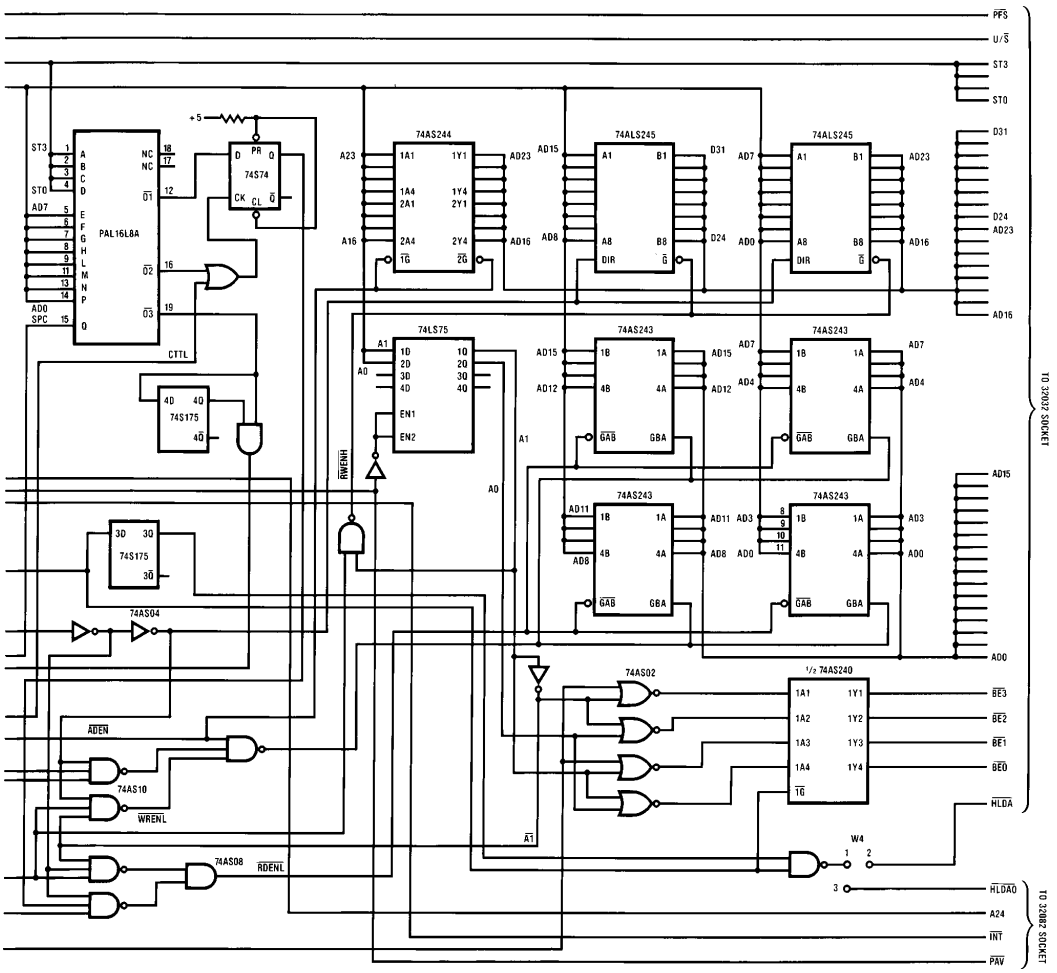

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FIGURE 4. ISE/32 adapter circuit diagram. Slave accesses to the target system are allowed. (Continued)

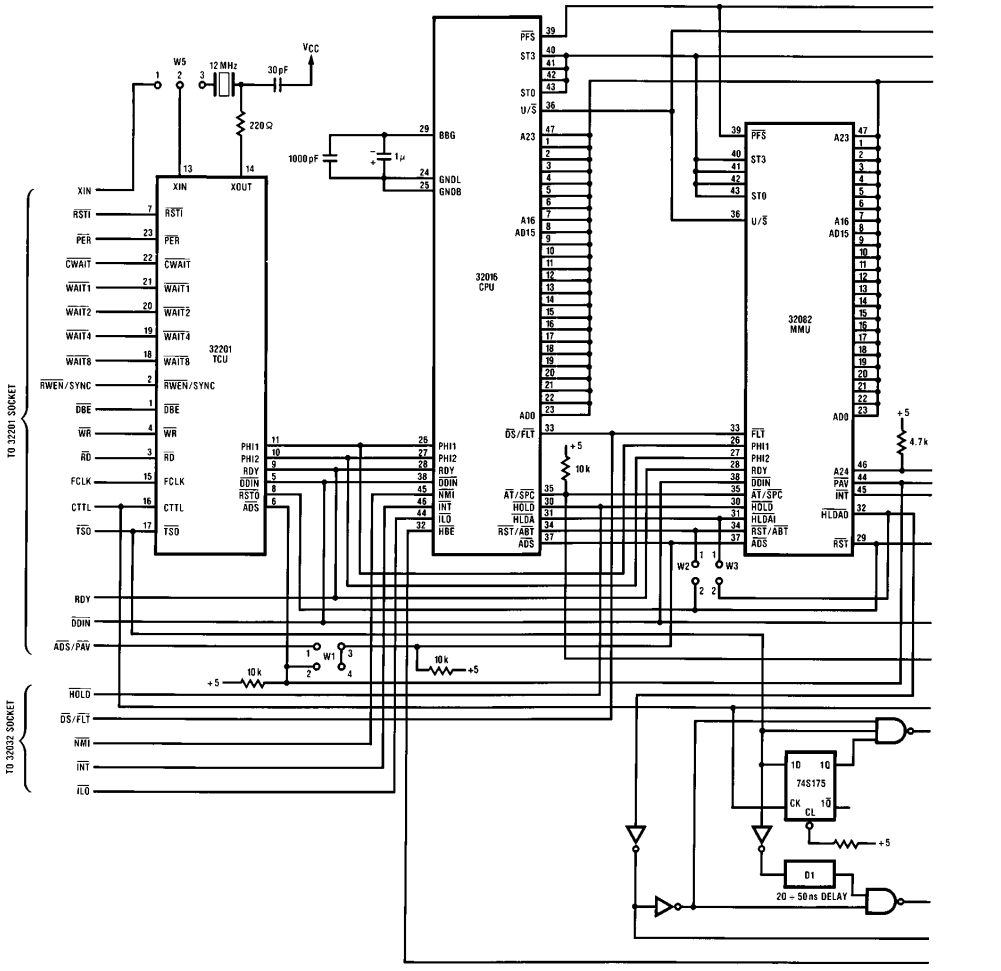

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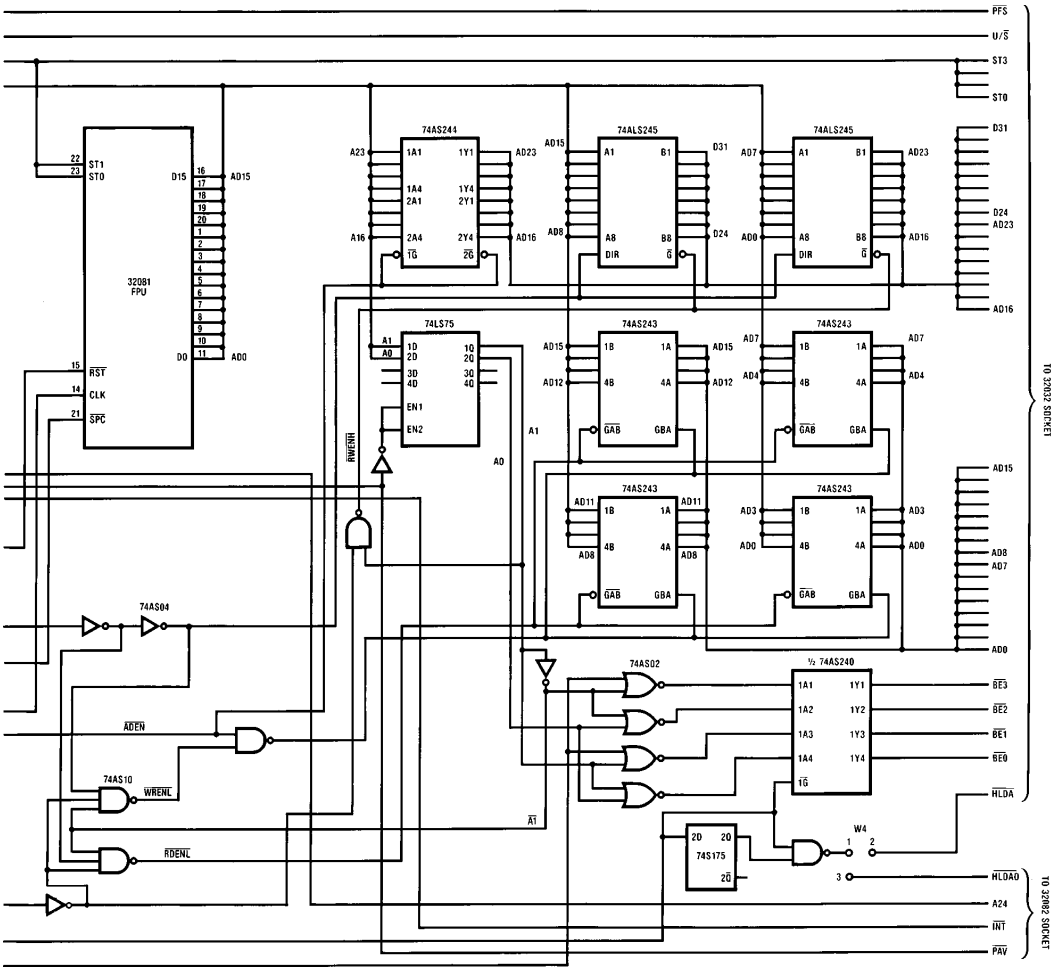
FIGURE 5. ISE/32 adapter circuit diagram. Slave accesses to the target system are not allowed.



TL/EE/8427–6

FIGURE 5. ISE/32 adapter circuit diagram. Slave accesses to the target system are not allowed. (Continued)

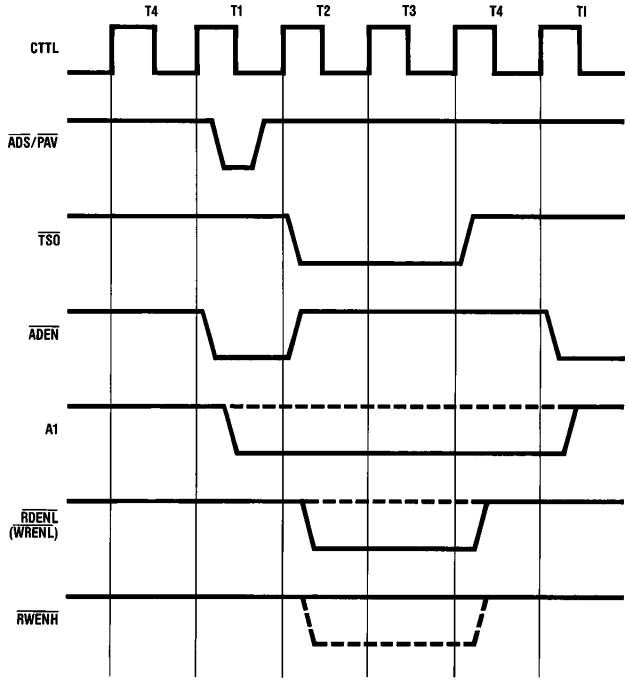


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FIGURE 6. Memory Read (Write) Timing Diagram

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National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408