Designing an LCD Dot Matrix Display Interface

National Semiconductor
Application Note 350
Bob Lutz
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The MM58201 is a CMOS LCD driver capable of driving a multiplexed display of up to 192 segments (24 segment columns by 8 backplanes). The number of backplanes being driven is programmable from one to eight. Data to be displayed is sent to the chip serially and stored in an internal RAM. An external resistor and capacitor control the frequency of the driving signals to the LCD. The MM58201 can also be programmed to accept the oscillator output and backplane signals of another MM58201 for cascading purposes. The displayed data may also be read serially from the on-chip RAM. A simplified functional block diagram of the MM58201 is shown in *Figure 1*.

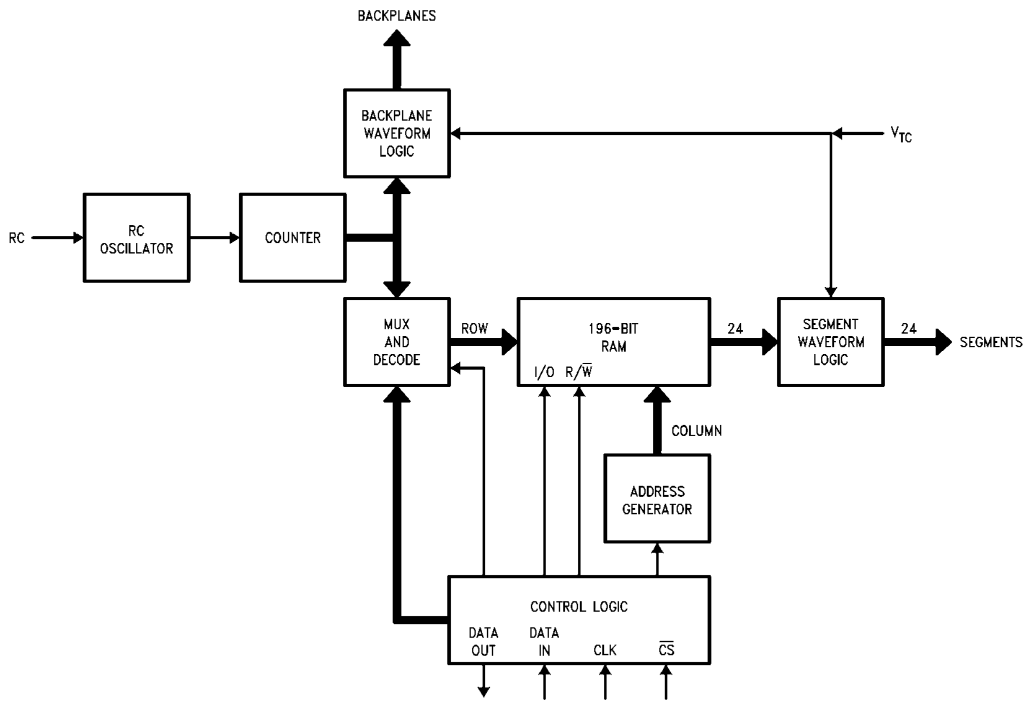

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FIGURE 1. MM58201 Functional Diagram

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BACKGROUND

LCD displays have become very popular because of their ultra-low power consumption and high contrast ratio under high ambient light levels. Typically an LCD has a backplane that overlaps the entire display area and multiple segment lines that each overlap just one segment or descriptor. This means that a separate external connection is needed for every segment or descriptor as shown in *Figure 2*. For a display with many segments such as a dot matrix display, the number of external connections could easily grow to be very large.

Unlike other display technologies that respond to peak or average voltage and current, LCDs are sensitive to the rms voltage between the backplane and given segment location. Also, any DC bias across this junction would cause an irreversible electrochemical action that would shorten the life of the display. A typical LCD driving signal is shown in *Figure 3*. The backplane signal is simply a symmetrical square wave. The individual segment outputs are also square waves, either in phase with the backplane for an ''off'' segment or out of phase for an ''on'' segment. This causes a Vrms of zero for an ''off'' segment and a Vrms of +V for an ''on'' segment.

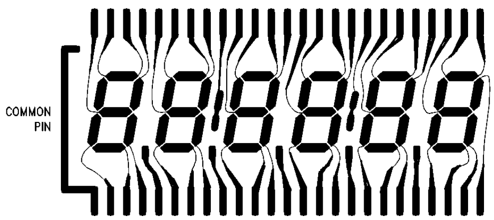

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FIGURE 2. Typical LCD Pin Connections

One way to reduce the number of external connections is to multiplex the display. An example of this could be an LCD with its segments arranged as intersections of an X-Y grid. A driver to control a matrix like this would be fairly straightforward for an LED display. However, it is more complex for an LCD because of the DC bias restriction.

A multiplexed LCD driver must generate a complex set of output signals to insure that an ''on'' segment sees an rms voltage greater than the display's turn-on voltage and that an ''off'' segment sees an rms voltage less than the display's turn-off voltage. The driver must also insure that there is no DC bias.

One pattern that can accomplish this is shown as an example in *Figure 4*. This is the pattern that the MM58201 uses. The actual Vrms of an ''on'' segment and an ''off'' segment is shown in *Figure 5*. If there are eight backplanes, the Vrms (ON) = 0.2935 × V_{TC} and the Vrms (OFF) = 0.2029 × V_{TC}. It can be seen in *Figure 6* that as the number of backplanes increases, the difference between Vrms (ON) and Vrms (OFF) becomes less. Refer to the specifications of the LCD to determine exactly what Vrms is required.

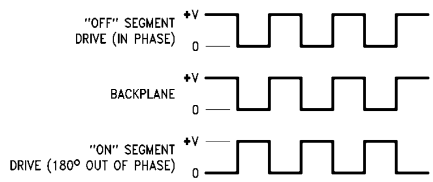

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FIGURE 3. Drive Signals from a Direct Connect LCD Driver

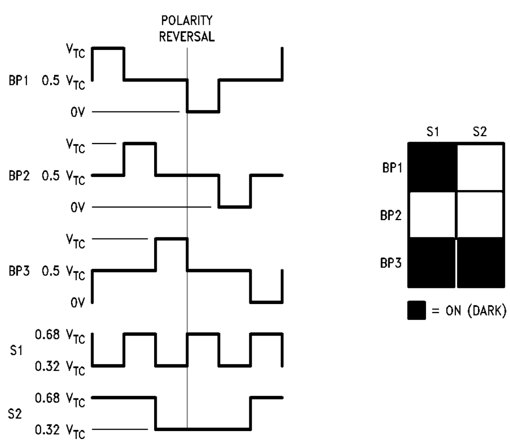

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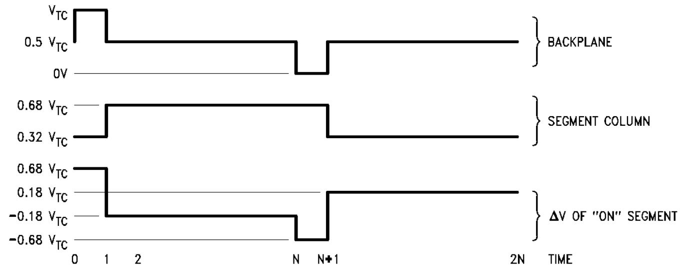
FIGURE 4. Example of Backplane and Segment Patterns



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$$\text{Vrms (ON)} = \left(\frac{1}{T}\int_{t0}^{t0+T} v^2(t)dt\right)^{1/2}$$

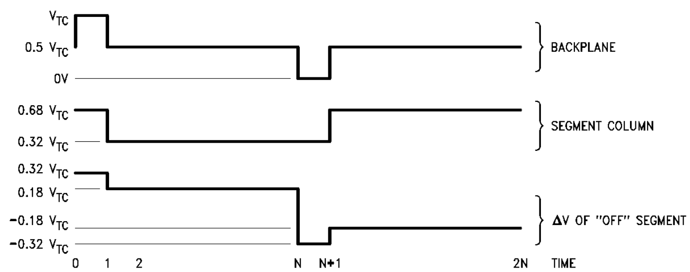
$$= \left(\frac{1}{N}\left[\int_0^1 (0.68\ V_{TC})^2 dt + \int_1^N (-0.18\ V_{TC})^2 dt\right]\right)^{1/2}$$

$$= \left(\frac{1}{N} V_{TC}^2 [0.4624 + 0.0324(N-1)]\right)^{1/2}$$

$$= V_{TC}\left[\frac{0.4624 + 0.0324(N-1)}{N}\right]^{1/2}$$

N = number of backplanes

a. Analysis of Vrms (ON)



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$$\text{Vrms (OFF)} = \left(\frac{1}{T}\int_{t0}^{t0+T} v^2(t)dt\right)^{1/2}$$

$$= \left(\frac{1}{N}\left[\int_0^1 (0.32\ V_{TC})^2 dt + \int_1^N (-0.18\ V_{TC})^2 dt\right]\right)^{1/2}$$

$$= \left(\frac{1}{N} V_{TC}^2 [0.1024 + 0.0324(N-1)]\right)^{1/2}$$

$$= V_{TC}\left[\frac{0.1024 + 0.0324(N-1)}{N}\right]^{1/2}$$

N = number of backplanes

b. Analysis of Vrms (OFF)

$$V_{TC} = 1/2 \left[\underbrace{\frac{V_{rms}\ (\text{OFF})}{\left(\frac{0.1024 + 0.0324(N-1)}{N}\right)}} + \underbrace{\frac{V_{rms}\ (\text{ON})}{\left(\frac{0.4624 + 0.0324(N-1)}{N}\right)}} \right]$$

MUST BE GREATER THAN →

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Example: If N = 8
and Vrms (OFF) = 1.8V
and Vrms (ON) = 2.2V
then V_{TC} = 7.5V

FIGURE 5

FUNCTIONAL DESCRIPTION

Connecting an MM58201 to an LCD

The backplane and segment outputs of the MM58201 connect directly to the backplane and segment lines of the LCD. These outputs are designed to drive a display with a total ‘‘on’’ capacitance of up to 2000 pF. This is especially important for the backplane outputs, as it is usually the backplanes that have the most capacitance. As the capacitance of the output lines increases, the DC offset between a backplane and segment signal may increase. Most LCD displays specify that a maximum offset of 50 mV is acceptable. For backplane capacitance under 2000 pF the MM58201 guarantees an offset of less than 10 mV.

If the LCD display to be used has 24 segments per backplane or less, then each MM58201 should be configured as a ‘‘master’’ so that each one will generate its own set of backplane signals. However, if the LCD display has more than 24 segments per backplane, more than one MM58201 will be needed for each backplane. To synchronize the driving signals there must be one ‘‘master’’ chip and then an additional ‘‘slave’’ chip for every 24 segments after the first 24. When a chip is configured as a ‘‘slave’’ it does not generate its own backplane signals. It simply synchronizes itself to the backplane signals generated by a ‘‘master’’ chip by sensing the BP1 signal. An example of both an all ‘‘master’’ configuration and a ‘‘master-slave’’ configuration will be shown later.

Voltage Control Pin and Circuitry

The voltage presented at the V_{TC} pin determines the actual voltage that is output on the backplane and segment lines. These voltages are shown in *Figure 7*. V_{TC} should be set with respect to Vrms (ON) and Vrms (OFF) and can be calculated as shown in *Figure 5*.

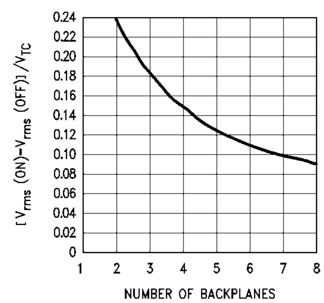

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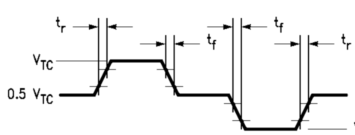
FIGURE 6. ΔVrms/V_{TC}



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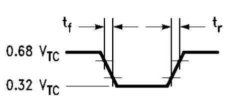
a. Backplane Output



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b. Segment Output

FIGURE 7. Output Voltages

Since the input impedance of V_{TC} may vary between 10 kΩ and 30 kΩ, the output impedance of the voltage reference at V_{TC} should be relatively low. One example of a V_{TC} driver is shown in *Figure 8*. To put the MM58201 in a standby mode, bring V_{TC} to V_{SS} (ground). This will blank out the display and reduce the supply current to less than 300 μA.

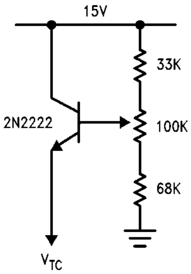

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FIGURE 8. Example of V_{TC} Driver

RC Oscillator

This oscillator works with an external resistor tied to V_{DD} and an external capacitor tied to V_{SS}. The frequency of oscillation is related to the external R and C by:

$$f_{OSC} = 1/1.25\ RC \pm 30\%$$

The value of the external resistor should be in the range from 10 kΩ to 1 MΩ. The value of the external capacitor should be less than 0.005 μF.

The oscillator generates the timing required for multiplexing the LCD. The frequency of the oscillator is 4N times the refresh rate of the display, where N is the number of backplanes programmed. Since the refresh rate should be in the range from 32 Hz to 100 Hz, the oscillator frequency should be:

$$128N < f_{OSC} < 400N$$

If the frequency is too slow, there will be a noticeable flicker in the display. If the frequency is too fast, there will be a loss of contrast between segments and an increase in power consumption.

Serial Input and Output

Data is sent to the MM58201 serially through the DATA IN pin. Each transmission must consist of 30 bits of information, as shown in *Figure 9*. The first five bits are the address, MSB first, of the first column of LCD segments that are to be changed. The next bit is a read or write flag. The following 24 bits are the actual data to be displayed.

The address specifies the first LCD column that is going to be affected. The columns are numbered as shown in *Figure 10*. Data is always written in three column chunks. Twenty-four bits of data must always be sent, even if some of the backplanes are not in use. The starting column can be any number between one (00000) and twenty-four (10111). If column 23 or 24 is specified the displayed data will wrap around to column 1.

If the R/$\overline{W}$ bit is a ‘‘0’’ then the specified columns of the LCD will be overwritten with the new data. If the bit is a ‘‘1’’ then the data displayed in the specified columns will be available serially at the DATA OUT pin and the display will not be changed.

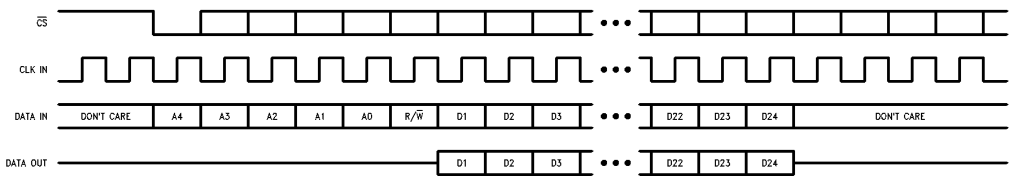

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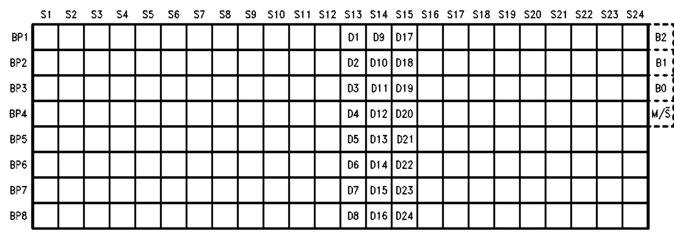
FIGURE 9. Transmission of Data



A4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
A3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1
A2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0
A1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0
A0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

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Diagram above shows where data will appear on display if starting address 01100 is specified in data format.

FIGURE 10. Address of Particular Segment Columns

The data is formatted as shown in *Figure 10*. The first bit in the data stream corresponds to backplane 1 in the first specified column. The second bit corresponds to backplane 2 in the first specified column and so on.

During initialization each MM58201 must be programmed to select how many backplanes are to be used, and whether the chip is to be a "master" or a "slave". The format of this transmission is just like a regular data transmission except for the following: the address must be 11000; the R/$\overline{W}$ must be a write (0); the first three data bits must be selected from the list in Table I. The next bit should be a "1" for the chip to be a master or a "0" for the chip to be a slave. The following 20 bits are necessary to complete the transmission but they will be ignored. The mode cannot be read back from the chip.

TABLE I. Backplane Select

Number of Backplanes	B2	B1	B0
2	0	0	1
3	0	1	0
4	0	1	1
5	1	0	0
6	1	0	1
7	1	1	0
8	1	1	1

The timing of the CLK, $\overline{CS}$, DATA IN, and DATA OUT are illustrated in *Figure 11*. The frequency of the clock can be between DC and 100 kHz with the shortest half-period being 5.0 μs. A transmission is initiated by $\overline{CS}$ going low. $\overline{CS}$ can then be raised anytime after the rising edge of the first clock pulse and before the rising edge of the last clock pulse (the clock edge that reads in D24). 30 bits of information must always be sent.

The data at DATA IN is latched on each rising edge of the clock pulse. The data at DATA OUT is valid after each falling edge of the last 24 clock pulses.

It is important to note that during a read or write transmission the LCD will display random bits. Thus the transmissions should be kept as short as possible to avoid disrupting the pattern viewed on the display. A recommended frequency is:

$f_{OSC} = 30/(t_{LCD} - 7\ t_S)$

t_{LCD} = turn on/off time of LCD

t_S = time between each successive transmission.

This should produce a flicker-free display.

The DATA OUT pin is an open drain N-channel device to V_{SS}. This output must be tied to V_{DD} through a resistor if it is to be used. It could also be tied to a lower voltage if this output is to be interfaced to logic running at a lower voltage. The value of the resistor is calculated by:

$R = (+V - 0.4)/0.0006$

$+V$ = voltage of lower voltage logic

Power Supply

V_{DD} can range between 7V and 18V. A voltage should be used that is greater than or equal to the voltage that you calculate for V_{TC} as shown in *Figure 5*.

TYPICAL APPLICATIONS

One application of the MM58201 is a general purpose display to show graphic symbols and text. This type of display could be used in an electronic toy or a small portable computer or calculator. One such display is shown in *Figure 12*. This display consists of four separate LCD displays that are built into one housing. Each separate LCD display has 8 backplanes and 24 segment lines. The entire display will require four MM58201s to control it.

The circuit diagram of this application is shown in *Figure 14*. Each separate LCD display is driven by one MM58201. The backplanes are driven by the separate MM58201s and are not paralleled together. There are three common lines: CLK, DATA IN, and DATA OUT. The CLK and DATA IN are generated from an output port such as an INS8255. Four other bits of the output port generate a linear select with a different bit going to each MM58201 chip select as shown in *Figure 13*. DATA OUT is sent to one bit of an input port. The V_{TC} driver is as described beforehand. The MM74C906 is an open drain CMOS buffer that has near regular TTL compatible inputs. This is to provide level translation from the 5V supply of the computer system to the 12V supply of the MM58201.

If I/O ports are not available, the circuit in *Figure 15* could be used as an interface between the MM58201s and a microprocessor bus.

To reduce the number of connections between the circuit and the LCD, all of the backplanes could have been driven by one MM58201 as shown in *Figure 16*. The other MM58201s would be configured as ‘‘slaves’’ synchronized to the one ‘‘master’’ MM58201. This would save 24 connections to the LCD but would increase the capacitance of the backplanes. In this application the capacitance is not a problem with either setup.

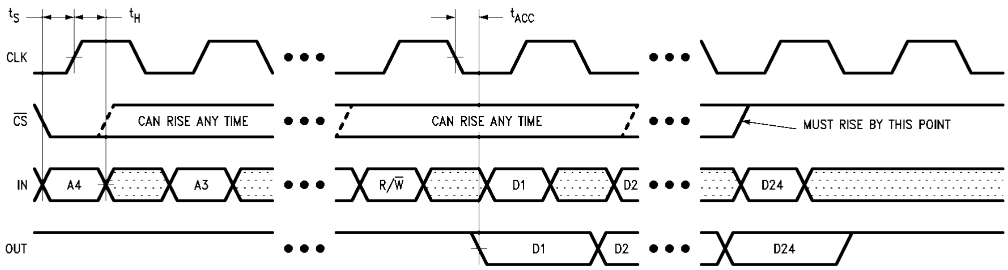

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FIGURE 11. Timing of One Transmission

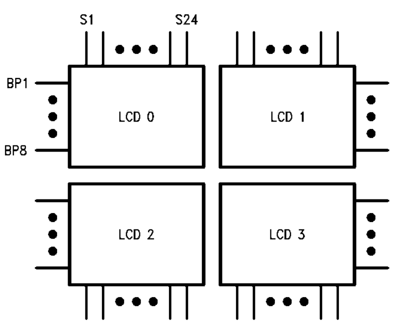

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FIGURE 12. Four Separate LCD Displays Positioned to Look Like One Display

7	6	5	4	3	2	1	0
DATA IN	**CLK**	**X**	**X**	**$\overline{CS4}$**	**$\overline{CS3}$**	**$\overline{CS2}$**	**$\overline{CS1}$**

$\overline{CS4}$	$\overline{CS3}$	$\overline{CS2}$	$\overline{CS1}$	
1	1	1	0	Chip 1 Selected
1	1	0	1	Chip 2 Selected
1	0	1	1	Chip 3 Selected
0	1	1	1	Chip 4 Selected
1	1	1	1	No Chip Selected

FIGURE 13. Chip Select Scheme

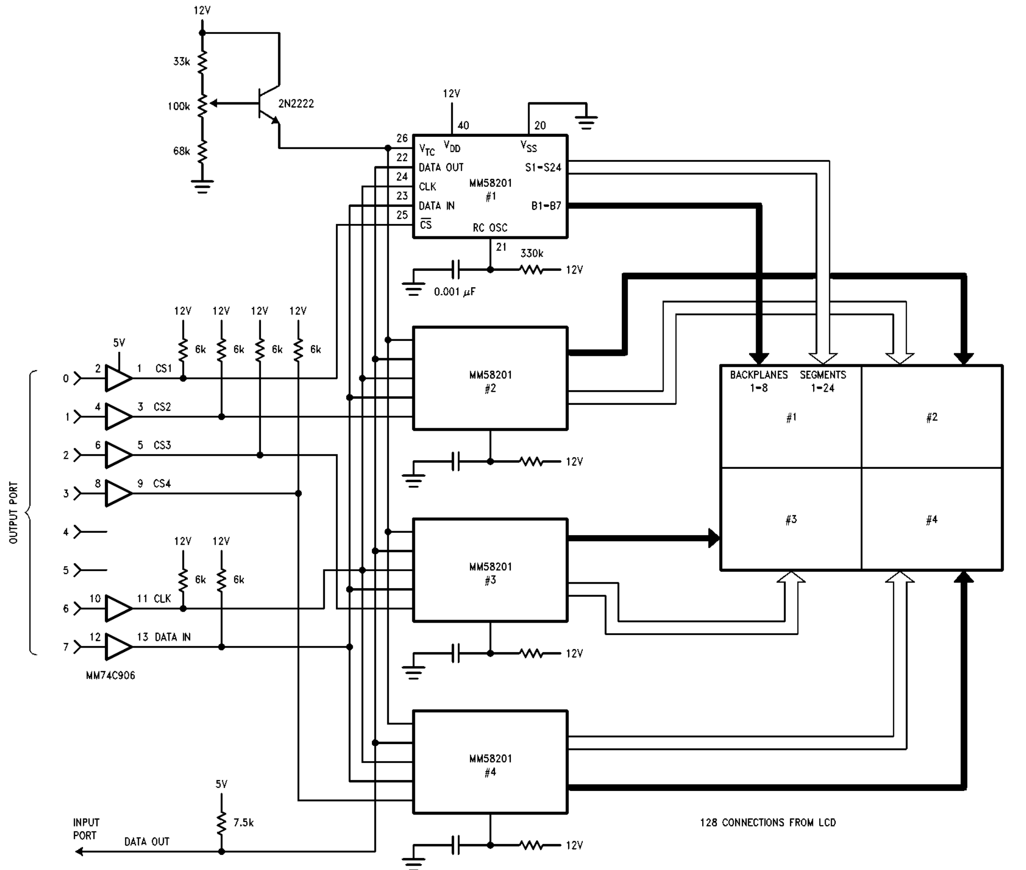

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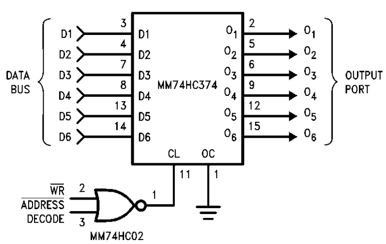
FIGURE 14. Diagram of Application



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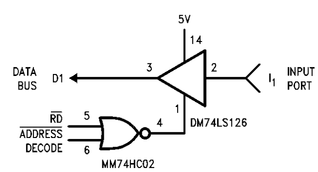
a. Output Port



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b. Input Port

FIGURE 15. Input and Output Ports for Interface

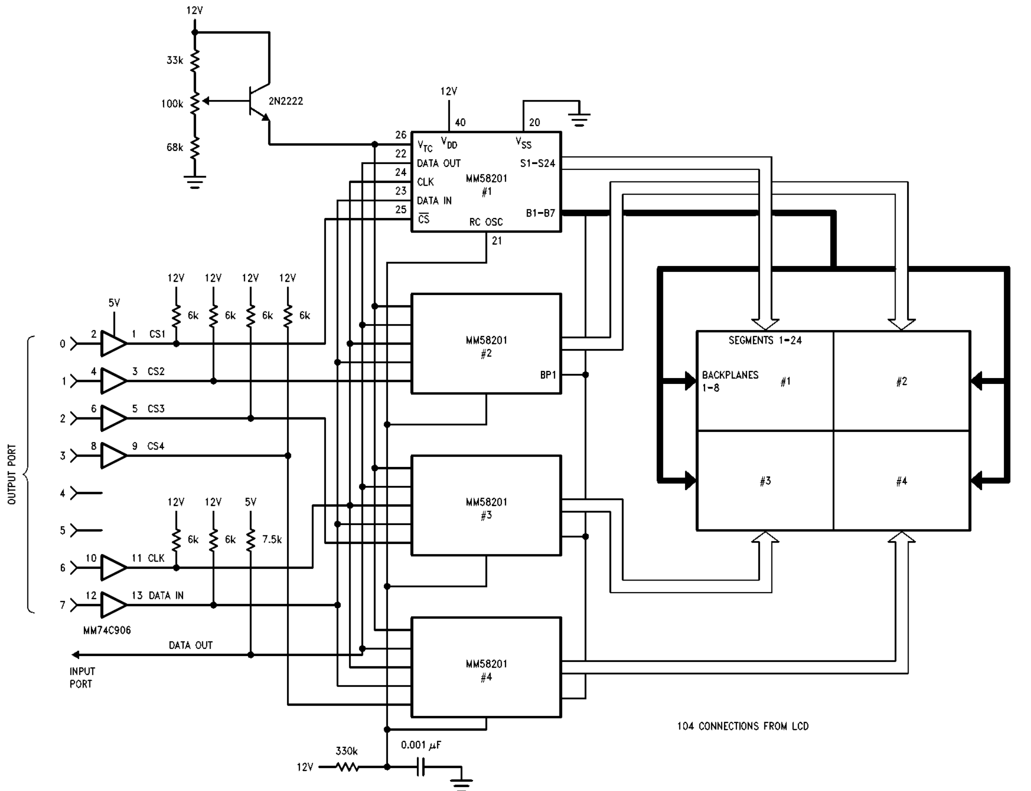

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FIGURE 16. Diagram of a Master-Slave Set-Up Not Used for This Application

SOFTWARE

The real heart of this system is the software which consists of four parts. Part one is the initialization portion. This sets up the MM58201s as ''masters'' and programs them for 8 backplanes. It then sets up the needed pointers for the other subroutines which consist of:

1) GRAPH: displays pattern on LCD.

2) TEXT: prints ASCII characters on display.

3) SCROLL: scrolls whatever pattern is displayed to the right until LCD is cleared.

This application used an NSC800™ with 8080 mnemonics. It could easily be adapted for other microprocessors.

MAIN

This program initializes the MM58201s. It controls the sequence of display output by calling other programs.

It first sends out a ''dummy'' transmission to make sure that the chips are ready to respond to a valid transmission. It then programs the chips to be ''masters'' and to use eight backplanes.

After initialization, this program sets up the correct pointers to display a graphic symbol. First it displays the upper eight bits of it, then it displays the lower eight bits.

The words ''TESTING MM58201'' are then displayed. A call to scroll then causes this to scroll to the right until the screen is blank. Finally the words ''END OF TEST'' appear and the program ends.

The method to create a custom graphic symbol will be demonstrated in the next section.

```
        N8080
        EXTRN GRAPH,WRITE,MODE,TEXT,CURSOR,SCROLL

;INITIALIZE THE STACK POINTER
        LXI SP,1FFFH

;INITIALIZE THE 810
;SET MODE 0 FOR PORT A
;INIT:  MVI A,00H
        OUT 27H
;SET PORT A AS OUTPUT AND PORT C AS INPUT
        MVI A,0FFH
        OUT 24H                 ;PORT A DDR
        MVI A,00H
        OUT 26H                 ;PORT B DDR

;INITIALIZE THE FOUR 58201'S
        MVI A,0                 ;SET FOR WRITE MODE
        STA MODE
        LXI H,MASTER,           ;SEND A COMPLETE TRANSMISSION TO CLEAR OUT
        MVI E,11000B            ;   ANY OLD CHIP SELECT.
        MVI D,00001110B
        CALL WRITE
        LXI H,MASTER            ;CONFIGURE CHIPS 0, 1, 2, AND 3 AS MASTERS
        MVI D,00001110B
        CALL WRITE
        LXI H,MASTER
        MVI D,00001101B
        CALL WRITE
        LXI H,MASTER
        MVI D,00001011B
        CALL WRITE
        LXI H,MASTER
        MVI D,00000111B
        CALL WRITE

;SET UP POINTER AND COUNTERS TO DISPLAY NATIONAL SEMI SYMBOL
        MVI B,21                ;B HOLDS # OF COLUMNS TO CHANGE
RESTRT: MVI D,0                 ;D HOLDS THE STARTING COLUMN NUMBER FOR UPPER HALF
        MVI E,48                ;E HOLDS STARTING COLUMN NUMBER FOR LOWER HALF
DSLOOP: MOV C,D
        LXI H,NATSM1            ;DISPLAY UPPER HALF OF GRAPHIC
        CALL GRAPH
        LXI H,NATSM2            ;DISPLAY LOWER HALF OF GRAPHIC
        MOV C,E
        CALL GRAPH

        LXI H,0FFFFH            ;PAUSE
PAUSE:  DCX H
        MOV A,H
        ORA L
        JNZ PAUSE

        INR D                   ;INCREMENT STARTING COLUMN NUMBERS
        INR D
        INR D
        INR E
        INR E
        INR E
        MVI A,30                ;DISPLAY IT UNTIL COLUMN COUNT IS 30
        CMP D
        JNZ DSLOOP

        LXI H,TEXT1             ;PRINT FIRST TEXT
        MVI A,0                 ;ZERO THE CURSOR
        STA CURSOR
        CALL TEXT

        CALL SCROLL             ;SCROLL THE TEXT

        LXI H,TEXT2             ;PRINT SECOND TEXT
        MVI A,0                 ;ZERO THE CURSOR
        STA CURSOR
        CALL TEXT

        LXI H,0FFFFH            ;PAUSE
PAUSE1: DCX H
        MVI A,2
PAUSE2: DCR A
        JNZ PAUSE2
        MOV A,H
        ORA L
        JNZ PAUSE1
```

```
        LXI H,TEXT3             ;PRINT THIRD TEXT
        MVI A,0
        STA CURSOR
        CALL TEXT

        RST 6                   ;END

TEXT1:  DB "TESTING MM58201 ", 0
TEXT2:  DB "THIS IS THE END ", 0
TEXT3:  DB " OF THE   TEST  ", 0

MASTER: DB 1111B                ;ADDRESS FOR MASTER
SLAVE:  DB 0111B                ;ADDRESS FOR SLAVE

NATSM1: DB 0FFH, 0FFH, 0FFH, 7FH, 3FH, 9FH, 0CFH, 67H, 33H, 01H, 7FH
        DB 3FH, 9FH, 0CFH, 67H, 33H
        DB 99H, 0FFH, 0FFH, 00H, 00H
NATSM2: DB 0FFH, 0FFH, 0FFH, 0E6H, 0F3H, 0F9H, 0FCH, 0FEH, 0FFH
        DB 0E0H, 0E6H, 0F3H, 0F9H, 0FCH
        DB 0FEH, 0FFH, 0FFH, 0FFH, 0FFH, 00H, 00H
        END
```

GRAPH

This subroutine is the center of the software. It is the interface between the calling programs and the hardware. All I/O is generated by this subroutine.

There are two entrances to this subroutine: graph and read. Graph is the entrance used to display new data. Read is the entrance used to read data from the display.

The HL register should point to the beginning of the data to be displayed. The B register should hold the number of columns to change. This must be a multiple of three. The C register should hold the column number to start with. This must also be a multiple of three. These restrictions are to simplify the software.

The first operation is the calculation of the correct chip to enable and the column number to start within that chip. The first bit of the column address is output with the correct chip select going low. The rest of the column address is then output with all the chip selects high. If the operation is a write, the data is sent to the display bit by bit. If the operation is a read, the data is read in bit by bit.

To create a custom graphic symbol, draw it on a grid as shown in *Figure 17*. Group the upper eight squares as a byte with the least significant bit at the top, counting a dark square as a one. Group the lower eight squares as a byte with the most significant bit at the bottom. Use this generated data as input lists to the graph subroutine. A good example of this is shown in the listing of main when it calls graph.

Pad the data at the end with zeros as shown to keep the number of data values a multiple of three. Remember, this is only a software restriction. A different routine could be used that would allow any number of columns to be displayed.

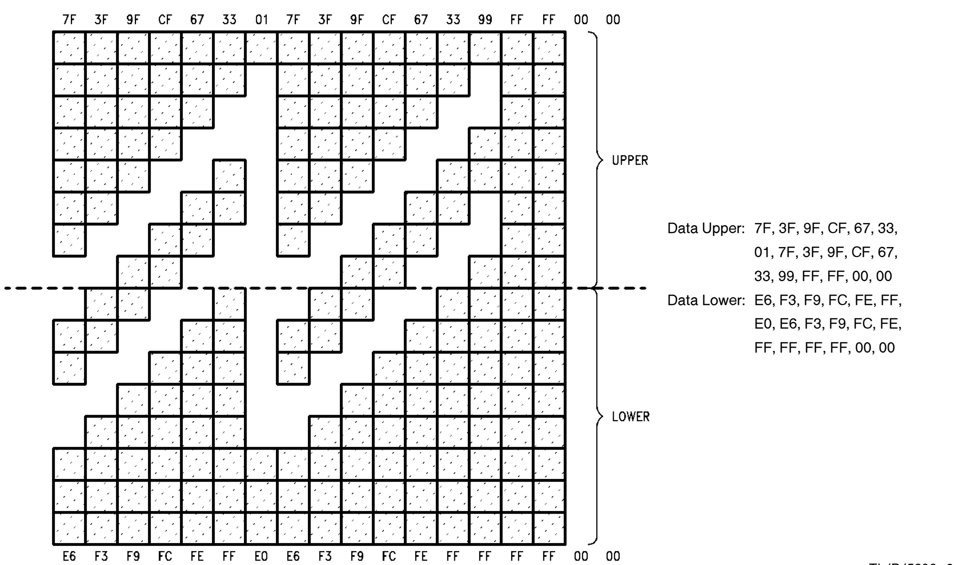


FIGURE 17. Example Graphic Symbol

```
        N8080
        PUBLIC GRAPH, READ, WRITE, MODE
;GRAPHIC DISPLAY DRIVER
;       INPUT:  HL - POINTS TO START OF DATA
;               B- # OF 8 BIT COLUMNS TO CHANGE (MUST BE MULT. OF 3)
;               C- COLUMN # TO START WITH (MUST BE MULT. OF 3)
;       OUTPUT: NO REGISTERS DISTURBED
;               DATA POINTED TO IS DISPLAYED ON LCD DISPLAY.
;               COLUMNS NOT SPECIFIED ARE NOT AFFECTED.
READ:
;SAVE ALL STATES
        PUSH PSW
        PUSH B
        PUSH D
        PUSH H
;FLAG FOR A READ OPERATION
        MVI A,10000000B
        STA MODE
        JMP GRAPH1
GRAPH:
;SAVE ALL STATES
        PUSH PSW
        PUSH B
        PUSH D
        PUSH H
;FLAG FOR A WRITE OPERATION
        MVI A,0
        STA MODE
;CALCULATE WHICH 58201 TO ACCESS
GRAPH1: MVI D,0EEH              ;START WITH CS1
ACC:    MOV A,C
        SUI 24                  ;SUBTRACT 24 FROM COLUMN COUNT
        JC GO                   ;IF CARRY IS SET THE CORRECT CHIP IS SELECTED
        MOV C,A                 ;REG C GETS NEW COLUMN NUMBER
        MOV A,D
        RLC                     ;INCREMENT THE CS TO NEXT CHIP
        MOV D,A
        JMP ACC
;MAIN LOOP
GO:     MOV E,C                 ;GET COLUMN NUMBER
M.LOOP: CALL WRITE              ;DRAW 3 COLUMNS
        DCR B                   ;SUBTRACT 3 FROM COLUMN COUNT
        DCR B
        DCR B
        JZ END.G                ;IF DONE, JUMP.
        MOV A,E                 ;ADD 3 TO ADDRESS
        ADI 3
        CPI 11000B              ;IF ADDRESS NOT MAX THEN SKIP THIS
        JNZ SKIP1
        MOV A,D
        RLC                     ;SELECT NEXT 58201 CS
        MOV D,A
        MVI A,0
SKIP1:  MOV E,A                 ;SAVE NEXT ADDRESS
        JMP M.LOOP              ;LOOP UNTIL DONE
END.G:  POP H                   ;RESTORE ALL STATES
        POP D
        POP B
        POP PSW
        RET
WRITE:
;       DISPLAY 3 COLUMNS OF DATA
;       INPUT:  HL- POINTS TO START OF DATA
;               E - ADDRESS
;               D - OUTPUT CS
;       OUTPUT: HL <- HL + 3
;SAVE ALL STATES
        PUSH PSW
        PUSH B
        PUSH D
START:  MVI A,00001111B ;ISOLATE CS IN REG D
        ANA D
        MOV D,A
        MOV A,E                 ;GET ADDRESS BITS AT HIGH END OF BYTE
        RLC
        RLC
        MOV E,A
```

```
;OUTPUT FIVE ADDRESS BITS WITH CHIP SELECT
        MVI C,5
W.LOOP: MOV A,E
        RLC                     ;ROTATE ADDRESS
        MOV E,A
        MVI A,10000000B
        ANA E                   ;GET MSB
        ORA D                   ;MERGE WITH CHIP SELECT
        CALL DISPLY
        DCR C                   ;DEC ADDRESS BIT COUNTER
        JNZ W.LOOP              ;LOOP UNTIL ADDRESS IS OUT

;SIGNAL FOR A READ OR WRITE
        LDA MODE
        ORI 00001111B
        CALL DISPLY
        JP DIS0                 ;JUMP IF THIS IS A WRITE

;READ THE DATA
        MVI B,3                 ;3 BYTES OF DATA
READ1:  MVI C,B                 ;8 BITS PER BYTE
        MVI D,0                 ;CLEAR DATA BYTE
READ2:  IN 22H                  ;GET A BIT OF DATA
        ANI 00000001B           ;MASK OFF UNWANTED BITS
        ORA D                   ;MERGE WITH DATA BYTE
        RRC                     ;ROTATE DATA
        MOV D,A
        MVI A,00001111B         ;SET UP 58201 TO READ NEXT BIT
        CALL DISPLY
        DCR C                   ;LOOP UNTIL DONE WITH BYTE
        JNZ READ2
        MOV M,D
        INX H                   ;INCREMENT BYTE POINTER
        DCR B                   ;LOOP UNTIL DONE WITH ALL BYTES
        JNZ READ1

;RESTORE STATES
        POP D
        POP B
        POP PSW
        RET

;DISPLAY THE DATA
DIS0:   MVI B,3                 ;3 BYTES OF DATA
DIS1:   MVI C,8                 ;8 BITS PER BYTE
        MOV D,M
DIS2:   MOV A,D                 ;ROTATE DATA
        RRC
        MOV D,A
        ANI 10000000B           ;GET NEXT BIT
        ORI 00001111B           ;SET CS
        CALL DISPLY             ;OUTPUT A BIT OF DATA
        DRC C
        JNZ DIS2                ;LOOP UNTIL DONE WITH BYTE
        INX H
        DCR B
        JNZ DIS1                ;LOOP UNTIL DONE WITH 3 BYTES

;RESTORE STATES
        POP D
        POP B
        POP PSW
        RET

DISPLY:
;DISPLAY ROUTINE
;       INPUT:  A - DATA AND CHIP SELECT
;                               BIT 7 - DATA
;                               BITS 0-3 - CHIP SELECT
;       OUTPUT: NO REGISTERS DISTURBED
;               OUTPUT ONE BIT TO 58201

        PUSH PSW                ;SAVE STATES

        ANI 10001111B           ;MASK OFF UNWANTED BITS
        OUT 20H                 ;SET UP DATA AND CHIP SELECT
        ORI 01000000B           ;CLOCK HIGH
        OUT 20H
        ANI 10111111B           ;CLOCK LOW

        POP PSW                 ;RESTORE STATES
        RET

MODE:   DS 1
        END
```

TEXT

This subroutine will take the ASCII text pointed to by HL and display it on the LCD starting at the column pointed to by the memory location CURSOR. The data should end with a zero. CURSOR should be in the range of 0–15 as this is the extent of this LCD display. The first operation is the calculation of the offset into the ASCII table of the first character. Thirty-two is subtracted from the ASCII number because the table starts with a space character. This result is then multiplied by six because the data to be displayed is six bytes long. We now have the offset into the table. The character is displayed on the LCD. This operation is repeated until all the characters have been displayed.

A custom font can be generated using the same technique as that used to create a custom graphic symbol.

```
        N8080
        EXTRN GRAPH
        PUBLIC TEXT, LET        TR, CURSOR

TEXT:
;DISPLAY A CHARACTER STRING ON LCD DISPLAY
;       INPUT:  HL-POINTS TO BEGINNING OF STRING
;               CURSOR-CURRENT CURSOR POSITION
;       OUTPUT: CURSOR <= CURSOR + LENGTH OF STRING
;               NO REGISTERS DISTURBED

        PUSH PSW                ;SAVE STATES
        PUSH H
T.LOOP: MOV A,M                 ;CHECK FOR END OF STRING
        CPI 0
        JZ T.FIN
        CALL LETTR              ;PRINT LETTER
        INX H
        JMP T.LOOP              ;LOOP UNTIL DONE
T.FIN:  POP H                   ;RESTORE STATES
        POP PSW
        RET


LETTR:
;DISPLAY AN ASCII CHARACTER ON LCD DISPLAY
;       INPUT:  A-CHARACTER TO DISPLAY
;               CURSOR-CURRENT CURSOR LOCATION (0 - 95)
;       OUTPUT: CURSOR <= CURSOR + 1
;               NO REGISTERS DISTURBED

;SAVE STATES
        PUSH PSW
        PUSH B
        PUSH D
        PUSH H

;SET UP HL TO POINT TO CORRECT DATA
        LXI H,ASCII             ;HL POINTS TO BASE ADDRESS
        MVI B,0                 ;BC GETS ASCII OFFSET MINUS A CONSTANT
        SUI 20H
        MOV C,A
        CALL MULT               ;MULTIPLY OFFSET BY 6 (DOUBLE PRECISION)
        DAD B                   ;HL POINTS TO CORRECT CHARACTER DATA
        LDA CURSOR              ;MULTIPLY CURSOR BY 6 TO GET COLUMN NUMBER
        MOV B,A
        ADD B
        ADD B
        ADD B
        ADD B
        ADD B
        MOV C,A
        MVI B,6                 ;EACH CHARACTER IS SIX COLUMNS WIDE
        CALL GRAPH              ;DISPLAY THE CHARACTER
        LDA CURSOR              ;INCREMENT CURSOR
        INR A
        CPI 16                  ;CHECK FOR END OF LCD DISPLAY
        JNZ T.END
        MVI A,0                 ;IF SO, RESET TO ZERO
T.END:  STA CURSOR

;RESTORE STATES
        POP H
        POP D
        POP B
        POP PSW
        RET
```

```
MULT:
;MULTIPLY BC REG BY SIX
;       INPUT:  BC - MULTIPLICAND
;       OUTPUT: BC <= BC * 6
;               NO REGISTERS DISTURBED
        PUSH PSW
        PUSH H
        MOV H,B
        MOV L,C
        DAD B
        DAD B
        DAD B
        DAD B
        DAD B
        MOV B,H
        MOV C,L
        POP H
        POP PSW
        RET
CURSOR: DS 1
ASCII:  DB 0,0,0,0,0,0          ;SPACE
        DB 0,95,95,0,0,0        ;!
        DB 0,7,0,7,0,0          ;"
        DB 20,127,20,127,20,0   ;#
        DB 36,42,127,42,18,0    ;$
        DB 35,19,8,100,98,0     ;%
        DB 54,73,102,32,80,0    ;&
        DB 0,0,7,0,0,0          ;'
        DB 0,28,34,65,0,0       ;(
        DB 0,65,34,28,0,0       ;)
        DB 34,20,127,20,34,0    ;*
        DB 8,8,62,8,8,0         ;+
        DB 0,64,48,0,0,0        ;'
        DB 8,8,8,8,8,0          ;-
        DB 0,96,96,0,0,0        ;.
        DB 32,16,8,4,2,0        ;/
        DB 62,81,73,69,62,0     ;0
        DB 0,66,127,64,0,0      ;1
        DB 122,73,73,73,70,0    ;2
        DB 34,65,73,73,54,0     ;3
        DB 15,8,8,126,8,0       ;4
        DB 39,69,69,69,57,0     ;5
        DB 62,73,73,73,49,0     ;6
        DB 1,97,17,9,7,0        ;7
        DB 54,73,73,73,54,0     ;8
        DB 6,9,9,9,126,0        ;9
        DB 0,54,54,0,0,0        ;:
        DB 96,54,54,0,0,0       ;;
        DB 8,20,34,65,0,0       ;<
        DB 20,20,20,20,20,0     ;=
        DB 0,65,34,20,8,0       ;>
        DB 2,1,88,5,2,0         ;?
        DB 62,65,93,89,78,0     ;@
        DB 124,18,17,18,124,0   ;A
        DB 127,73,73,73,54,0    ;B
        DB 62,65,65,65,34,0     ;C
        DB 127,65,65,65,62,0    ;D
        DB 127,73,73,65,65,0    ;E
        DB 127,9,9,1,1,0        ;F
        DB 62,65,65,81,114,0    ;G
        DB 127,8,8,8,127,0      ;H
        DB 0,65,127,65,0,0      ;I
        DB 32,64,64,64,63,0     ;J
        DB 127,8,20,34,65,0     ;K
        DB 127,64,64,64,64,0    ;L
        DB 127,2,12,2,127,0     ;M
        DB 127,4,8,16,127,0     ;N
        DB 62,65,65,65,62,0     ;O
        DB 127,9,9,9,6,0        ;P
        DB 62,65,81,33,94,0     ;Q
        DB 127,9,25,41,70,0     ;R
        DB 34,69,73,81,34,0     ;S
        DB 1,1,127,1,1,0        ;T
        DB 63,64,64,64,63,0     ;U
        DB 31,32,64,32,31,0     ;V
        DB 127,32,24,32,127,0   ;W
        DB 99,20,8,20,99,0      ;X
        DB 3,4,120,4,3,0        ;Y
        DB 97,81,73,69,67,0     ;Z
END
```

SCROLL

This subroutine will scroll whatever is displayed on the LCD to the right until the screen is clear. It first reads in three columns of data. It then writes three columns of data with the HL pointer shifted by one byte. This will shift the displayed data by one column. This is repeated until the entire LCD has been shifted by one column. Then the entire operation is repeated until all the displayed data is shifted off the screen.

This subroutine could easily be adapted to scroll the display to the left if desired.

```
        N8080
        PUBLIC SCROLL
        EXTRN READ,GRAPH

SCROLL:
;SCROLLS DISPLAY TO THE RIGHT UNTIL CLEAR
;       INPUT:  NONE
;       OUTPUT: NO REGISTERS ARE CHANGED
;               SCREEN IS SCROLLED UNTIL CLEAR

;SAVE ALL STATES
        PUSH PSW
        PUSH B
        PUSH D
        PUSH H

;SET UP ALL THE POINTERS
        MVI D,96                ;LOOP UNTIL SCREEN IS CLEAR (96 CYCLES)
REPEAT: MVI A,0                 ;CLEAR FIRST BYTE IN BUFFER
        STA BUFFER
        MVI B,3                 ;READ 3 COLUMNS ALWAYS
        MVI C,0                 ;START WITH COLUMN ZERO

;READ THE DATA
L.READ: LXI H,BUFFER+1          ;SET HL TO POINT TO BUFFER+1
        CALL READ
        LXI H,BUFFER            ;SET HL TO SHIFT THE DATA
        CALL GRAPH              ;REDRAW THE SHIFTED DATA

;MOVE LAST COLUMN OF LAST READ INTO FIRST COLUMN OF NEXT WRITE
        LDA BUFFER+3
        STA BUFFER

;UPDATE COUNTERS
        MOV A,C                 ;INCREMENT COLUMN NUMBER
        ADI 3
        MOV C,A
        CPI 96                  ;CHECK IF DONE WITH ONE CYCLE
        JNZ L.READ
        DCR D                   ;DECREMENT LOOP COUNT
        JNZ REPEAT              ;LOOP UNTIL DONE WITH ALL CYCLES

;RESTORE STATES
        POP H
        POP D
        POP B
        POP PSW
        RET

BUFFER: DS 4

        END
```

OTHER APPLICATIONS

There are many different types of LCDs that can be controlled by the MM58201. Some of these are shown in *Figure 18*.

Up to 24 seven-segment digits can be controlled by one MM58201. The software to control a multiplexed seven-segment display is not too much different from that of the previous application. The software is simpler because only one MM58201 is needed instead of four. A logic diagram for a six-digit multiplexed seven-segment LCD display is shown in *Figure 19* and the software to control it is in Listing 5.

Given a string of numbers to display, this subroutine simply looks up the data it needs from a look-up table and stores this data in a buffer. After every three digits, the subroutine sends this data to the MM58201 to be displayed. The digit backplanes are wired backward in groups of three to simplify the software. The subroutines that this subroutine uses are very similar to the equivalent subroutines in the LCD dot matrix application. Since there is only one MM58201, the software is simpler. There is no need to calculate which MM58201 chip select to enable.

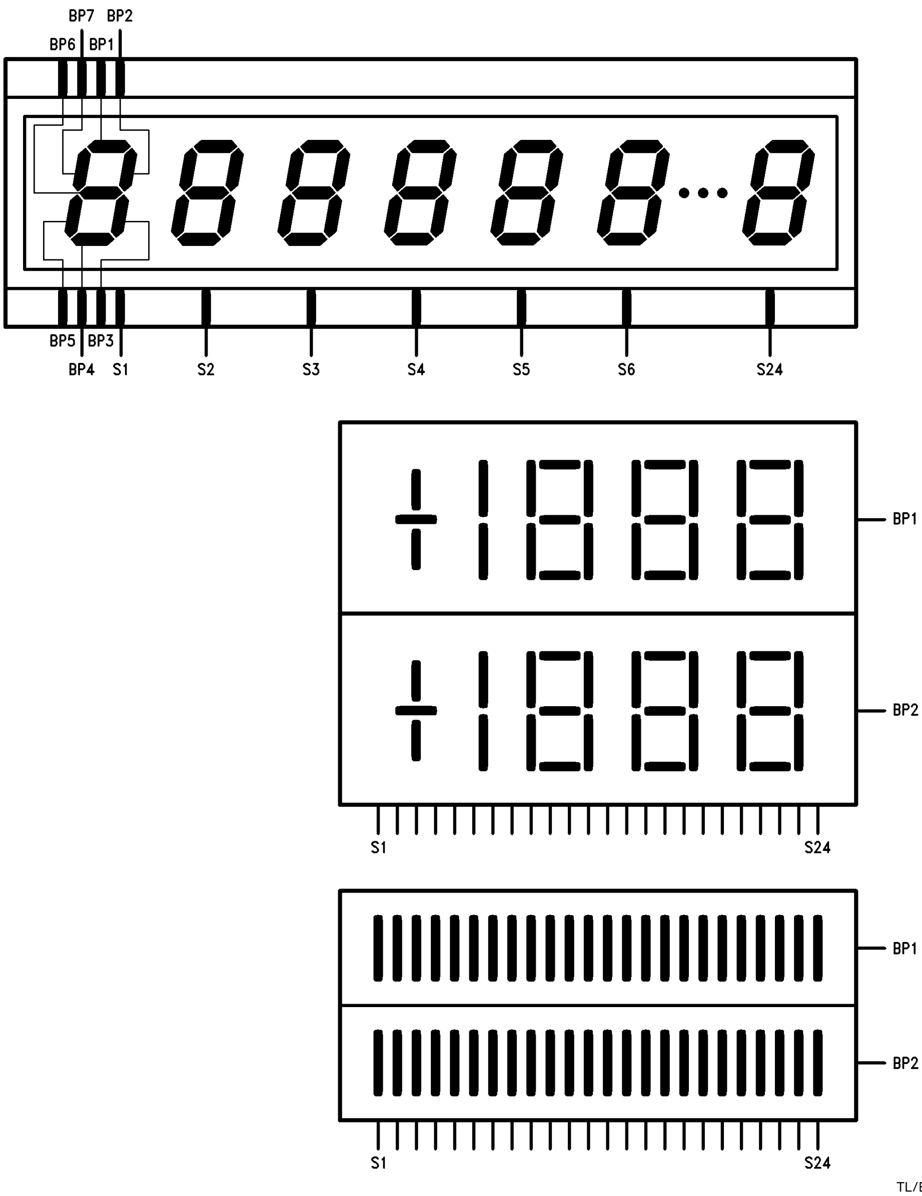
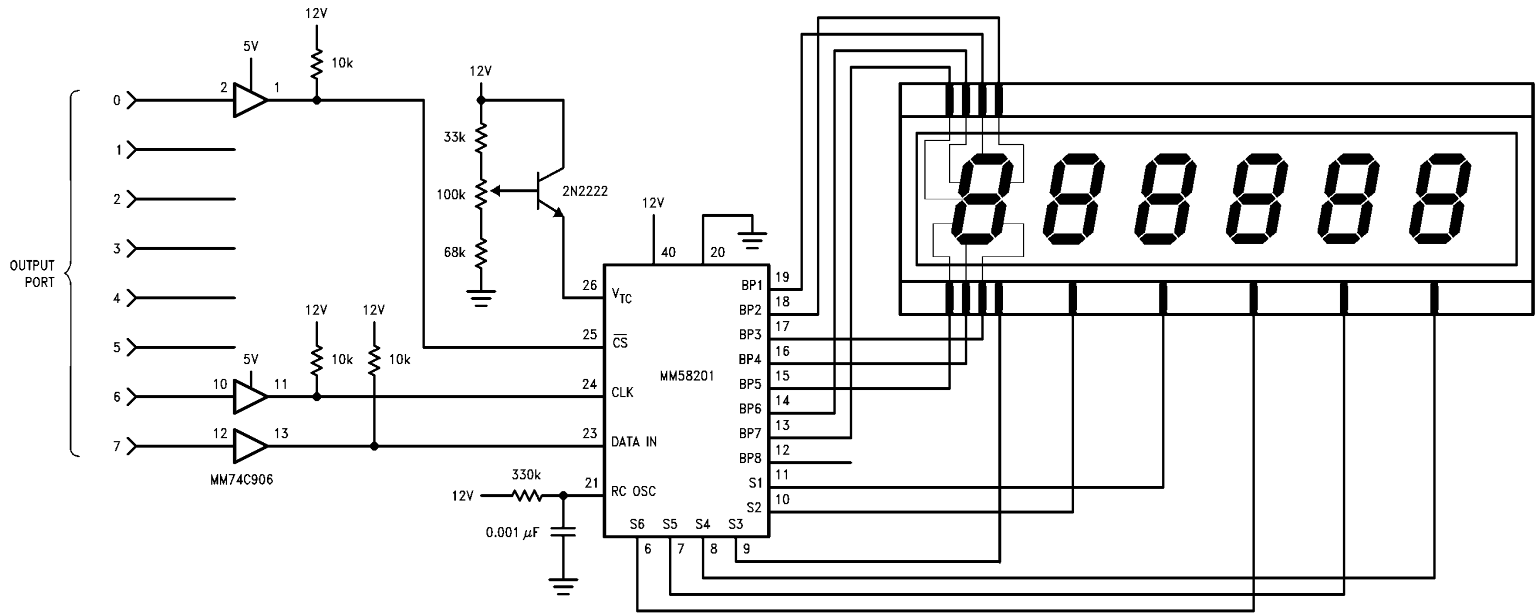


FIGURE 18. Typical LCD Connections to the MM58201



TL/B/5606–22

FIGURE 19. Diagram of a Six-Digit Seven-Segment LCD Multiplexed Display

```
        N8080
;INITIALIZE THE 810
        MV A,0
        OUT 27H
        MVI A,0FFH
        OUT 24H

        LXI BC,TEST
        MVI E,6
        CALL NUMBER
        RST 6

TEST:   DB 1,2,3,4,5,6

;SUBROUTINE TO DISPLAY NUMERALS ON LCD DISPLAY
;       INPUT   BC-POINTS TO BCD DATA STRING
;               E -LENGTH OF DATA STRING (MULTIPLE OF 3)
;       OUTPUT    -NO REGISTERS DISTURBED
;                 -DATA STRING IS DISPLAYED
;
NUMBER: PUSH PSW                ;SAVE STATES
        PUSH B
        PUSH D
        PUSH H

DIG3:   MVI D,3                 ;LOOP FOR 3 DIGITS
LOOP:   LDAX B
        LXI H,TABLE             ;CALCULATE ADDRESS INTO TABLE
        ADD L
        MOV L,A
        MVI A,00H
        ADC H
        MOV H,A

        MOV A,M                 ;GET OUTPUT DATA FROM TABLE
        PUSH PSW

        LXI H,DATA              ;STORE INTO DATA BUFFER
        MOV A,L
        ADD D
        MOV L,A
        DCR L
        POP PSW
        MOV M,A

        INX B                   ;INCREMENT POINTER TO DATA STRING
        DCR E                   ;DECREMENT # OF DIGITS
        DCR D                   ;DECREMENT 3 DIGIT COUNT
        JNZ LOOP                ;IF NOT THIRD DIGIT THEN LOOP BACK

        LXI H,DATA
        CALL WRITE              ;DISPLAY THESE THREE DIGITS

        MOV A,E                 ;CHECK FOR LAST DIGIT OF DATA STRING
        ANA A
        JNZ DIG3

        POP H                   ;RESTORE STATES
        POP D
        POP B
        POP PSW
        RET

WRITE:
; DISPLAY 3 DIGITS
;       INPUT   HL-POINTS TO START OF DATA
;               E -COLUMN ADDRESS
;       OUTPUT    -NO REGISTERS DISTURBED
;
        PUSH PSW                ;SAVE STATES
        PUSH B
        PUSH D
        PUSH H

        MOV A,E                 ;GET ADDRESS BITS AT HIGH END OF BYTE
        RLC
        RLC
        MOV E,A
```

```
;OUTPUT FIVE ADDRESS BITS
        MVI C,5
W.LOOP: MOV A,E
        RLC                     ;ROTATE ADDRESS
        MOV E,A
        MVI A,10000000B         ;GET MSB & ENABLE CHIP SELECT BIT
        ANA E
        CALL OUT                ;OUTPUT BIT WITH CHIP SELECT
        DCR C
        JNZ W.LOOP              ;LOOP UNTIL ADDRESS IS OUT

;SIGNAL FOR A WRITE
        MVI A,00H
        CALL OUT                ;OUTPUT A ZERO BIT

;OUTPUT THE DATA
        MVI B,3                 ;3 BYTES OF DATA
DIS1:   MVI C,B                 ;8 BITS PER BYTE
        MOV D,M
DIS2:   MOV A,D                 ;ROTATE DATA
        RRC
        MOV D,A
        ANI 10000000B           ;GET NEXT BIT
        ORI 00000001B           ;DISABLE CHIP SELECT
        CALL OUT
        DCR C
        JNZ DIS2                ;LOOP UNTIL DONE WITH BYTE
        INX H
        DCR B
        JNZ DIS1                ;LOOP UNTIL DONE WITH 3 BYTES

        POP H                   ;RESTORE STATES
        POP D
        POP B
        POP PSW
        RET

OUT:
;SUBROUTINE TO OUTPUT ONE BIT TO THE MM58201
;       INPUT   A -DATA BIT IN MSB POSITION
;       OUTPUT    -NO REGISTERS DISTURBED
;                 -OUTPUT ONE BIT TO 58201

        PUSH PSW
        OUT 20H
        ORI 01000000B           ;CLOCK HIGH
        OUT 20H
        ANI 10111111B           ;CLOCK LOW
        OUT 20H
        POP PSW
        RET

DATA:   DS 3
TABLE:  DB 00111111B, 00000110B, 01011011B, 01001111B
        DB 01100110B, 01101101B, 01111101B, 00000111B
        DB 01111111B, 01101111B

        END
```

SUMMARY

The MM58201 makes it easy to interface a multiplexed LCD display to a microprocessor. It is simply a matter of connecting the display and the microprocessor to the chip, choosing a value for V_{CT}, then interfacing your program to use the subroutines listed here or similar ones. Multiplexed LCDs are the perfect way to cut down on display interconnections while still taking advantage of the LCD's low power consumption and high contrast ratio—and the MM58201 makes them easy to use.

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National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408