Internal ROM Verification For The 48-Series Microcontrollers

National Semiconductor
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INTRODUCTION

The introduction and development of semiconductor industry has also spawned associated problems in the area of testing the devices. Testing the devices is a major expenditure. As the complexity of the device increases the testing costs escalate. This is especially true for microcontrollers since they incorporate complete microcomputer systems. Verifying the program code sequences mask programmed into the microcontroller forms an integral part of testing the devices. This note briefly discusses the ideas involved in carrying out a ROM dump for the 48-series of microcontrollers from National Semiconductor. At the end of the discussion a procedure to ensure a successful ROM dump is recommended.

THE 48-SERIES MICROCONTROLLERS

The 48-series family of microcontrollers are complete 8-bit computer systems incorporating the required ALU, RAM, ROM and I/O with diverse technologies such as NMOS, CMOS and XMOS. The ideas and principles involved being the same, the discussion revolves around the INS8048 without any loss of generality.

The internal clock circuitry for the INS8048 accepts inputs from two pins viz XTAL1 and XTAL2. A crystal or an externally generated source can be connected across the two pins. The external clock frequency of the oscillator is divided by three to provide the basic clock for the system. Each clock comprises a single state and is referred to as a Machine Cycle. Five machine cycles comprise a single Instruction Cycle. To differentiate between the different machine cycles we refer to them as T1, T2, T3, T4 and T5. *Figure 1* pictorially summarizes these relationships and indicates the sequence of operations that normally take place in an instruction cycle. The microcontroller continuously generates the Address Latch Enable (ALE) signal.

ROM VERIFICATION MODE

In a nutshell the ROM verification program consists of three distinct steps. The first step involves suspending the normal instruction execution mode of the microcontroller. The second step requires presenting specific ROM location addresses to the microcontroller. The microcontroller responds by placing the contents of the addressed ROM location on the bus. Reading the contents of the ROM location from the bus constitutes the final step. Repeating this sequence of three steps allows the contents of a block of ROM locations to be verified. We now detail the three steps.

The microcontroller contains logic which disables normal instruction execution mode and forces it into a special ROM verification mode. The logic triggers the changeover to the ROM verification mode when it senses the voltage at the Enable Access (EA) pin to be greater then +6V. This condition remains active as long as the voltage at the EA pin, typically +12V, is present.

The second step in the sequence requires specific ROM locations to be addressed. The addresses are presented as in the regular mode via the ports DBO-DB7 and P20-P23. To avoid possible bus conflicts it becomes imperative to ensure that the two ports are in an input mode. This can be very simply done by resetting the device. The microcontroller transfers the address presented at DBO-DB7 and P20-P23 to the Program Counter (PC). The transfer is done in two stages. The two stage transfer is necessitated by the fact that the PC is 12 bits wide whereas the internal data bus is only byte wide. An internal control signal clocks the lower order and the higher order sections into the PC. The data transfers are done during T2 and T3 machine cycles. The higher order bits of the PC are loaded in before the lower order bits. Obviously two complete instruction cycles are minimally required to latch in the address. Extra instruction cycles can be included to provide a wider margin of safety.

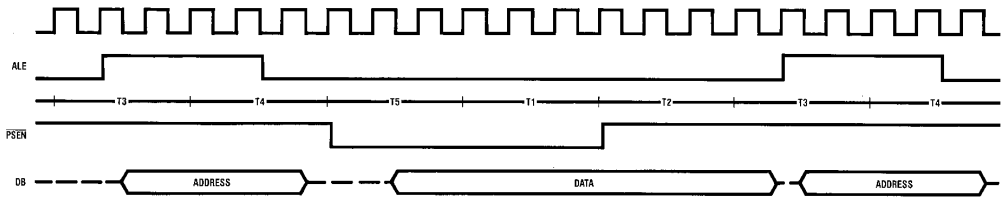

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FIGURE 1. Instruction Fetch from External Program Memory

  RRD-B30M105/Printed in U. S. A.

The third step in the sequence consists of ensuring that the address has been latched and then reading the ROM contents placed on the bus in response. The microcontroller continues to alternately latch in the two sections of the PC. This can be discontinued by pulling the $\overline{\text{RESET}}$ pin high. Care must be exercised when doing this since a transition occurring during a transfer can latch undefined addresses. A point to be borne in mind when attempting to change the state of the $\overline{\text{RESET}}$ pin is that the microcontroller does not respond immediately. The $\overline{\text{RESET}}$ pin is polled continuously during the T4 machine cycle, at the end of which the machine recognizes the reset signal. The next step consists of disabling the external circuitry holding the address on DB0-DB7 preparatory to reading the contents of the ROM location. The falling edge of the ALE signal can be used to disable the external circuitry. This is possible because of two internal conditions. First the ALE signal goes low during the T4 machine cycle and second the contents of the ROM location are enabled onto DB0-DB7 in the T1 machine cycle.

The preceding discussion highlights the different points to be borne in mind when attempting a ROM dump. The factors and their effects have been minutely described. The next section presents a ROM dump procedure.

THE RECOMMENDED ROM DUMP PROCEDURE

A procedure to guarantee reading the contents of the internal ROM locations is presented in this section. It is assumed that a Megatest or Fairchild type test setup is being used. The procedure is based upon the factors outlined in the previous section. The minimum timings obtained from it are suitably modified to include a margin of safety. The timings have been specified in machine cycle units rather then absolute timings so that they are valid over the entire frequency of operation.

1. $\overline{\text{RESET}}$ must be low before EA goes high.
2. Synchronize to the falling edge of the ALE signal. Falling edge of the ALE indicates T4, the fourth machine cycle.
3. Starting in T5 force address in with $\overline{\text{RESET}}$ low for 21 machine cycles.
4. Force address in with $\overline{\text{RESET}}$ high for 4 machine cycles.
5. Force $\overline{\text{RESET}}$ high for 12 machine cycles.
6. Force $\overline{\text{RESET}}$ high for 4 machine cycles. Data is valid on the bus till the falling edge of $\overline{\text{RESET}}$.
7. Force $\overline{\text{RESET}}$ low for 4 machine cycles.
8. Repeat steps 3 thru 7 for other addresses.

The procedure is presented pictorially *Figure 2*. *Figure 3* gives a flowchart for the recommended procedure. The timings recommended guarantee correct operation. The timings are obviously greater then the minimum required. The ROM dump circuitry is used only for verifying the ROM contents and was not designed to, in any way, be indicative of normal instruction fetch timing.

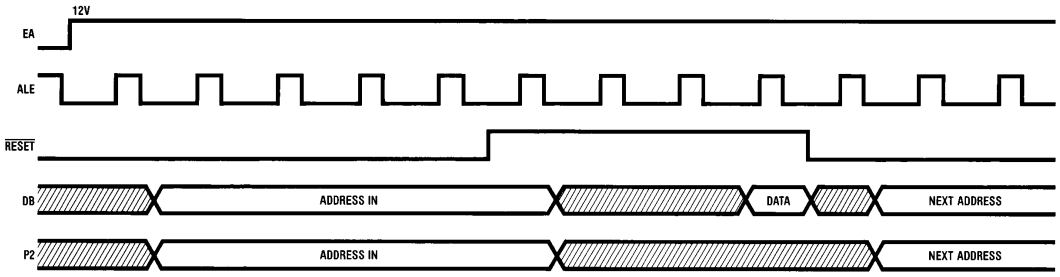

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FIGURE 2. ROM Verification Timing Diagram

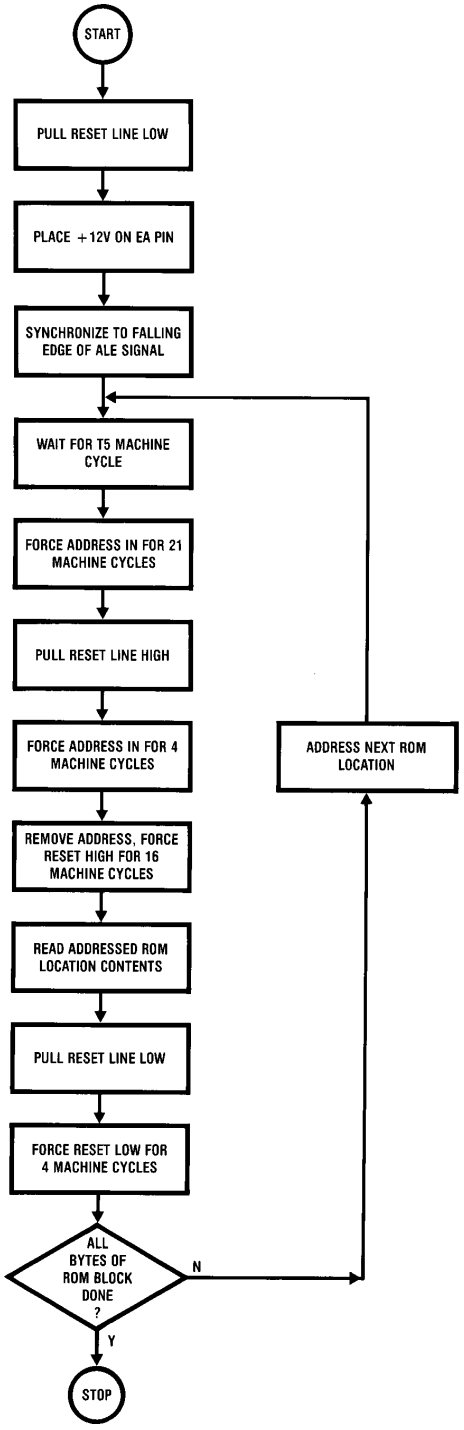

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FIGURE 3. Flowchart of the Recommended ROM Dump Procedure

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