The Subscriber Line Card in a Distributed Control Switching System

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Abstract: *This note describes a set of integrated circuit components that, together, form a major portion of a complete subscriber line card subsystem. At the center of this unique configuration is the digital line interface controller (DLIC). It is a multi-purpose system interface and control circuit for a line card of between four and thirty-two subscribers. In addition, this same circuit is useful as the interface device for trunk, special service, maintenance and administration circuit cards. Also presented are two combination CODEC and filter devices to interface the parallel bus subscriber interface port of the DLIC.*

INTRODUCTION

Distributed control switching is once again becoming a popular concept for system designs. Having gone full circle from the first fully distributed Strowger exchanges through the totally centralized architectures of the fifties and sixties, the telecommunications industry is now examining the new benefits of a distributed arrangement. Modularity, lower incremental costs, better flexibility and reliability are important features derived from the distributed approach.

This is not to say that central control is waning. Quite the opposite is true. The central processor is still important as an arbitrator and overseer. Except in some unusual cases[1], this marriage of distributed and central control is the structure most system designers are adopting and it is anticipated that this trend will continue. The central processor will manage the system at a high level while local or preprocessors perform the routine tasks associated with call processing. The primary topic of this paper is the line circuit components of this mixed control architecture. Special emphasis, however, is reserved for the control aspects of this proposed line circuit card.

A HYPOTHETICAL SWITCH

One example of a distributed architecture is shown in *Figure 1.* Line switch groups are configured as peripheral modules to a base or second level switching group. The interconnection between these two elements is a standard 128-channel TDM interface of two or four serial links plus the necessary timing and power busses. Also connected to the second level is a pair of central control processors. Again, serial data links are the interconnection choice.

The second level switch group acts as a base switching matrix for all voice (PCM), customer data and system control signals. As a typical arrangement, it is structured as a time-space-time switch with at least 35 full duplex serial access ports. For reliability and increased flexibility, the second level is normally duplicated and often replicated. This allows cross access between line switch groups and between line switch groups and the central controller.

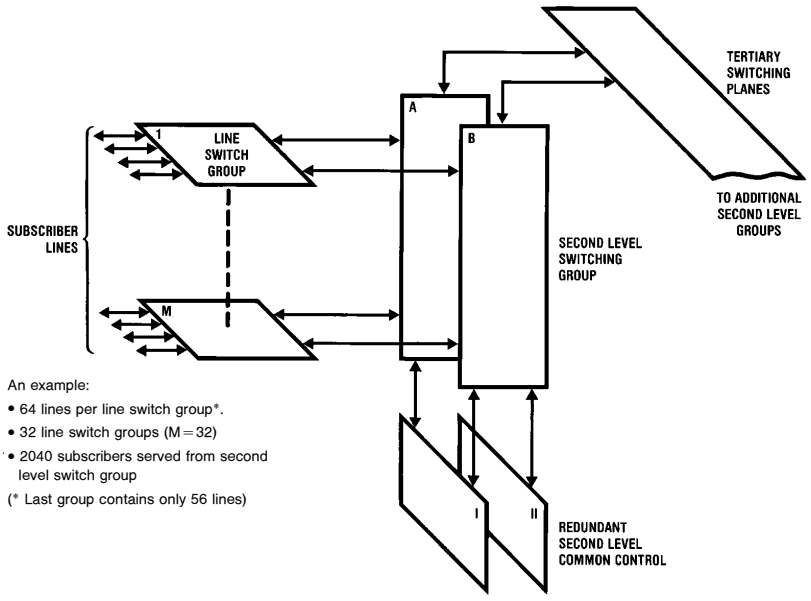

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FIGURE 1. An Integrated Voice, Data and Control Digital Line Switch

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The 35 duplex ports of each second level switching plane are connected to 32 line switch groups, two central control processors and a tertiary level of switching. This is a minimum configuration. Trunk, maintenance, administration and service circuit groups may also require access ports on the second level switch group. Of course, it is possible to contain these special circuits within the line switch groups. This would make the line groups more independent and eliminate the need for extra second level access. Remote switching would be the application that benefits the most from this latter configuration.

In this hypothetical arrangement, control information between the processors of a line switch group (local processors) and the common controller is communicated by way of the second level switching network. Four or eight software assigned channels on the TDM serial ports are reserved for general control, maintenance and subscriber card polling. These channels would use a high level control protocol (e.g., HDLC) for improved control integrity, layered message capabilities and upward compatibility with future requirements.

THE SUBSCRIBER LINE INTERFACE CARD

The subscriber line circuit card for this distributed control system is outlined in *Figure 2.* The local processor is a single-chip microprocessor controlling only one line card. This card would serve from four to thirty-two subscriber lines, although a maximum of sixteen per card is considered optimal. The local processor could be shared over several line cards, but this requires extra backplane wiring to interconnect the local processor and the circuit cards it controls (see *Figure 3*).

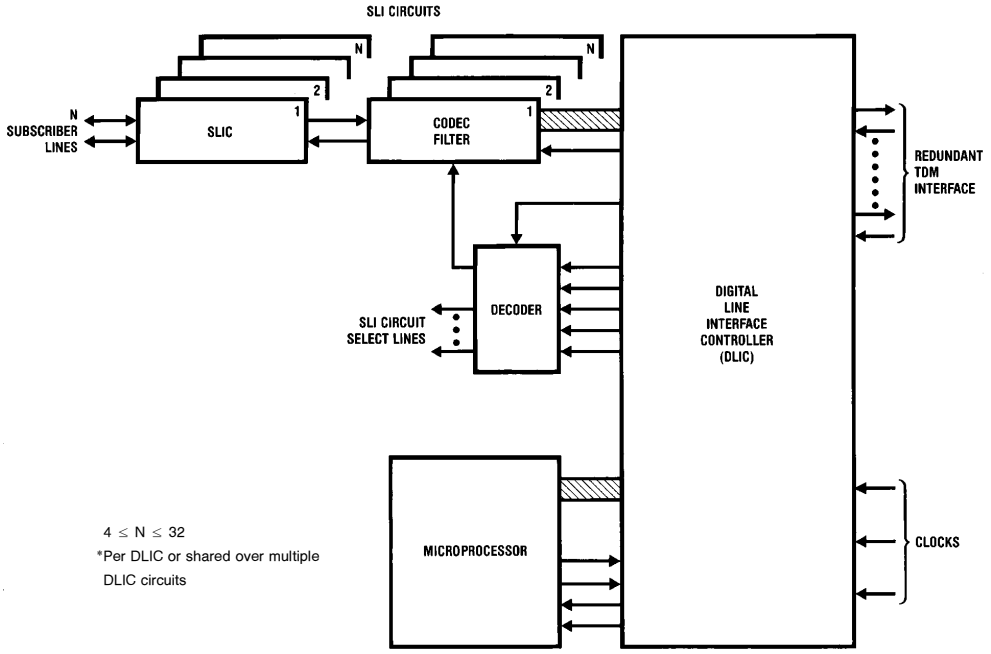

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FIGURE 2. Subscriber Line Interface Card—A Systems Approach to the Line Circuit Group

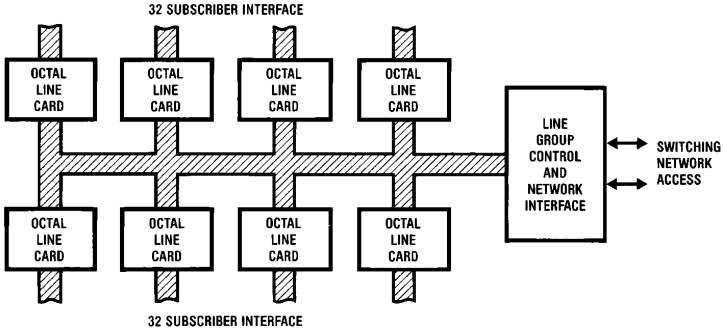

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FIGURE 3. Single Processor Line Group Arrangement

Between the per line SLIC, CODEC and filter components of the card and the serial TDM highways of the line switch group is the TP3110 or TP3120 Digital Line Interface Controller (DLIC). Either device functions as the first stage of space and time switching for the line switch group. It controls PCM, data and control communications between the system TDM serial highways, the per line CODEC, filter and SLIC circuits (or other subscriber line and special service circuit devices) and the single-chip microprocessor.

As shown in *Figures 4* and *5*, the DLIC contains two internal busses. The first is the data transport bus between the CODEC interface port and the two or four serial port transceivers. It operates in synchronism with the serial highway master clock. PCM, subscriber and signalling data are transferred through the DLIC via this bus. Control is maintained by way of instructions loaded in the on-chip time slot map memory.

The second internal bus is used exclusively by the local processor. Through this bus, the processor clears and loads the time slot map, sends or receives control information for any line circuit device and communicates line card control information to and from the central system processor. Data transfers between the synchronous and asynchronous busses are controlled by special time slot map instructions, a bus-to-bus interface register and the vectored interrupt structure of the DLIC.

The actions of the synchronous data circuit blocks within the DLIC are controlled by instructions loaded in the time slot map. Each instruction contains control, device address and transmit/receive selection information. The control code selects one of four operations: the control of data movement between serial port transceivers and the CODEC interface port, between the CODEC port and the microprocessor port, between the serial ports and the microprocessor (via an HDLC protocol circuit block) and finally a NOP condition. A fifth code, not directly loaded into the time slot map, controls a single cycle flow of data between a CODEC/filter or SLIC circuit and the microprocessor (by way of the DLIC interface register). This fifth code, when loaded by the microprocessor, operates in lieu of one time slot map NOP command. It allows the local processor to quickly control or monitor a line circuit device or function, in a simple one-shot fashion.

Contained within the DLIC is a complete HDLC receiver/transmitter. The circuit is channel assigned in the same manner used for any of the per line circuits. It will automatically monitor incoming data for an opening flag, valid DLIC address code (or a general purpose broadcast address) and a closing flag. The circuit also handles zero insertion and deletion as well as CRC accumulation and generation. Vectored interrupts are generated by the DLIC to properly control the interaction between this circuit function and the DLIC local microprocessor.

The DLIC HDLC protocol controller can be software assigned to separate and independent receive and transmit channels. Furthermore, the transmitter can simultaneously interface all serial transmit ports of the assigned transmit channel. This allows redundant control message transmission for system control information. In any arrangement, however, the total bandwidth of the duplex HDLC channel is always 64 kHz in each direction.

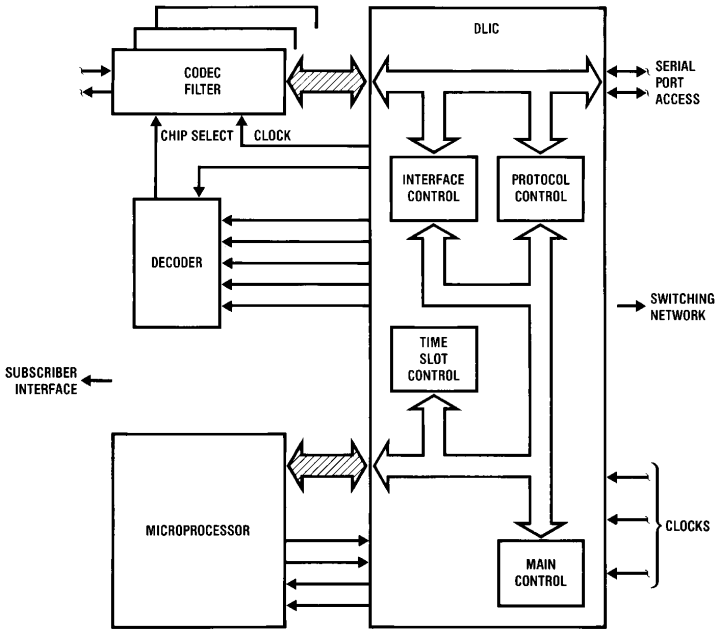

FIGURE 4. DLIC Signal Flows

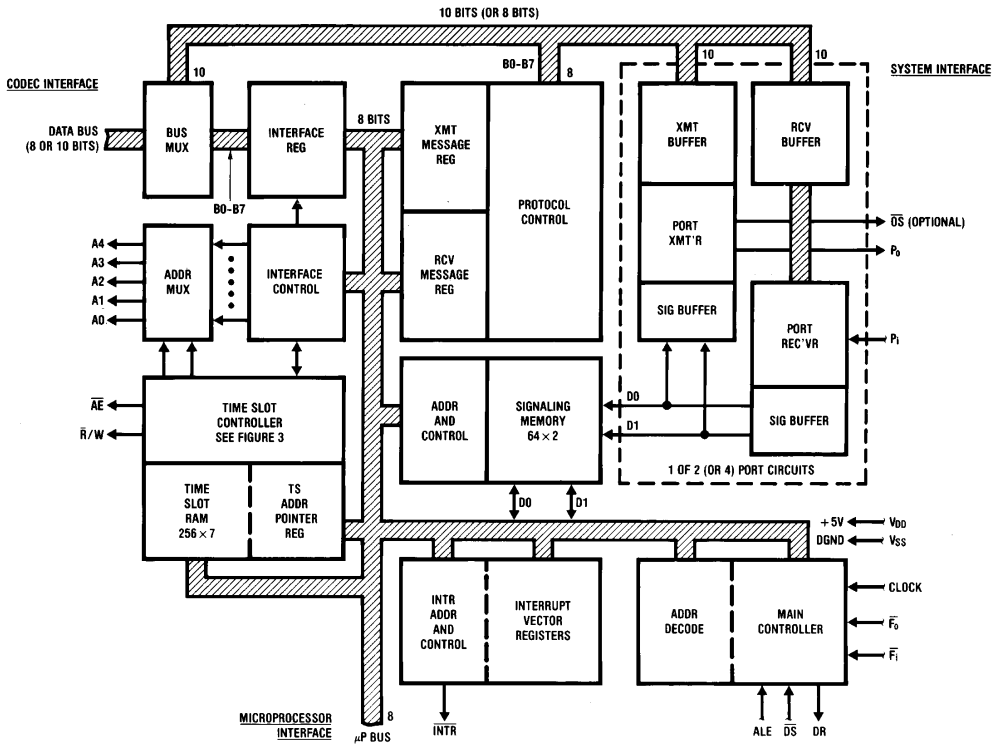

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FIGURE 5. TP3110 or TP3120 Digital Line Interface Controller (DLIC)

An interesting feature of the DLIC line card is the programmable channel bandwidth. The normal operating mode for the DLIC is with an integer number of time slots or channels of eight data bits per channel. This arrangement, for instance, would provide between six and thirty-two time division channels of 64 kHz per channel. A second arrangement provides similar channel programmability but each channel is 80 kHz wide. The 16 kHz of additional bandwidth is either directly bussed from the individual subscriber interface circuits or it is inserted and extracted through the DLIC signalling memory and local processor (see *Figure 5*). In either case, this extra data is switched with the 64 kHz voice data but can be easily extracted from the serial data stream with a DLIC circuit used as a channel demultiplexer.

Also incorporated in the DLIC is a feature known as the odd-clock mode of operation. When a system such as Bell's D series of channel bank must interface the DLIC, the DLIC can be programmed to accept the extra per frame synchronization clock cycle. This framing pulse is skipped by the DLIC so that proper frame alignment is maintained. As with all of the DLIC features, the odd clock mode is fully programmable with the standard device.

The DLIC is available in two standard arrangements. The first provides a 10-bit parallel data bus towards the subscriber interface circuits and a dual serial access towards the switching system. The second arrangement provides an 8-bit port for subscriber interface but four full duplex serial ports to interface the system TDM highways.

The parallel bus subscriber interface port of the DLIC necessitates a parallel interface CODEC/filter. The TP3051, TP3056 devices of *Figure 6* fulfill this requirement. The devices are pin compatible with each other and provide A or μ coding law CODECs with built-in switched capacitor filters. They represent the latest designs in high performance and low power double-poly silicon-gate CMOS. Both devices provide full control of operating clock frequency, digital and analog loopback testing, and power-down control. They require a minimum of external components since all sample and hold, voltage reference and auto-zero circuitry is built into the devices. Modern techniques in CODEC, filter and SLIC designs are described in several of the references listed at the end of this paper.

SUMMARY

The DLIC and associated per line circuits are actually a complete subscriber line card subsystem. As shown in *Figure 7*, an octal card can be implemented with fewer components than ever before possible. The use of a parallel data bus for the subscriber circuit interface increases overall PCM, signalling, control and subscriber data throughput without sacrificing the low power performance of the per line subscriber components. Actually, the unique features of the

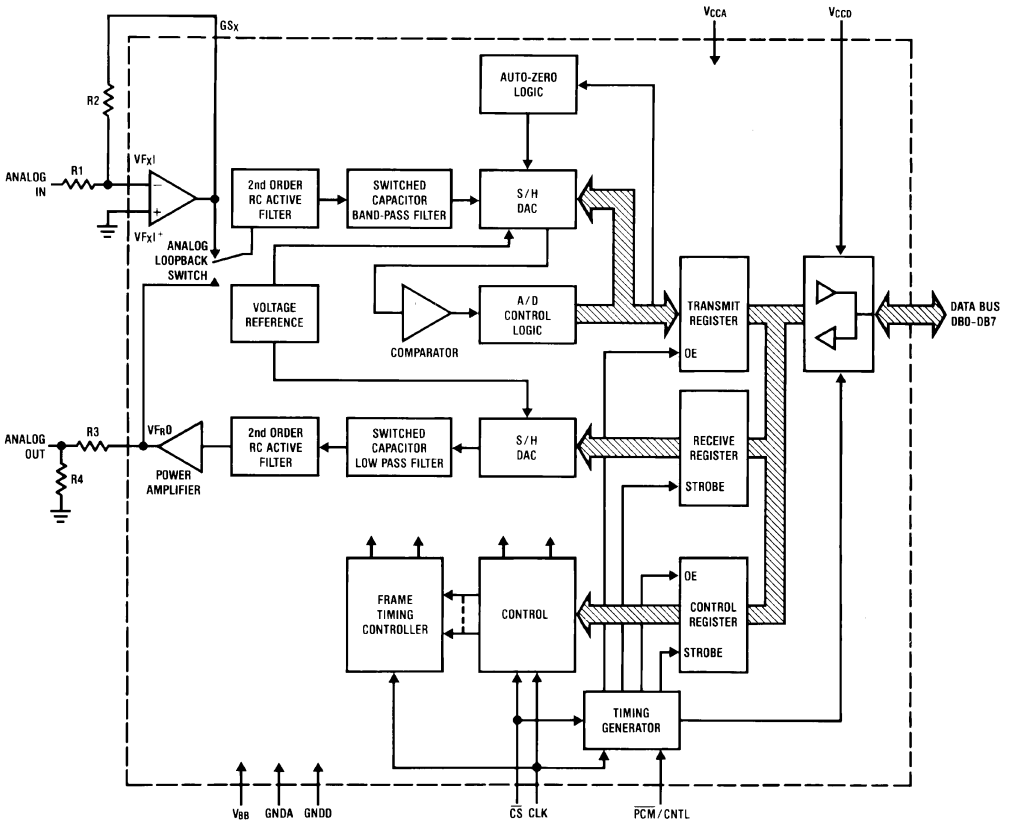

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FIGURE 6. TP3051, TP3056 Parallel I/O CODEC/Filter

DLIC allow the system designer to configure several subscriber, trunk and special service circuit cards using the DLIC as the universal system interface and control element. This approach would freeze the hardware interface between the digital switching network and the line, service, maintenance, trunk and data circuit groups without limiting the software flexibility or upward compatibility of the total system.

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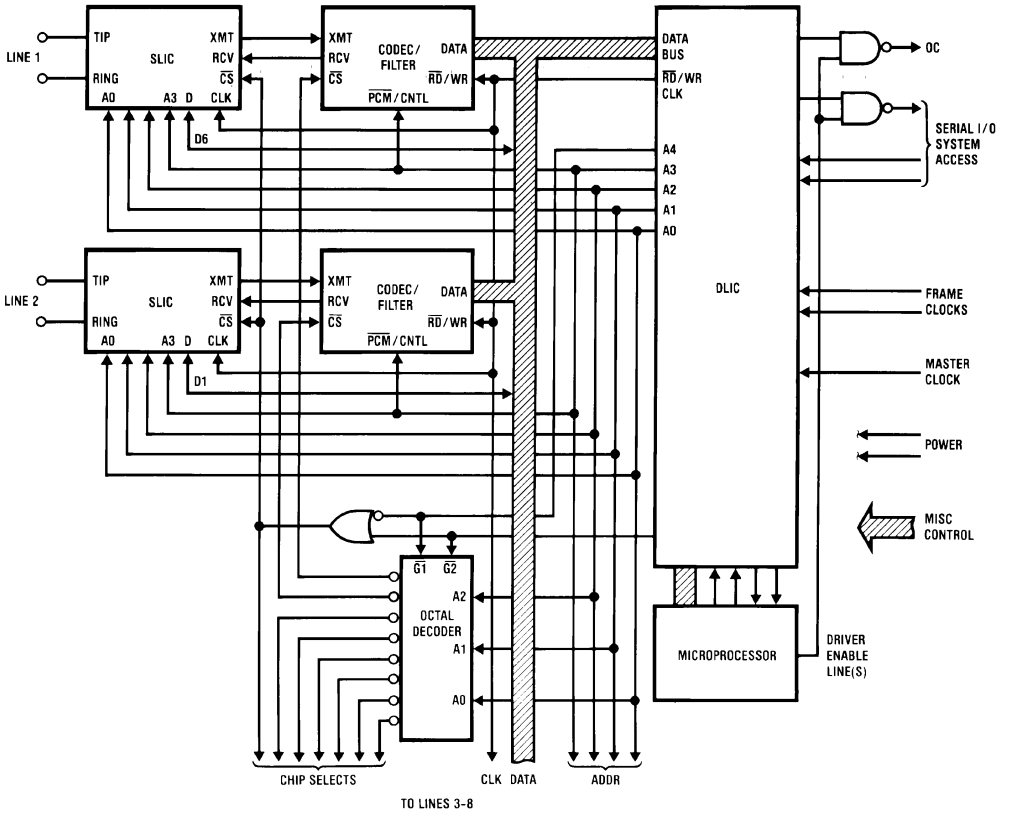

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FIGURE 7. Octal Line Card

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