DP8400s in 64-Bit Expansion

National Semiconductor
Application Note 308
Chuck Pham
October 1984

The purpose of this Application Note is to provide memory designers with detailed information on the DP8400 parallel expansion method. This method allows fast check bit generation, error detection, and error correction. A thorough understanding of the 16-bit implementation is a prerequisite. Included in this note are the following: error correction expansion matrix; detailed steps for check bit generation, error detection and error correction; an example of a single error correction; and the detailed wiring diagram for the 64-bit configuration.

The Error Correction Expansion Matrix

For a 16-bit word, the DP8400 reads data between the processor and memory, with its 16-bit bidirectional data bus connected to the memory data bus. The DP8400 uses an encoding matrix to generate six check bits from the 16 bits of data. This 16-bit matrix contains 16 unique syndrome patterns corresponding to each error location which allows the DP8400's Data Error Decoder (DED) to identify the data error location.

The DP8400 is easily expandable to other data configurations. For a 32-bit data word with seven check bits, two DP8400s are used. Three DP8400s can be used for 48 bits, four DP8400s for 64 bits, and five DP8400s for 80 bits, all with eight check bits. In order to expand the DP8400, additional check bits are required to provide the unique characteristic of the single data error syndrome. For expansion beyond 24 bits, check bits 6 and 7 (C6 and C7) are used. Note that these check bits can be configured to be always either zero or word parity, depending on the input voltage level of the Expansion Pin (XP). By rearranging all eight check bits (C0–C7) of each DP8400, we can obtain many different matrices that meet the above requirement. One of these is shown in Table I. For illustration, this matrix will be used throughout this application note to clarify the E^2C^2 expansion concept.

Check Bit Generation, Error Detection And Error Correction

CHECK BIT GENERATION (*Figure 1*)

In the Check Bit Generation mode, all four DP8400s are set to mode 0, normal write. The 64 bits of data from the system data bus are enabled into the Data Input Latches (DIL) of each DP8400. The individual Check Bit Generation (CG) of the four DP8400s then produce eight parity bits, or partial check bits, derived from the input data. (Note that all the syndrome input latches should be cleared so that only the partial check bits will pass through the Check Bit Output Latches/Buffers (COL and COB). In the normal write mode, the COBs are always enabled onto each check bit port. This allows the partial check bits to be combined externally in

TABLE I. Data Bit Error to Syndrome-Generate Matrix, 64-Bit Configuration

The partial code of device 0:

Error Locations (Data Bit Numbers)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
0	0	1	1	1	1	1	1	0	1	1	1	0	1	1	1	C0
0	0	0	1	0	0	1	0	1	1	0	1	0	1	1	1	C1
1	0	0	1	1	0	0	0	1	0	1	0	1	1	1	1	C2
0	1	1	0	0	0	0	1	1	1	1	0	1	0	1	1	C3
1	1	0	0	0	1	0	1	1	0	0	1	0	1	0	1	C4
1	1	1	0	1	1	1	0	1	0	0	0	1	1	1	0	C5
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C6
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C7

The partial code of device 1:

16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	
0	0	0	1	0	0	1	0	1	1	0	1	0	1	1	1	C1
1	1	1	0	1	1	1	0	1	0	0	0	1	1	1	0	C5
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C6
1	1	0	0	0	1	0	1	1	0	0	1	0	1	0	1	C4
0	1	1	0	0	0	0	1	1	1	1	0	1	0	1	1	C3
1	0	0	1	1	0	0	0	1	0	1	0	1	1	1	1	C2
0	0	1	1	1	1	1	1	0	1	1	1	0	1	1	1	C0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C7

The partial code of device 2:

32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C6
0	1	1	0	0	0	0	1	1	1	1	0	1	0	1	1	C3
1	1	1	0	1	1	1	0	1	0	0	0	1	1	1	0	C5
1	1	0	0	0	1	0	1	1	0	0	1	0	1	0	1	C4
1	0	0	1	1	0	0	0	1	0	1	0	1	1	1	1	C2
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C7
0	0	0	1	0	0	1	0	1	1	0	1	0	1	1	1	C1
0	0	1	1	1	1	1	1	0	1	1	1	0	1	1	1	C0

The partial code of device 3:

48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	
1	1	0	0	0	1	0	1	1	0	0	1	0	1	0	1	C4
1	1	1	0	1	1	1	0	1	0	0	0	1	1	1	0	C5
0	1	1	0	0	0	0	1	1	1	1	0	1	0	1	1	C3
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	C6
1	0	0	1	1	0	0	0	1	0	1	0	1	1	1	1	C2
0	0	1	1	1	1	1	1	0	1	1	1	0	1	1	1	C0
0	0	0	1	0	0	1	0	1	1	0	1	0	1	1	1	C1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	C7

RRD-B30M115/Printed in U. S. A.

Check Bit Generation, Error Detection And Error Correction (Continued)

the eight 74S280s' parity generators/checkers to produce eight composite check bits. Table II. shows how these check bits are generated.

Table II. Composite Check Bits Generation

Ccomp. 0 = C(0)0 ⊕ C(1)1 ⊕ C(2)6 ⊕ C(3)4
Ccomp. 1 = C(0)1 ⊕ C(1)5 ⊕ C(2)3 ⊕ C(3)5
Ccomp. 2 = C(0)2 ⊕ C(1)6 ⊕ C(2)5 ⊕ C(3)3
Ccomp. 3 = C(0)3 ⊕ C(1)4 ⊕ C(2)4 ⊕ C(3)6
Ccomp. 4 = C(0)4 ⊕ C(1)3 ⊕ C(2)2 ⊕ C(3)2
Ccomp. 5 = C(0)5 ⊕ C(1)2 ⊕ C(2)7 ⊕ C(3)0
Ccomp. 6 = C(0)6 ⊕ C(1)0 ⊕ C(2)1 ⊕ C(3)1
Ccomp. 7 = C(0)7 ⊕ C(1)7 ⊕ C(2)0 ⊕ C(3)7

Notes:

Ccomp: composite check bit.

C(X)N: the partial check bit N of device X.

(Refer to Table I. for clarification).

To aid in fast error detection during memory read cycles, these composite check bits are complemented and written into memory along with the system data. If the system data has vacated the data bus, the Output Enables ($\overline{OB0}$ and $\overline{OB1}$) must be set low so that the original data word with its eight composite check bits can be written into memory.

DETECTION MODE (*Figure 2*)

In the Detection mode, again all the DP8400s are set to mode 0, normal write, then the partial check bits derived from the memory data bits are generated in a manner similar to that described for the check bit generation mode. These partial check bits are then associatively compared with the memory check bits in the eight 74S280s to produce eight external $\overline{\text{Composite Syndrome}}$ bits. As explained in the check bit generation mode, the composite check bits are complemented before being written into memory. This shows why complemented Composite Syndrome bits are produced instead of true composite syndromes. Then, if any bits on the $\overline{\text{Composite Syndrome}}$ bus go low, this will cause the 74S30 NAND gate to go high, giving the Any Error indication. If there is no error, all $\overline{\text{Composite Syndrome}}$ bits remain high. These $\overline{\text{Syndrome}}$ bits are also latched into the 74ALS533 Octal D-type Transparent Latch (with inverted output). The composite syndromes are then fed into the syndrome ports of the DP8400s in different combinations for each, for error-type determination and/or error correction.

CORRECTION MODE: (*Figure 3*)

Upon receiving the Any Error indication during the detection mode, it takes an additional step to determine the error type and to correct a single data error. All the DP8400s should be set to mode 7B (which is mode 7 with $\overline{OES}$ high), this mode enables the external syndromes directly to the Syndrome Generator (SG) and then the Data Error Decoder (DED) of each chip. For a single data error, the input syndrome will be unique for that error location; consequently, only one DP8400 can decode that error location and correct that bit. The other three do not indicate an error and do not change their data output latch contents. This corrected data can be output to the system data bus by means of $\overline{OB0}$ and $\overline{OB1}$. The DP8400 that decodes the data error location will indicate a single data error, while all others indicate a check bit error. If there was a single check bit error or a double bit error, then all the DP8400s will indicate a check bit error or a double bit error, respectively, through their error flags.

AN EXAMPLE OF A SINGLE DATA ERROR CORRECTION

Assuming all zero data is to be written into memory, we obtain the following set of partial check bits for all DP8400s:

C0 = 0 C4 = 0
C1 = 0 C5 = 0
C2 = 1 C6 = 0
C3 = 1 C7 = 0

Note that each DP8400 contains the basic 16-bit matrix (C0—C5). Therefore, the first six partial check bits are the same for all devices; only C6 and C7 are different. With the 64-bit configuration using the above 64-bit matrix, C6 = C7 = 0 (by connecting XP directly to V_{CC}) for the devices 0, 1, and 2; and C6 = C7 = word parity (by leaving XP pin floating) for the device 3. However, with all zero data, word parity is also zero (even parity). Therefore, the above partial check bits are obtained.

Using the formulas given in Table II, the composite check bits are as follows:

Ccomp. 0 = 0 ⊕ 0 ⊕ 0 ⊕ 0 = 0
Ccomp. 1 = 0 ⊕ 0 ⊕ 1 ⊕ 0 = 1
Ccomp. 2 = 1 ⊕ 0 ⊕ 0 ⊕ 1 = 0
Ccomp. 3 = 1 ⊕ 0 ⊕ 0 ⊕ 0 = 1
Ccomp. 4 = 0 ⊕ 1 ⊕ 1 ⊕ 1 = 1
Ccomp. 5 = 0 ⊕ 1 ⊕ 0 ⊕ 0 = 1
Ccomp. 6 = 0 ⊕ 0 ⊕ 0 ⊕ 0 = 0
Ccomp. 7 = 0 ⊕ 0 ⊕ 0 ⊕ 0 = 0

Note that these composite check bits are complemented before they are written into memory. Thus, the memory check bits read later from memory are 1100 0101.

If an error has occurred in the data position 35 which is bit 3 of device 2, then the partial check bits C(3) N produced during the detection mode are as follows:

C(3)0 = 1 C(4) = 0
C(3)1 = 1 C(5) = 0
C(3)2 = 0 C(6) = 0
C(3)3 = 1 C(7) = 0

The partial check bits of other devices are unchanged. Consequently, the newly generated composite check bits (Ccomp) and the total syndrome bits are:

Bit #	Newly Generated Composite Check Bits		Memory Check Bits		$\overline{\text{Composite Syndrome}}$
0	0	⊕	1	=	1
1	1	⊕	0	=	1
2	0	⊕	1	=	1
3	1	⊕	0	=	1
4	0	⊕	0	=	0
5	1	⊕	0	=	1
6	1	⊕	1	=	0
7	1	⊕	1	=	0

Check Bit Generation, Error Detection And Error Correction (Continued)

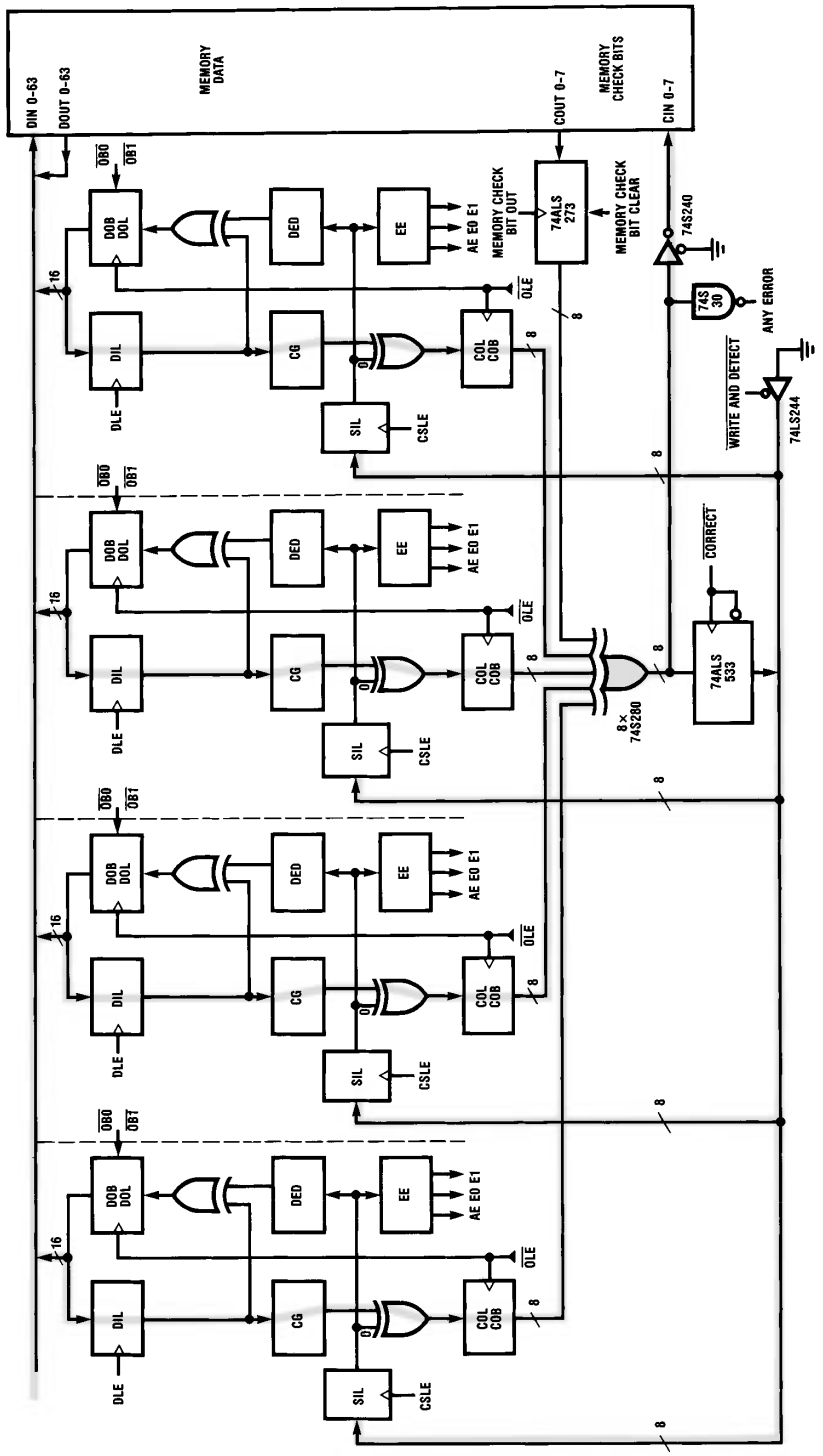


FIGURE 1. E²C² Simplified Block Diagram—64-bit Parallel Expansion, Check-Bit Generation

Check Bit Generation, Error Detection And Error Correction (Continued)

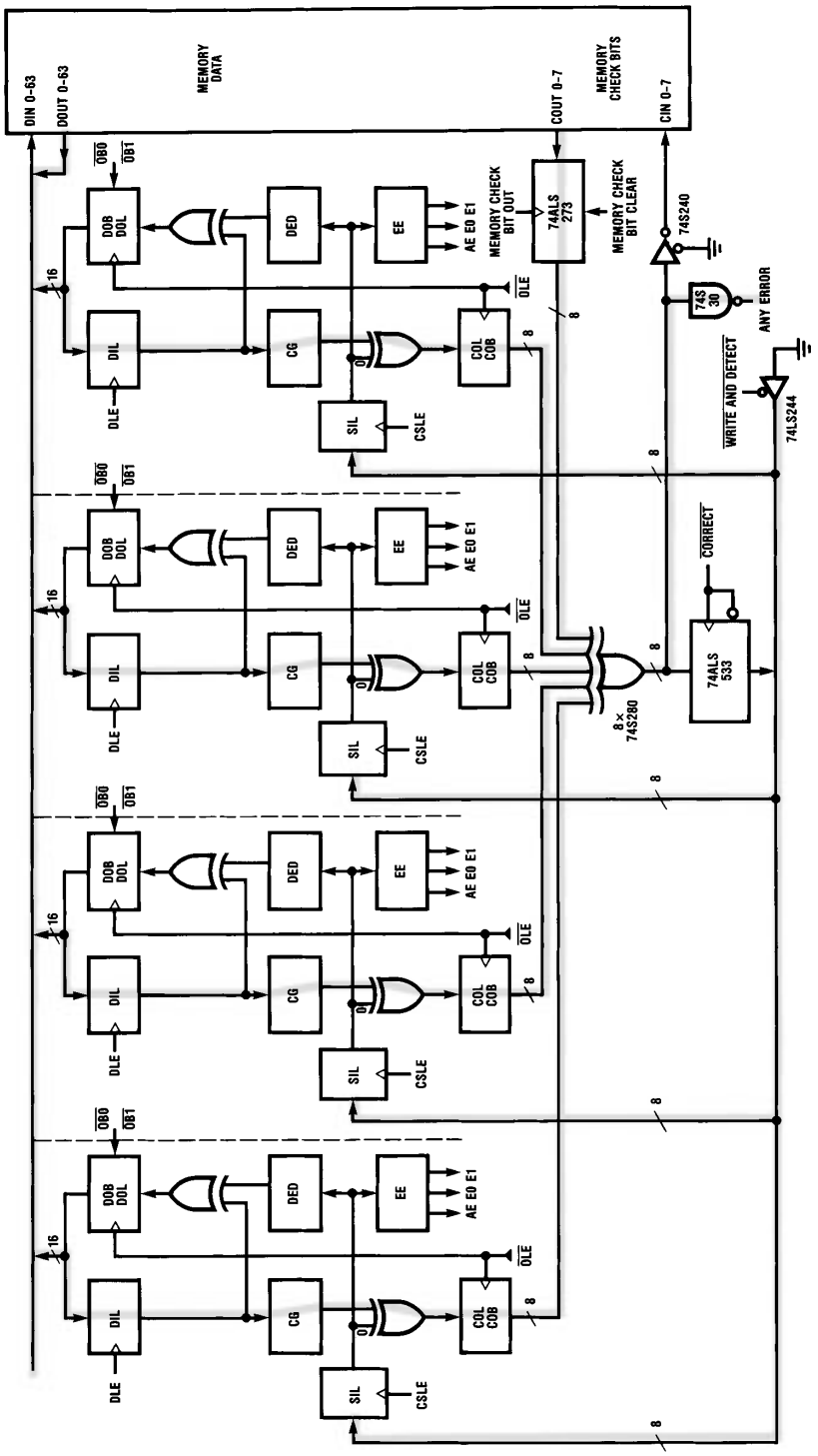


FIGURE 2. E²C² Simplified Block Diagram — 64-Bit Parallel Expansion, Error Detection

Check Bit Generation, Error Detection And Error Correction (Continued)

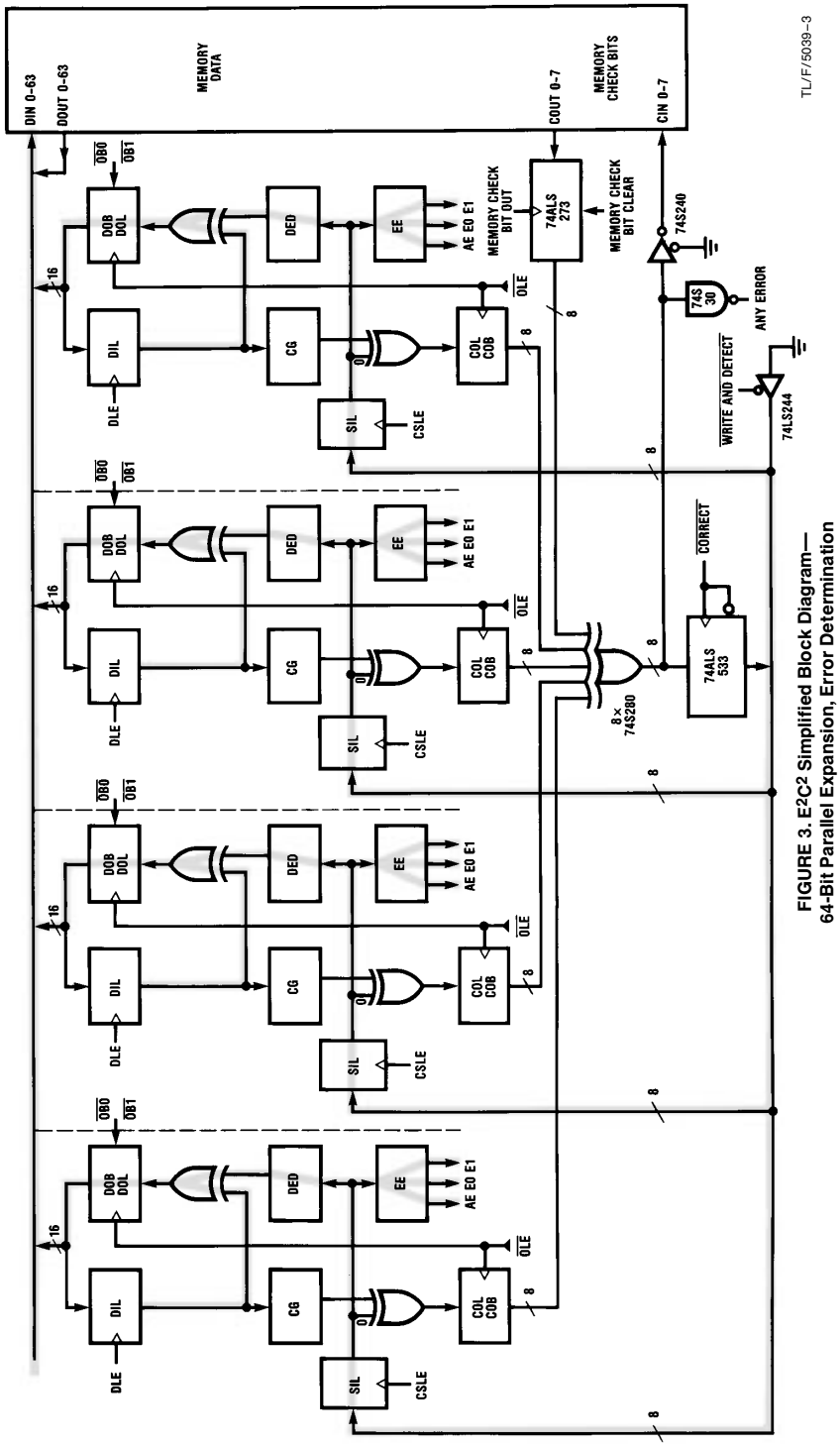


FIGURE 3. E²C² Simplified Block Diagram—64-Bit Parallel Expansion, Error Determination and Correction

Check Bit Generation, Error Detection And Error Correction (Continued)

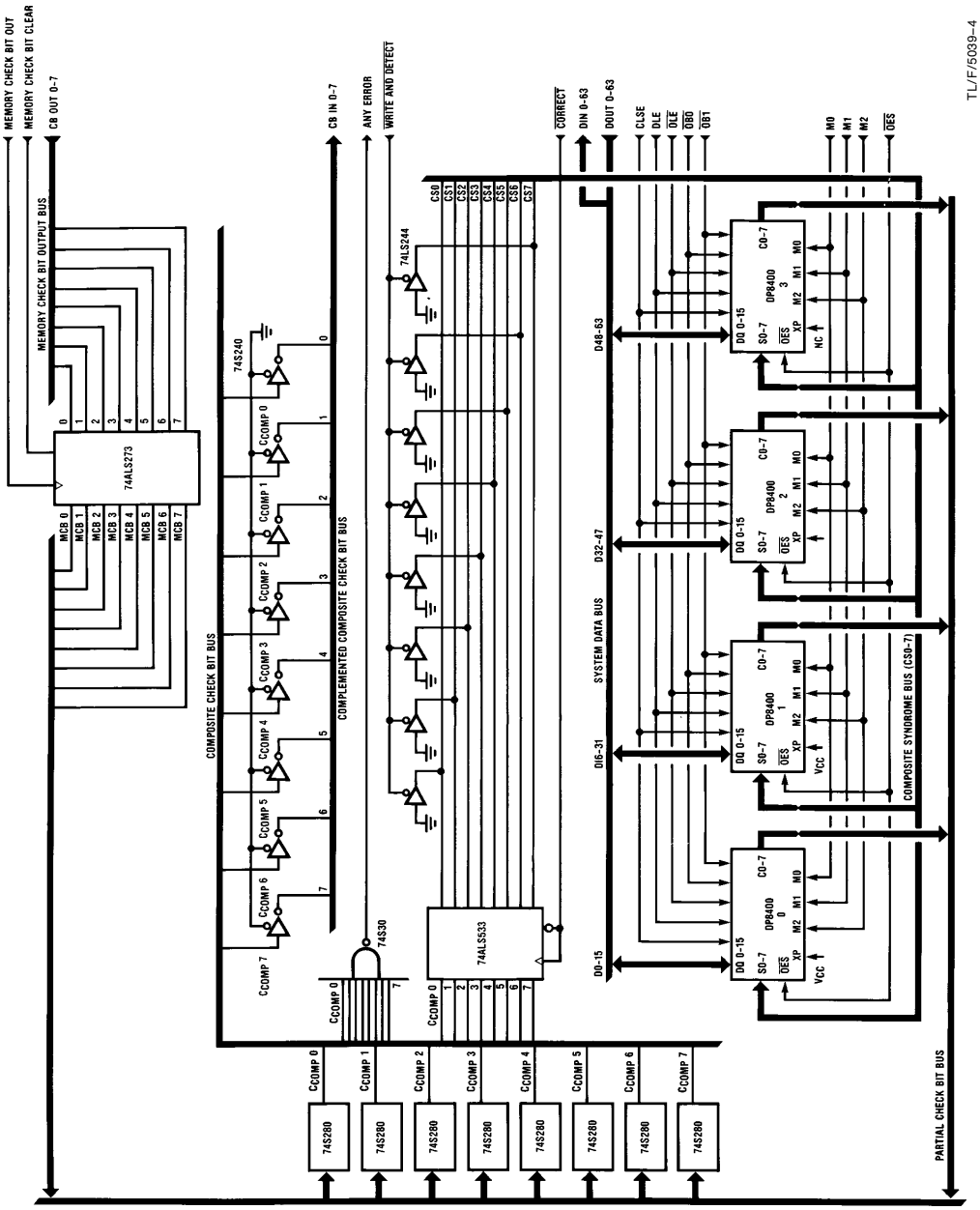
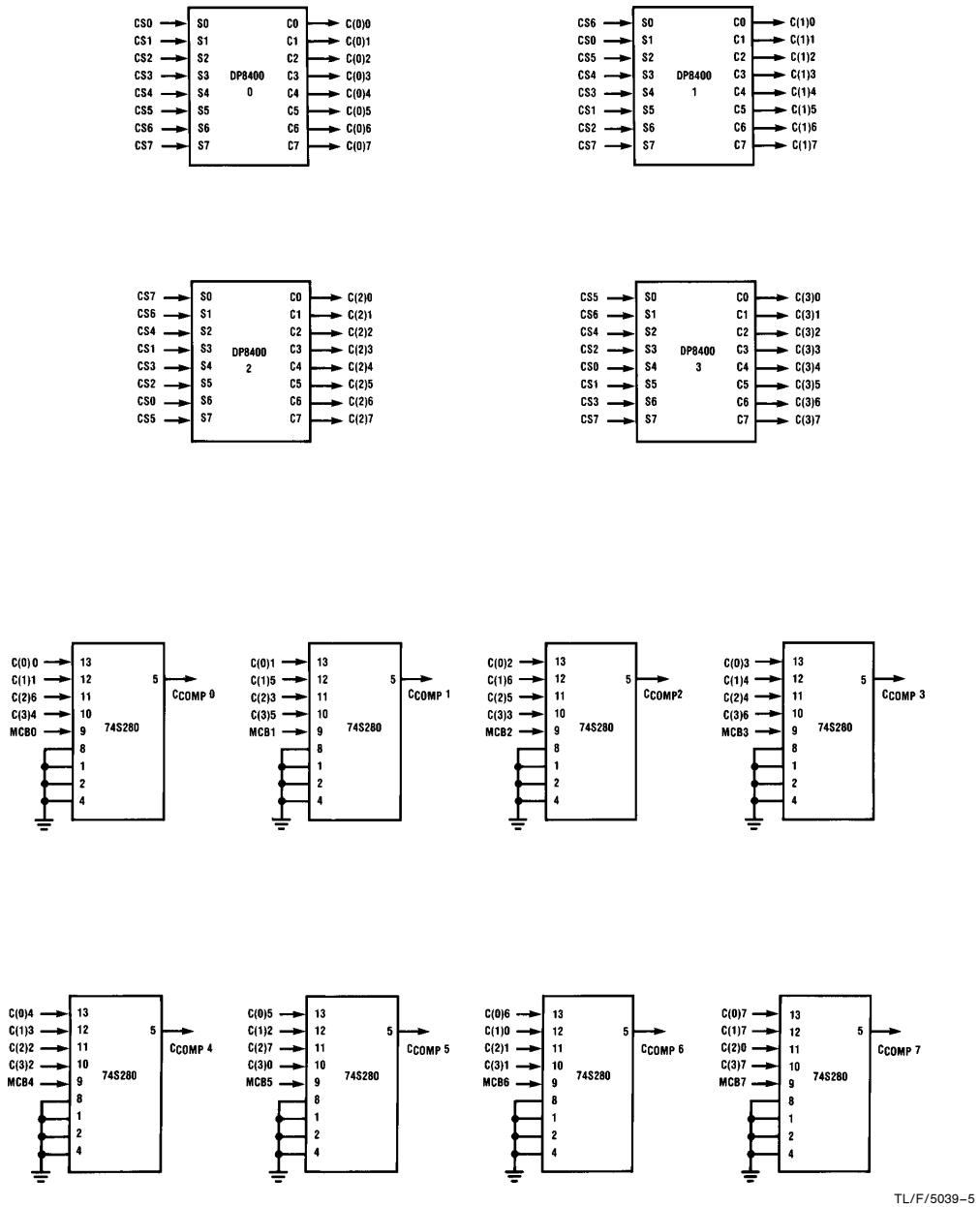


FIGURE 4. E2C2 64-Bit Parallel Expansion, Detailed Block Diagram

Check Bit Generation, Error Detection And Error Correction (Continued)



TL/F/5039–5

FIGURE 5. E²C² 64-Bit Parallel Expansion

Check Bit Generation, Error Detection And Error Correction (Continued)

The composite syndrome 11010000 is that of the error location 35. Since the syndrome is unique and fed reordered to each DP8400, only device 2 will recognize this syndrome pattern and complement its data bit 3. Then the corrected data can be output to the system data bus when $\overline{OB0}$ and $\overline{OB1}$ of all four DP8400s go low. Devices 0, 1, and 3 all output the same data they received from memory. Only device 2 changes its (erroneous) data. Refer to *Figure 6* below for the timing diagrams of a memory write and memory read cycle (detect then correct).

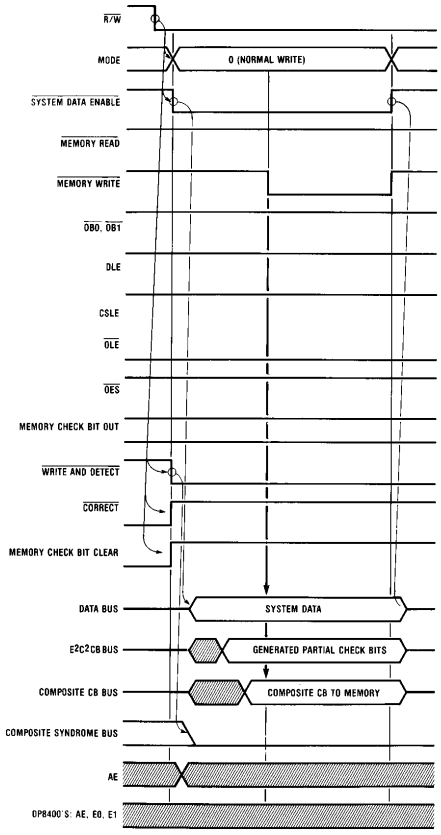
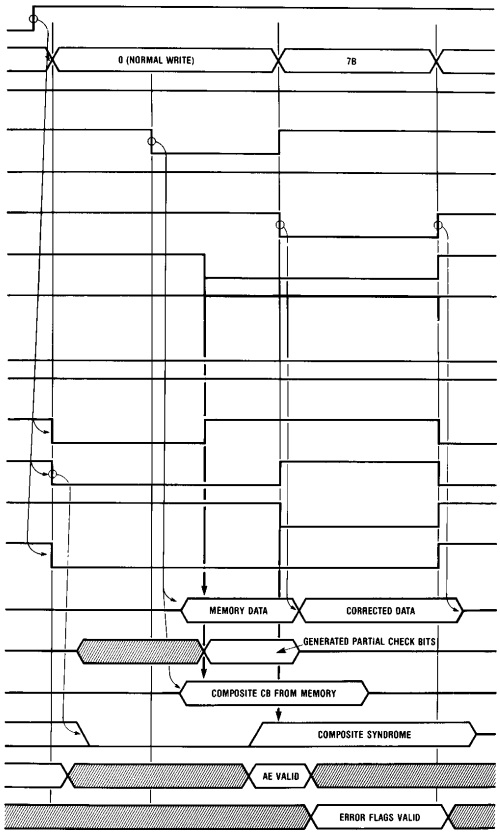


FIGURE 6A. E²C² 64-Bit Parallel Expansion Memory Write Cycle



TL/F/5039–6

FIGURE 6B. E²C² 64-Bit Parallel Expansion Memory Read Cycle (Detect Then Correct)

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408