The New MICRO-DAC™ Product Line for Microprocessor Systems

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A second generation of the popular MDAC (or multiplying DAC) is now available which has been designed to provide an easy interface to microprocessor systems. These new MICRO-DAC products are low power drain CMOS converters, which typically require only 0.5 mA supply current (2 mA max) and draw only approximately 600 μA from a 10 V_{DC} reference supply.

The basic problems which are inherent in bipolar designs are not present in this CMOS product. CMOS devices have nearly infinite current gain, therefore there are no β or α errors in the design. Also, there is no analogous term to offset voltage in these products, rather, an ON CMOS switch is nothing more than a small resistor which can be controlled by device geometry. To avoid the temperature coefficient and piezoresistive problems of diffused resistors, silicon chromium thin-film resistors are used.

These resistors track within 1 ppm/°C, which insures excellent temperature tracking characteristics. Also, the feedback resistor, which is needed with an external op amp, is provided on the chip, which insures a low temperature coefficient of the gain or full-scale reading of the DAC.

Bipolar designs in the 10-bit region can have a power dissipation of 300 mW. Unless extreme care is taken to insure an almost perfect thermal die layout, it is very possible to have a 1°C temperature gradient on the die. If a diffused resistor ladder were to be used in the presence of this gradient, it will cause a 0.15% error. This means that all of the allowable error in a 10-bit DAC will be used up due to this thermal gradient. From this, it is obvious that the CMOS DAC, with its combination of a low temperature coefficient thin-film resistor ladder and an on-chip power dissipation of 30 mW max, will overcome one of the major problems in bipolar designs.

DATA FORMATS AND DATA BUFFERS

From the digital viewpoint, a DAC seems little more than a *write only memory* where the information in the memory is made available as the analog output voltage. Problems arise concerning data formatting. Is the data to be left-justified (fractional binary) or right-justified (positionally weighted binary)? Also, updating a 10-bit DAC from an 8-bit bus can cause transient output voltage errors until the complete new word has been transferred.

The data format options are shown in *Figure 1*. Early converter manufacturers favored fractional binary, and this has caused the MSB to be labeled as ''Bit 1'' on DAC products. As may be expected, this convention has been changed in the new converter products to match the notation of the bits on the data bus of μPs. People supplying converter products still favor the fractional binary format, but it appears that the user groups are approximately split on the question of which to use.

MSB									**LSB**
1	0	1	0	1	0	1	0	2	0
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}
1/2	1/4	1/8	1/16	1/32	1/64	1/128	1/256	1/512	1/1024

V_{OUT} = (fractional binary number) × V_{REF}

a) Left-Justified Data

MSB									**LSB**
1	0	1	0	1	0	1	0	1	0
2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
512	256	128	64	32	16	8	4	2	1

V_{OUT} = (positionally weighted binary number) × V_{LSB}
where $V_{LSB} = V_{REF}/1024$

b) Right-Justified Data

FIGURE 1. Data Formats for a 10-Bit Converter

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Both of these problems go away with the addition of flexible input digital data buffers (latches) which allow complete applications flexibility (*Figure 2*). For example, with two levels of input buffers (double buffering), the DAC Register has the job of holding the current digital data which is being converted, and the other, the Input Latch, is then available to acquire new digital data which will eventually be used to update the DAC. This allows 10 bits to be assembled with two data bytes from the μP and prevents the transient output error at updating time. Further, even with 16-bit μPs, double buffering is necessary to allow many DACs to be updated simultaneously. This is useful to establish the proper conditions for a next test, or to allow new system parameters to be set up at the same time.

Data formatting is handled by providing flexibility in the way the digital data is entered into the Input Latch. To allow operation with either an 8-bit (two write cycles) or a 16-bit (one write cycle) data bus, all 10 locations of the Input Latch are enabled on the first write cycle from the μP. Then, depending on the data format, the next write cycle, if used, will overwrite two of these locations with the proper data.

Two product options are offered, as shown in the matrix of *Figure 3*. Each of the 2 functional options is offered in accuracies of 8, 9 or 10 bits. The 20 pin 0.3″ wide packages are used for fixed left-justified data format. The 24 pin part is pin programmable for either right- or left-justified data.

All of these options make use of the standard μP control signals, such as $\overline{CS}$ and $\overline{WR}$, and the data on the bus can be read by the converter in a standard write cycle. As expected, the internal CMOS logic is faster for higher supply voltages, and this effect on the write strobe width is shown in *Figure 4*.

The internal transfer of the digital data from the Input Latch to the DAC Register can be controlled in three ways: 1) automatic transfer when the second byte occurs, 2) use the μP to control the transfer—this signal can update several DACs, if desired, or 3) use an external strobe to cause the transfer.

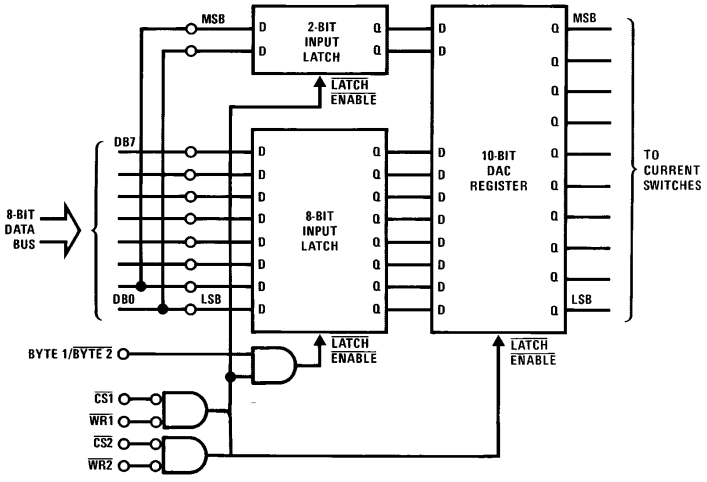

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FIGURE 2. Double-Buffering the Digital Input Data

Part #	Accuracy (Bits)	Pin	Description
DAC1000	10	24	Has All Logic Features
DAC1001	9		
DAC1002	8		
DAC1006	10	20	For Left-Justified Data
DAC1007	9		
DAC1008	8		

FIGURE 3. MICRO-DAC Product Options

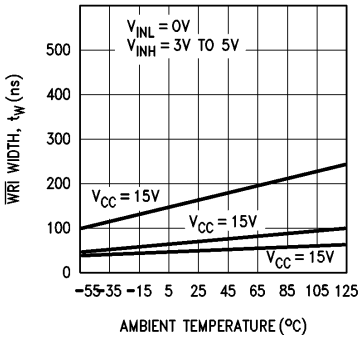

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FIGURE 4. Write Strobe as a Function of the V_{CC} Supply Voltage and Temperature

MEETING T²L INPUT VOLTAGE SPECS WITH CMOS

Logic compatibility is aided by having the CMOS logic inputs meet T²L voltage level specs. A special biasing circuit makes use of the parasitic NPN bipolar transistors which are available on the CMOS chip (*Figure 5*). These bipolar devices will supply base-emitter voltage, V_{BE}, references for the digital inputs. By using this circuit, these CMOS MICRO-DAC products have the same input voltage threshold, 2 V_{BE}, as exists with standard T²L!

The details of this bias referencing circuit are shown in *Figure 6*. Notice that the reference N-channel transistor, Q1, is tied in a feedback loop, which forces it to conduct the 60 μA which is supplied to its drain. The gate voltage of the transistor thus biases at V_N, the voltage which is necessary for Q1 to conduct the 60 μA. The three NPN transistors add 3 V_{BE} to this voltage. The output emitter-follower, Q2, causes a loss of 1 V_{BE} and produces a voltage reference of 2 V_{BE} + V_N to be used by all of the logic input circuits. One of these input stages, Q3, is also shown on this figure. Note that the digital input is applied to the source of Q3. This transistor has the same geometry as Q1, and also has a 60 μA current source feeding its drain. Due to device matching, Q3 will therefore conduct when the logic input voltage is equal to 2 V_{BE}, and this is the logic threshold *voltage of standard T²L logic gates.* The variation of this logic threshold with supply voltage and temperature is shown in *Figure 7*. This input circuitry may surprise a new user because here is a CMOS part which outputs 60 μA of current at the digital input leads when pulled to the low voltage state!

ON THE ANALOG SIDE

Conceptually, it is easiest to think of DACs which use binary weighted resistors. Unfortunately, the large resistance ratios which result have limited this design approach to 4-bit converters where the ratio is 16 to 1.

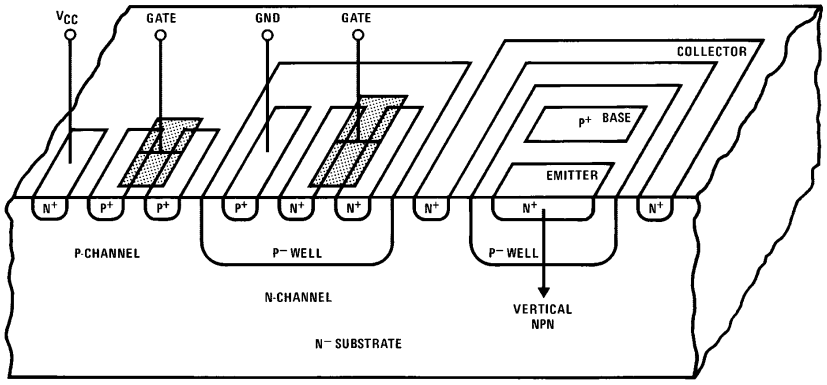

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FIGURE 5. A Simplified Wafer Cross Section Showing the CMOS FETs and the NPN Bipolar Transistor

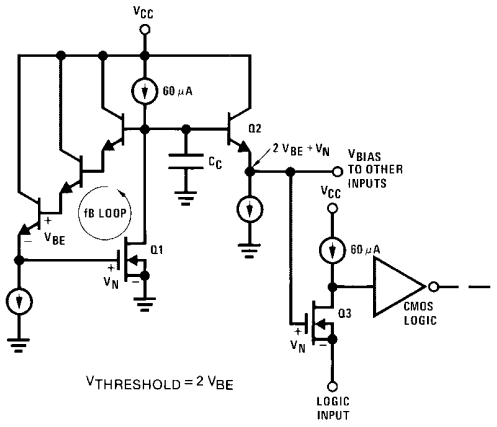

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FIGURE 6. Basic Logic Threshold Loop

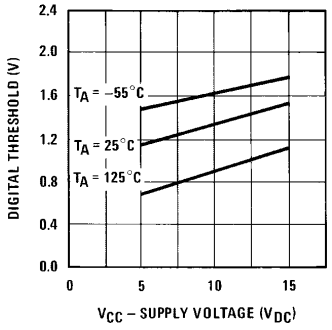

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FIGURE 7. Digital Input Threshold vs Supply Voltage

The R-2R resistor ladder is an old trick to keep the resistors always in a 2:1 ratio, independent of the resolution of the converter. Three variations on the use of these ladders exist which depend on whether voltages or currents are being switched, and whether the output from the ladder is a current or a voltage. The current-switching, current-mode, R-2R ladder is used in the MICRO-DAC products and is shown in *Figure 8*. This is the heart of the analog section of the DAC and, as can be seen, it consists of all passive components. This inherent simplicity is the strong point of this design approach. The main DAC design problem is to provide a relatively straightforward function—but to do it with a very high accuracy!

Proper operation of the ladder requires that all of the 2R legs always go to exactly 0 V_{DC} (ground). Therefore, offset voltage, V_{OS}, of the external op amp cannot be tolerated, as every millivolt of V_{OS} will introduce 0.01% of added linearity error. At first this seems unusually sensitive, until it becomes clear that 1 mV is 0.01% of the 10V reference!

High resolution converters of high accuracy require attention to every detail in an application to achieve the available performance which is inherent in the part.

Also note that no ''DC balancing'' resistance should be used in the grounded positive input lead of the op amp, *Figure 9*. This resistance and the input current of the op amp can also create errors. The low input biasing current of the BI-FET™ op amps makes these ideal for use in DAC current-to-voltage applications. The V_{OS} of the op amp should be adjusted with a digital input of all zeros to force I_{OUT1} = 0 mA. A 1 kΩ resistor can be temporarily connected from the inverting input to ground (*Figure 9*) to provide a DC gain of approximately 15 to the V_{OS} of the op amp and make the zeroing easier to sense. Note also that the feedback resistor for the op amp is provided on the chip and should always be used. This guarantees both a good initial matching and this resistor will match the R-2R ladder over temperature changes.

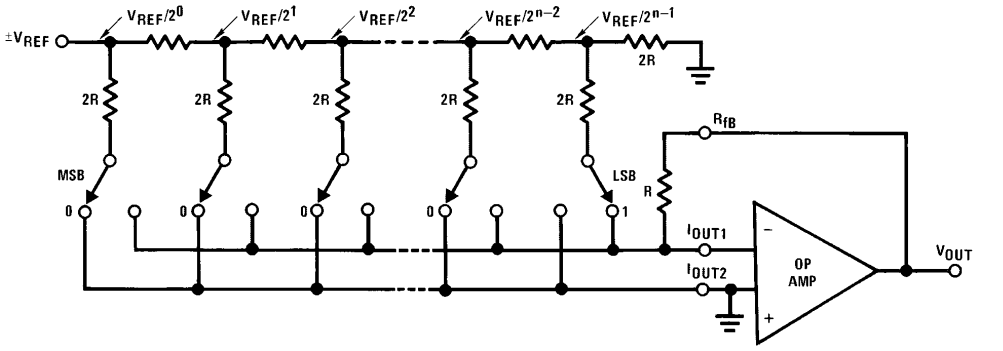

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FIGURE 8. The Current Switching—Current Mode R-2R Ladder of the MICRO-DAC Products

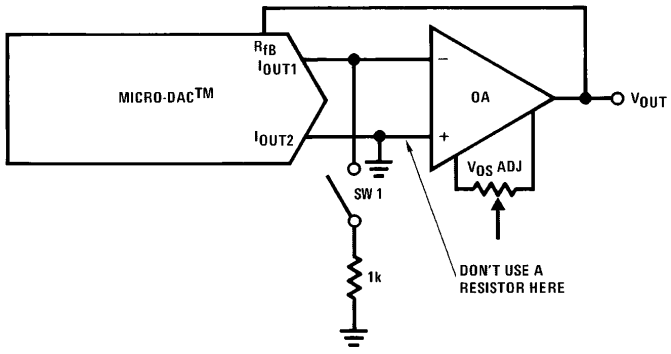

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FIGURE 9. Adjusting the V_{OS} of the Op Amp

The internal details of the SPDT current-mode switches are shown in *Figure 10*. The N-channel transistors are driven by the V_{CC} supply voltage which is used for the part. Operation at 15 V_{DC} reduces the switch ON resistance as compared to the use of a 5 V_{DC} supply and, therefore, improves the performance of the DAC. The change in gain and linearity errors as a function of the supply voltage are shown in *Figure 11*. These curves are normalized to the performance with a 15 V_{DC} power supply and show the degradation as the supply voltage is reduced.

The usefulness of a DAC can be determined by noting the linearity errors which result as the magnitude of the reference voltage is reduced. This is important for multiplication applications and other uses which require small values of reference voltage. In the case of the MICRO-DAC converters, reducing the reference voltage from 10V to 1V results in a linearity error change of approximately 0.005%.

END POINT GUARANTEE VS BEST-STRAIGHT-LINE

Suppliers of DACs like to use a Best-Fit Straight-Line linearity guarantee to increase yields. Unfortunately, this technique is based upon iterating the zero and the full-scale adjustments to optimumly split the errors to be equidistant from a straight line. To the user, this means that each DAC has to go through a rather sophisticated adjustment procedure to home in on this best approximation—which is different for each part.

The alternative specification is called an End Point Spec. This means that after a standard zeroing of the V_{OS} of the op amp (the DAC itself doesn't require a zero adjustment, so a pre-trimmed low V_{OS} op amp can eliminate this adjustment) and a standard full-scale adjustment, the linearity of *each of the 1024 steps* is within spec! This is a large benefit to the DAC user.

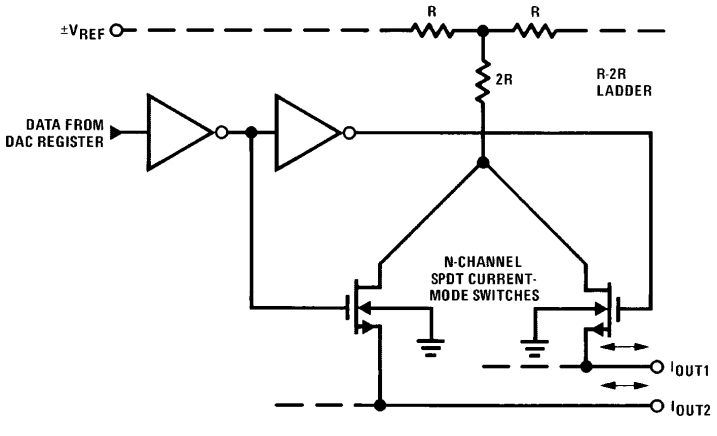

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FIGURE 10. The Basic DAC Circuit

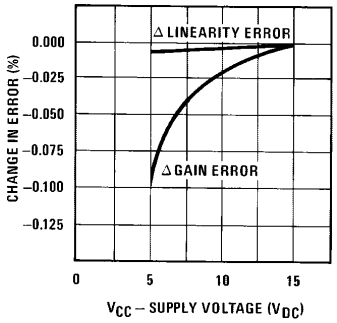

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FIGURE 11. Effects of Supply Voltage on Linearity and Gain Error

The differences between these specification techniques are shown in *Figure 12*. A DAC with an error of 1 LSB and failing the end point test is shown in *Figure 12*. Notice that by readjusting the full-scale, the error of this DAC can be optimumly split to be symmetrically located about a Best-Fit Straight-Line. This search for the optimum end point readjustments has to be done by the user for each individual DAC. The end point spec allows standard zero and full-scale adjustment procedures to be used in PC board assembly, and no time-consuming searching or special readjusting techniques need to be used. Further, it can be seen that the end point spec is a more stringent requirement on the linearity of the DAC.

SUMMARY

The CMOS current-switching DACs have evolved from the unbuffered MDACs to the μP compatible double-buffered MICRO-DAC products. Many non-DAC applications have been generated for the MDACs and we now have the new possibility of μP controlled gain, attenuators and multipliers—all of which easily interface to a μP system. These new low cost monolithic DACs will open up many new applications in the modern electronic systems.

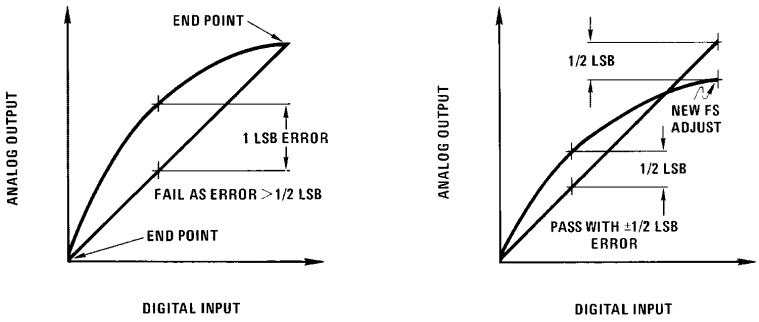

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FIGURE 12. Best-Straight-Line vs End Points Specs

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