Data Acquisition Using the ADC0816 and ADC0817 8-Bit A/D Converter with On-Chip 16 Channel Multiplexer

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I. Introduction

The ADC0816 and ADC0817, CMOS 16-Channel Data Acquisition devices are selectable multi-input 8-bit A/D converters. In addition to a standard 8-bit successive approximation type A/D converter, these devices contain a 16 channel analog multiplexer with 4-bit latched address inputs. They include much of the circuitry required to build an 8-bit accurate, medium through-put data acquisition system.

These two converters are similar to the ADC0808/ADC0809 A/D converters except that the ADC0816/ADC0817 have 16 analog inputs instead of 8, and the multiplexer output and the A/D comparator input are externally available. (The ADC0808/ADC0809 connect these internally.) This feature is useful when connecting signal processing circuitry to the A/D. Also the ADC0816/ADC0817 have an expansion control pin to allow addition of more multiplexers, hence more input channels.

The ADC0816 is identical to the ADC0817 except for accuracy. The ADC0816 is the more accurate part, having a total unadjusted error of $\pm\frac{1}{2}$ LSB. The ADC0817 has a total unadjusted error ± 1 LSB. In many applications where a slightly lower accuracy is tolerable, the ADC0817 represents a more economical solution.

II. Functional Description

The ADC0816/ADC0817 can be subdivided into two major functional blocks; a multiplexer/latch and an A/D converter, *Figure 1*. The multiplexer/latch is composed of a 16 channel multiplexer, a 4 bit channel select register, and some channel select decoding circuitry.

The channel select address is loaded on the positive transition of the Address Latch Enable (ALE) input. *Figure 2*

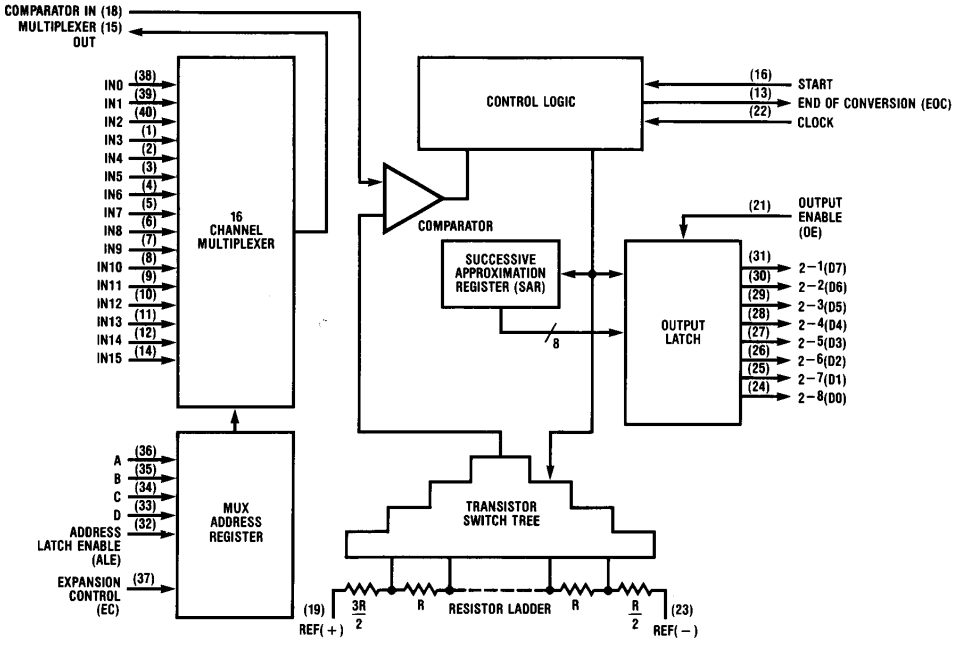

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FIGURE 1. ADC0816/ADC0817 Functional Block Diagram

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shows this addressing scheme. A multiplexer enable pin called Expansion Control (EC) is also provided. Taking this pin low will disable the on chip multiplexer, allowing other multiplexers to be used, thus expanding the number of inputs.

Address				Expansion	Selected
D	C	B	A	Control	Channel
0	0	0	0	1	IN0
0	0	0	1	1	IN1
0	0	1	0	1	IN2
0	0	1	1	1	IN3
0	1	0	0	1	IN4
0	1	0	1	1	IN5
0	1	1	0	1	IN6
0	1	1	1	1	IN7
1	0	0	0	1	IN8
1	0	0	1	1	IN9
1	0	1	0	1	IN10
1	0	1	1	1	IN11
1	1	0	0	1	IN12
1	1	0	1	1	IN13
1	1	1	0	1	IN14
1	1	1	1	1	IN15
X	X	X	X	0	NONE

FIGURE 2. Analog Input Selection Table

The output of the multiplexer usually feeds the input of the second major functional block, the A/D converter. This converter is a successive approximation type converter that is composed of a comparator, 256R type resistor ladder, successive approximation register (SAR), control logic, and output data latch.

Under normal operation the control logic of the A/D will first detect a positive going pulse on the START input. On the rising edge of this pulse the internal registers are cleared, and will remain clear as long as START is high. When the START input goes low, the conversion is initiated. The control logic will cycle to the beginning of the next approximation cycle at which time End of Conversion goes low and the conversion is started. During a conversion, the control logic will select a tap on the resistor ladder, and route the signal through a transistor switch tree to the input of the comparator. The comparator will decide whether this tap voltage is higher or lower than the input signal and indicate this to the control logic. The control logic then decides which tap is to be selected next. Meanwhile, the SAR maintains a record of the conversion's progress. This algorithm takes 8 clock periods per approximation and requires 8 approximations to convert 8 bits. Thus 64 clock periods are required for a complete conversion.

Once the entire conversion is completed the data in the SAR is loaded into the output register. This is a TRI-STATE® register which requires that its outputs be enabled by rising the Output Enable (OE or TRI-STATE) input. The data can then be read by the controlling logic.

During operation, the EOC output must be monitored to determine whether the device is actively converting or is ready to output data. Once the channel address is loaded, a positive going pulse on START will start the conversion and cause EOC to fall. When EOC goes high again the data is ready to be read, which, as was previously stated, is accomplished by raising the OE input. The data can be read any time prior to one clock period before the completion of the *next* conversion. The ADC0816/ADC0817 timing is shown in *Figure 3*. (See data sheet for exact specifications.)

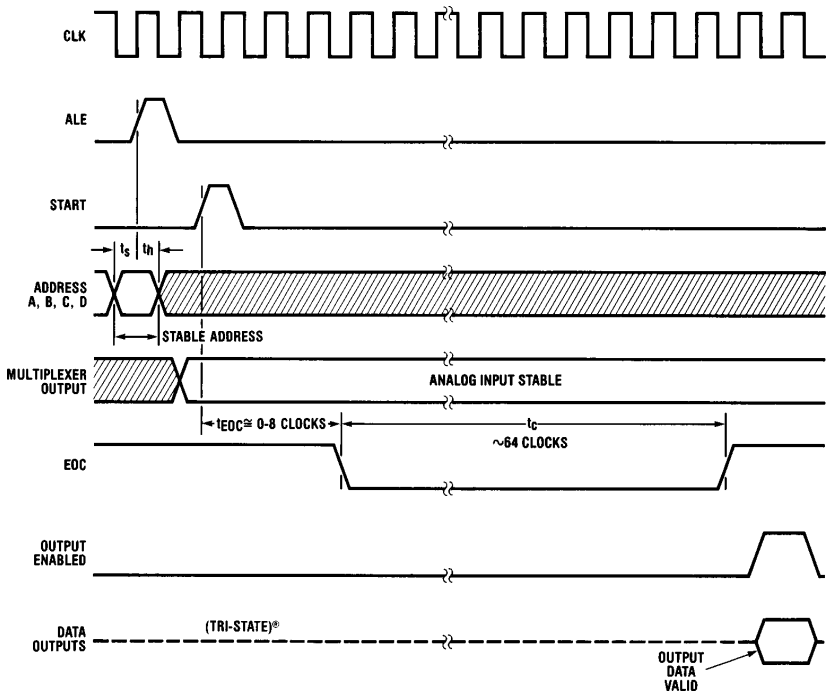

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FIGURE 3. ADC0816/ADC0817 Timing Diagram

III. Analog Input Designs

A. Ratiometric Conversion

The external availability of both ends of the 256R resistor ladder makes this converter ideally suited to use with ratiometric transducers. A ratiometric transducer is a conversion device whose output is proportional to some arbitrary full scale value. In other words, the actual value of the transducers output is of no great importance, but the ratio of this output to the full scale reference is valuable. For example, the potentiometric transducers of *Figure 4* have this feature.

The prime advantage of these transducers is that an accurate reference is not required. However, the reference should be noise free because voltage spikes during a conversion could cause inaccurate results.

Perhaps the simplest method to obtain a reference would be to use a voltage already present in the system, the power supply. As shown in *Figure 4* the 5V supply can be easily connected as the reference, but care must be taken to reduce power supply noise. The supply lines should be well bypassed with filter capacitors and it is recommended that separate PC board traces be used to route the 5V and ground to the reference inputs and to the supply pins.

B. Absolute Conversion

Absolute conversion refers to the use of transducers whose output value is not related to some other voltage. The ''absolute'' value of the transducer's output voltage is very important. This implies that the reference must be very accurately known to be able to accurately determine the value of the transducers output. *Figure 5* shows a typical grounded reference connection using the LM336-5, 5V reference. Note that ratiometric transducers can also be used in this application along with absolute transducers.

In most of the following applications either absolute or ratiometric transducers can be used. The only difference being that when absolute transducers are employed, more accurate references should be used.

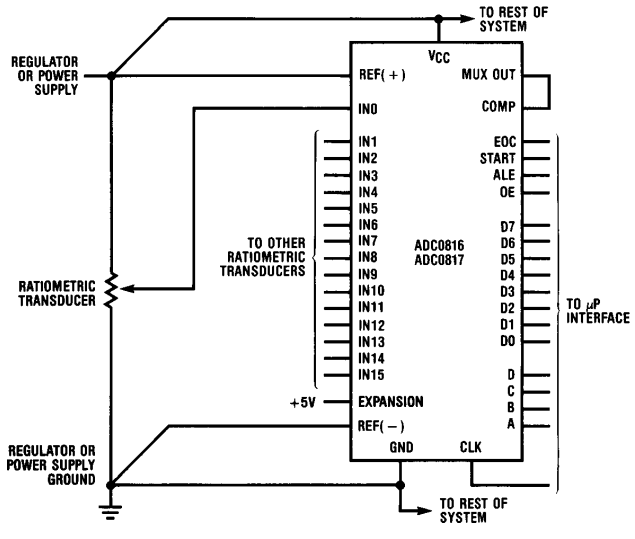

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FIGURE 4. Simple Ratiometric Converter Using Power Supply as Reference

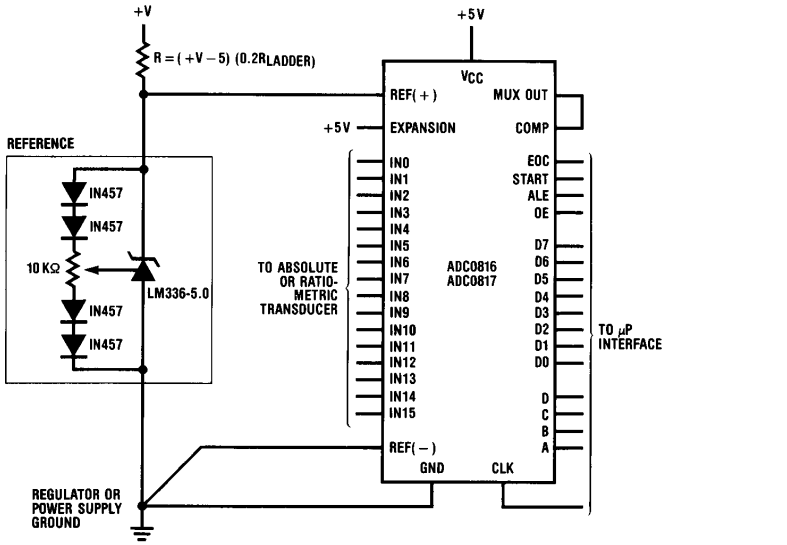

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FIGURE 5. Simple Absolute Converter Using LM336-5.0 Converter

C. Reference Manipulation

In some small systems (particularly CMOS systems) where a reference is required, one can use the reference as a supply as shown in *Figure 6*. In this case the LM336-5 is used to generate the 5V reference and also the 5V supply. An unregulated supply greater than 5V is required to allow the reference to operate. The series resistor, R, is chosen such that the maximum current needed by the system is supplied while keeping the LM336-5 in regulation. The value of this resistor is simply:

$$R = \frac{V_S - V_{REF}}{I_{LAD} + I_{TR} + I_P + I_R}$$

where V_S = unregulated supply voltage; V_{REF} = reference voltage; $I_{LAD} = V_{REF}/1\ k\Omega$, resistor ladder current; I_{TR} = transducer currents; I_p = system power supply requirements; and I_R = minimum reference current.

Figure 7 shows a simple method of buffering the references to provide higher current capabilities. This eliminates the I_p term in the above equation. In *Figures 5, 6*, and *7*, it is advisable to add some supply bypass capacitors to reduce noise, typically 0.1 μF.

D. Reference Voltage Variation

In some cases it is possible to eliminate the need for gain adjustments on the analog input signals by varying the Ref(+) and Ref(−) voltages to achieve various full scale ranges. The reference voltage can be varied from 5V to about 0.5 volts with the one restriction that $[V_{Ref(+)} - V_{Ref(-)}]/2 = (V_{CC}\text{-GND})/2 \pm 0.1$ volts. In other words, the center of the reference voltage must be within ± 0.1V of mid-supply. The reason for this is that the reference ladder is taped by an n or p-channel MOSFET switch tree. Offsetting the voltage at the center of the switch tree from $V_{CC}/2$ will cause the transistors to incorrectly turn off, resulting in inaccurate and erratic conversions. However, if properly applied, this method can reduce parts counts as well as eliminate extra power supplies for the input buffers.

Figure 8 shows a simple supply centered reference where R1 and R2 offset Ref(+) and Ref(−) from V_{CC} and Ground. An LM336, 2.5V reference is shown here, but any reference between 0.5V and 5V can be used. For odd reference values the simple op amp scheme shown in *Figure 9* can be used. Single power supply op amps such as the LM324's or LM10's would work well. R1, R2, and R3 form a resistor divider in which R1 and R3 center the reference at $V_{CC}/2$ and R2 can be varied to obtain the proper reference magnitude.

E. Analog Channel Expansion

The ADC0816/ADC0817 have an expansion control (EC) pin which is actually a multiplexer enable. When this signal is low, all the switches are inhibited so that another signal can be applied to the comparator input. Additional channels can be implemented very simply, as shown in *Figure 10*. This design has expanded the number of channels from 16 to 32. To address the channels, 5 address lines are required. The lower 4 bits are directly applied to the A/D's A, B, C, and D inputs. All 5 bits are also applied to an MM74C174 Hex "D" flip-flop which is used as an address latch for the two CD4051's. The 1Q, 2Q, and 3Q outputs of the MM74C174 feed the CD4051 address inputs 4Q and 5Q are gated to form enable signals for each CD4051. 5Q is also routed to the EC input to properly enable the A/D's multiplexer.

The CD4051s are used with a 5V supply, so their specifications are very similar to the ADC0816/ADC0817 multiplexer. Thus, anything that can be done with the ADC0816/ADC0817 multiplexer can be done with the CD4051's. This includes making use of the previously discussed input designs as well as others.

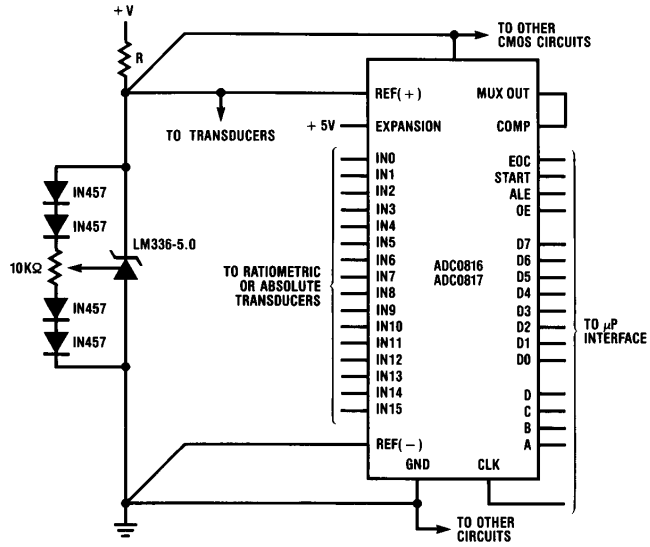

FIGURE 6. Reference Used as Power Supply

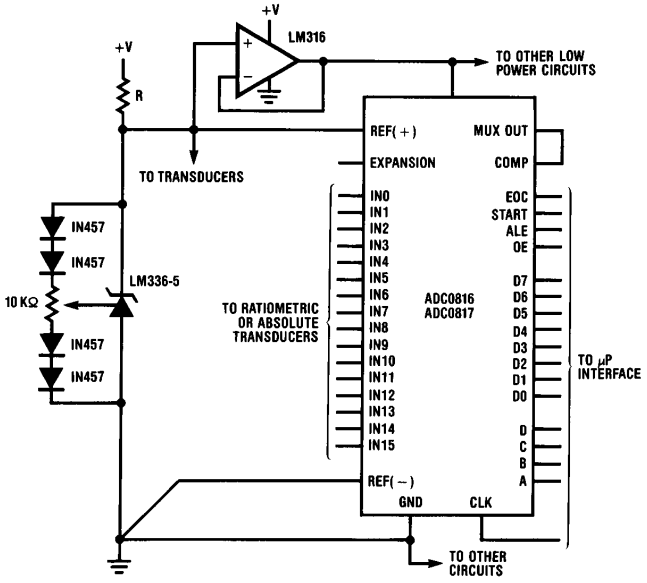

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FIGURE 7. Buffered Reference Used as Power Supply

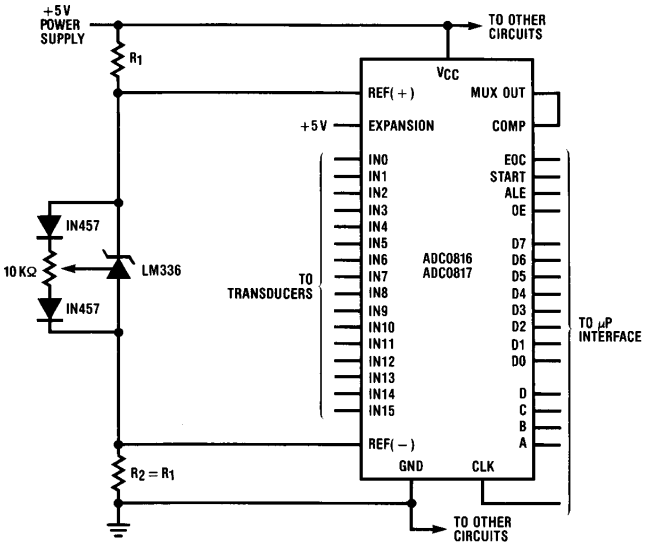

FIGURE 8. Supply Centered Reference Using LM336 2.5V Reference

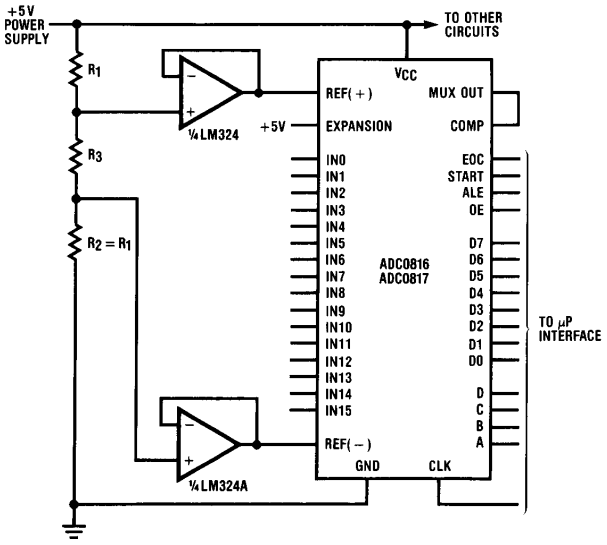

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FIGURE 9. Supply-Centered Reference Using Buffered Resistor Divider

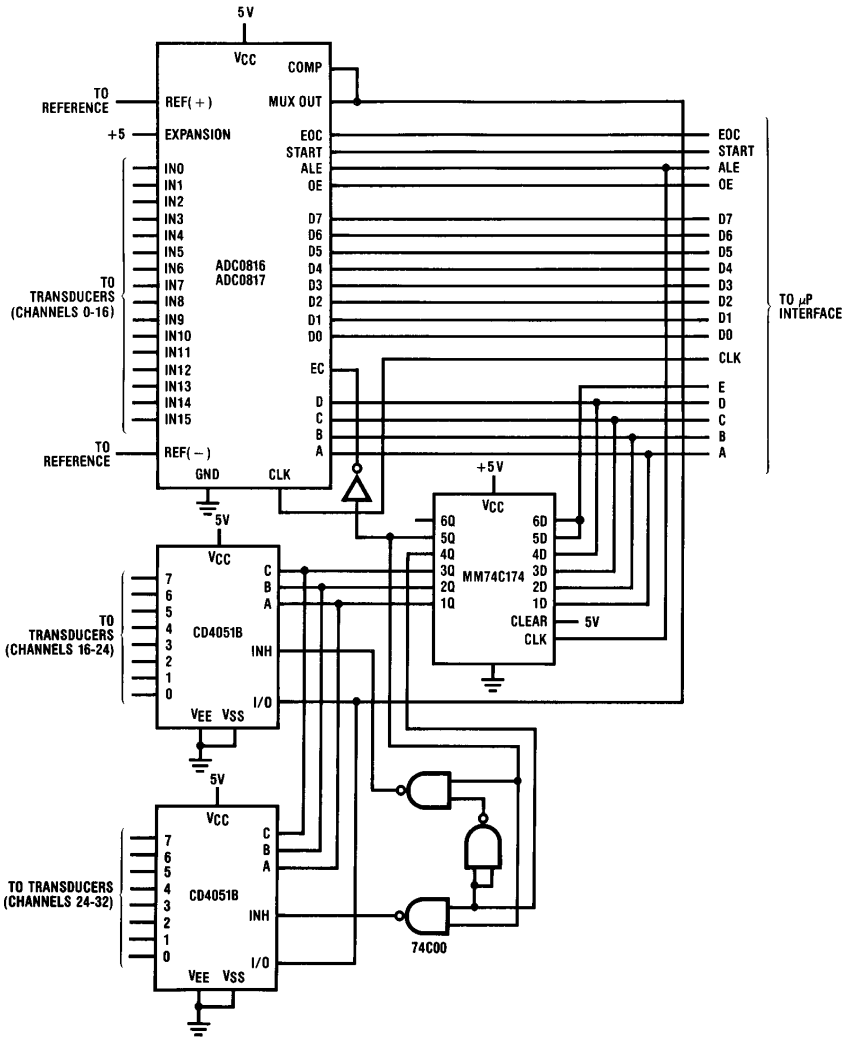

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FIGURE 10. Simple 32-Channel A/D Converter

F. Differential Analog Inputs

An easy, and sometimes overlooked method for implementing a differential input scheme is shown in *Figure 11*. This approach actually implements the differential in software. All 16 channels are paired into positive and negative inputs. Then the controlling logic or microprocessor will convert each channel of a differential pair, load each result, and then subtract the two results. This method requires two single ended conversions to do one differential conversion, hence the effective differential conversion time is twice that of a single channel or a little over 200 μS (Ck = 640 kHz). The differential inputs should be stable throughout both of the conversions to produce accurate results.

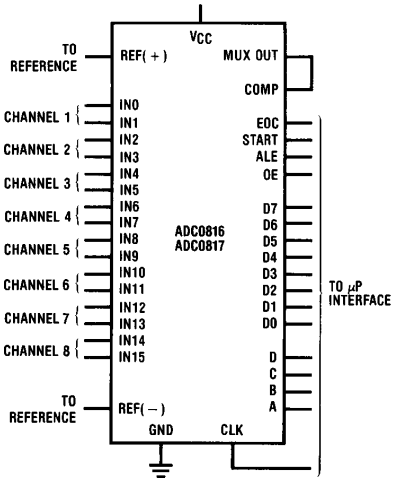

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FIGURE 11. Simple 8-Differential Channel Converter

A 16 channel differential system can be realized by modifying *Figure 10*. This is accomplished by changing the CD4051's addressing and adding a differential amplifier in between the multiplexer outputs and the comparator input. The select logic for the CD4051's has been modified to enable the switches to be selected in parallel with the ADC0816/ADC0817. The outputs of the three multiplexers are connected to a differential amplifier, composed of 2 inverting amplifiers with gain and offset trimmers. A dual op amp configuration of inverting amplifiers can more easily be trimmed and has less stringent feed-back resistor matching requirements, as compared to a single op amp design. The transfer equation for the dual op amp amplifier shown in *Figure 12* is:

$$V_o = \left[\frac{R_2R_5}{R_1R_3}\right] V_1 - \left[\frac{R_5}{R_4}\right] V_2$$

Propagation delay through the op amps should be considered to provide sufficient time between the analog switch selection and start conversion to allow the analog signal at the comparator input to settle. Using the LF353 op amp, this delay should be about 5 μs.

G. Input Signal Buffering

There are three basic ranges of input signal levels that can occur when interfacing the ADC0816/ADC0817 to the ''real world''. These are: a) signals which exceed V_{CC} and/or go below ground; b) signals whose input ranges are less than V_{CC} and Ground, but are different than the reference range; c) and signals that have an input range that is equal to the reference range. Each of these situations require different buffering.

The last situation, case ''c'' is usually trivial. No buffering is required unless the source impedance of the input signal is very high. If this is the case a buffer may be added between the multiplexer output and comparator input pins. If a high input impedance op amp is used, the input leakage looking from the multiplexer input can be greatly reduced. This circuit is shown in *Figure 13*. Using a buffer like this eliminates the necessity for large capacitors on the multiplexer inputs (explained later), but these buffers usually require two supplies and can contribute their own conversion errors.

If the input signal is within the supply, but the reference cannot be manipulated to conform to the full input range, the unity gain buffer of *Figure 13* can be replaced by another op amp as shown in the *Figure 13* inset. This type of amplifier will provide gain and/or offset control to create a full scale range equal to the reference.

The third case, c, where the input range exceeds V_{CC} and/or goes below ground, the input signals must be level shifted before they can go to the multiplexer with the only exception being when the magnitude of the input voltage range is within 5V, but outside the 0-5V supply range. In this case the supply for the entire chip could be shifted to the analog input range, and the digital signals level shifted to the system's 5V supply.

A typical example would be bipolar inputs from -2.5V to $+2.5$. If the ADC0816/ADC0817 have their supply and reference derived as shown in *Figure 14*, then the ± 2.5V logic outputs need only to be level shifted to 0 and 5V logic levels, *Figure 15*.

H. Digital Data Acquisition

The ADC0816/ADC0817 make good analog data acquisition subsystems, but there are many instances where these converters are good digital data acquisition systems as well. If a system has unused channels, digital inputs can be connected to these channels instead of being separately buffered into the system. In the case of a microprocessor system this could eliminate an I/O port and associated logic. The speed at which this input is accessed is one conversion cycle, but many times this will be fast enough. These inputs can be used as input switches, power supply indicator devices, or other system status flags. The microprocessor converts the digital input channel and reads it. Software then decides whether the input is high enough or low enough to cause a particular action.

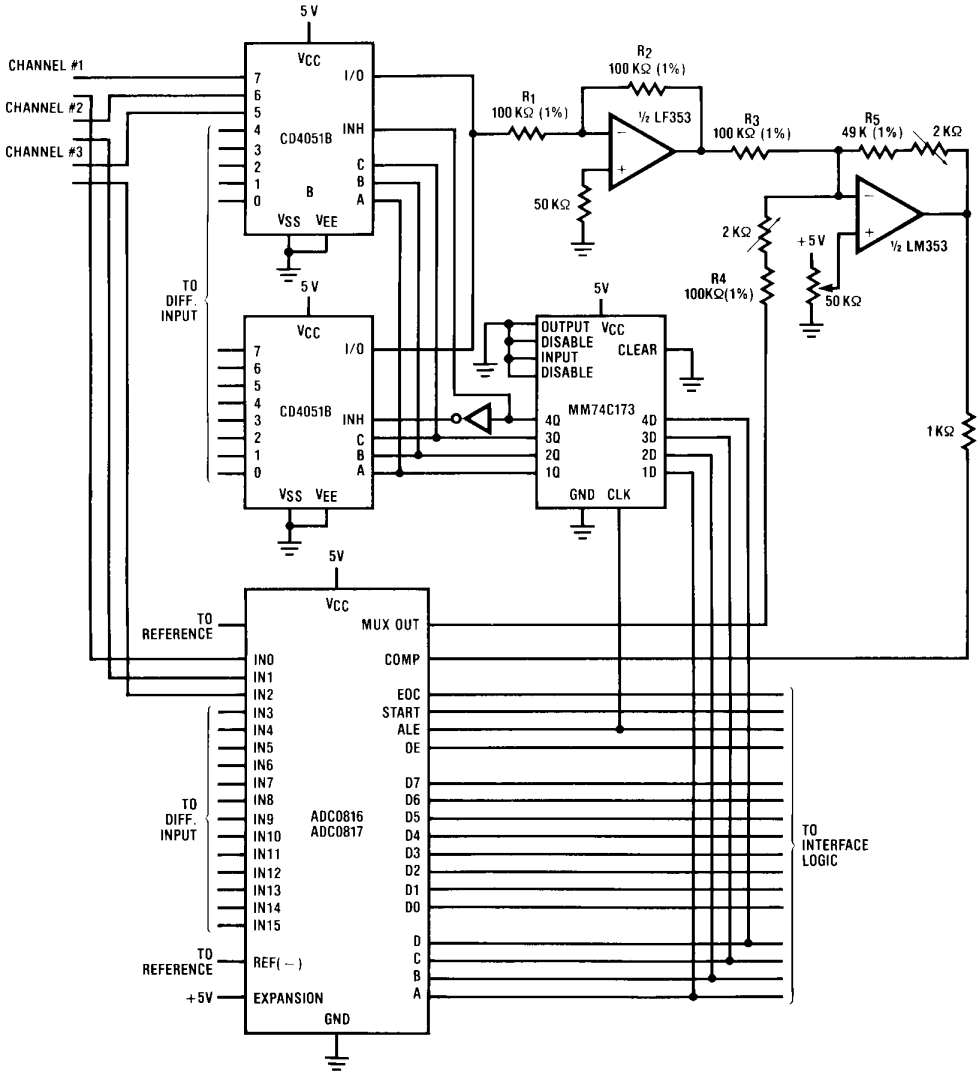

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FIGURE 12. Differential 16-Channel A/D Converter

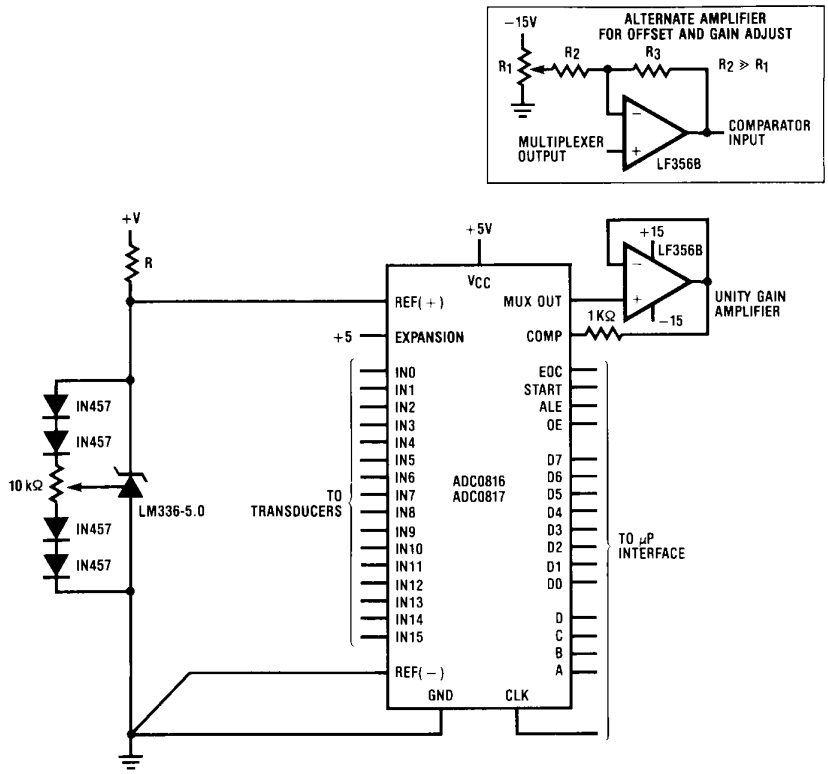

FIGURE 13. Single Input Amplifier Buffering

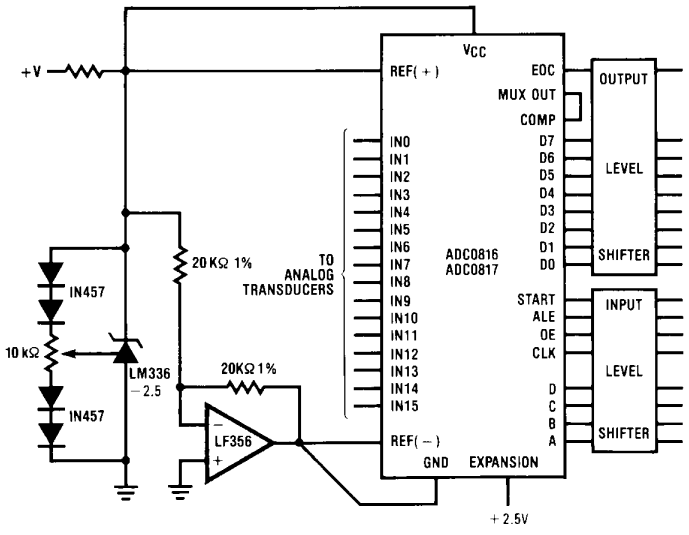

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FIGURE 14. ±2.5V Input Range Data Acquisition

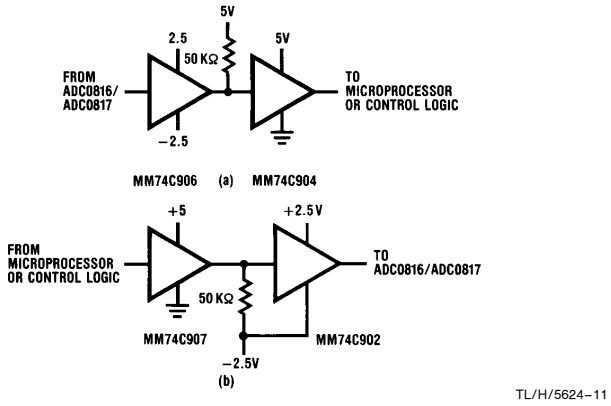

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FIGURE 15. Input/Output Level Shifters

I. Input Considerations

In most instances interfacing analog circuitry is very straightforward, but there are some constraints that should be observed if a reliable accurate system design is to result. One major consideration, input source impedance is actually more complicated than it appears. One would expect that the input current would be a small D.C. current, but due to the nature of the comparator, it is not. The A/D's comparator is a capacitor sampling comparator whose input current is a series of spikes. *Figure 16* shows a simplified model of the comparator input.

When determining a single bit value during a conversion, S1 will close causing C_C and C_p to charge to the input voltage. Then S1 is opened and S2 is closed sampling the ladder. The input current is an RC transient charging current whose magnitude and duration is dependent on the values of C_c, C_p, R_s, R_m and R_L. The duration of the transient must be shorter than the input sample period, and the sample period is dependent on the converter's clock frequency. Thus the maximum source impedance is dependent on the clock period. At a clock frequency of 1 MHz, $R_s \leq$ 1k; and at 640 kHz, $R_s \leq$ 2k. The source impedance of potentiometric transducers vary as a function of wiper position. Thus transducers with a value of $\leq$ 10k at a frequency of 640 kHz and $\leq$ 5k at 1 MHz are suitable.

When a sample-and-hold or some other active device is inserted between the multiplexer and comparator pins, the output impedance of the transducers are no longer as restricted and depend more on the particular Sample/Hold or op amp chosen. The critical parameter now is the source impedance of the buffer which should be $\leq$ 3k at a clock frequency of 1 MHz and $\leq$ 5 kΩ with the clock equal to 640 kHz.

If higher impedances are unavoidable, RC charging errors can be reduced to an average current error by placing a capacitor = 1 μF, from the multiplexer input to ground. Adding this capacitor will average the transient current spikes and cause a small DC current error which for a potentiometric transducer is:

$$V_{ERR} = \frac{Rp}{8}(I_{IN})\frac{Ck}{640\ kHz}\ Volts$$

where Rp = total potentiometer resistance; I_{IN} = 2 μA (maximum input current at 640 kHz); and Ck = clock frequency. For a standard buffer source impedance the voltage error is:

$$V_{ERR} = I_{IN}(R_s)\frac{Ck}{640\ kHz}\ Volts$$

where R_s = buffer source impedance; I_{IN} = 2 μA (maximum average input current at 640 kHz); and Ck = clock frequency.

In addition, whenever analog signals are present in a digital system, several precautions should be exercised to reduce noise on the analog inputs. The analog input signals and the reference input should be kept physically isolated from the digital signals and a single point analog ground should be employed.

J. Protecting the Analog Inputs Against Over Voltages

During normal operation, it is important to keep the analog input voltages to the multiplexer or comparator between V_{CC} and Ground to ensure proper operation. There may be some occasions where over or under voltages cannot be avoided. Protecting the analog inputs, due to their unique nature, can be more difficult than digital inputs. The most effective method is to use external Schottky diodes as shown in *Figure 17a*. Since the Schottky knee voltage is 0.4 volts the IN5166 diodes of *Figure 17a* will safely shunt currents up to several milliamps. To shunt possible currents larger than several milliamps some series resistance may be added to limit these currents as shown in *Figure 17b*, but this value resistor must be no greater than the values specified in the previous section.

A less expensive solution would be to replace the Schottky diode with some standard switching diodes, *Figure 17b*, but since these diodes could only partially shunt the input current from the internal clamp diodes, some series resistor should be used as in *Figure 17c*. If the external diode must shunt a large amount of current the two series resistors of *Figure 17d* should be used. If the input design is such that the input can exceed only one supply the diode going to the other supply can be omitted.

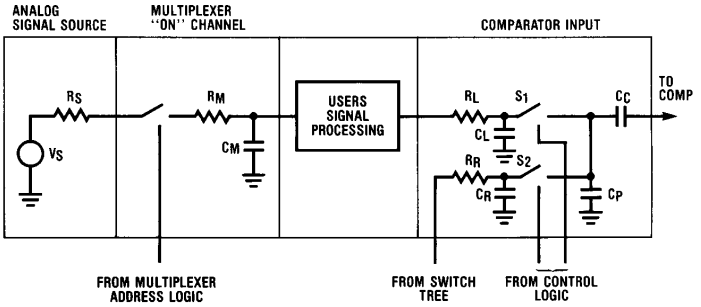

FIGURE 16. Simplified Multiplexer/Comparator Equivalent Circuit

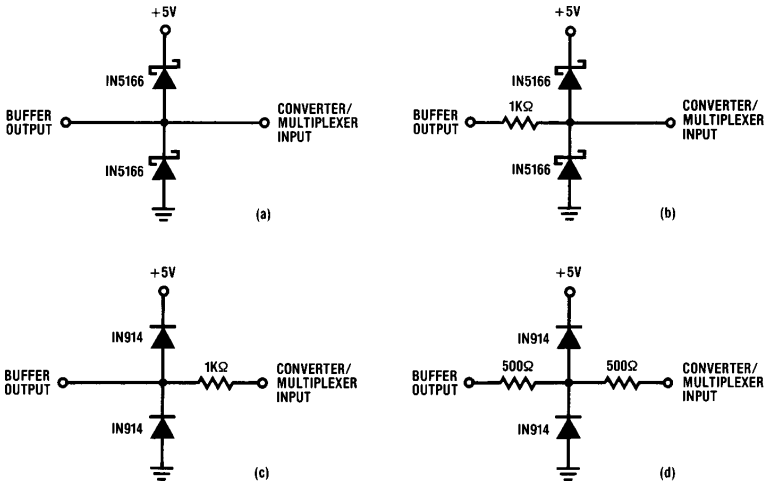

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FIGURE 17. Analog Input Protection Circuitry

IV. Signal Conditioning

There are many applications where it is desirable to add some signal processing circuitry to improve circuit performance. Typical additions would be filter circuits, sample/holds, gain controlled amplifiers, and others. Here again the external accessibility of the multiplexer output and comparator input pins can greatly reduce the amount of circuitry required by enabling the use of only one circuit required by all 16 outputs instead of 1 for each input.

A. Gain Control

Previous examples of gain manipulation have dealt with one fixed gain for all 16 channels, but there are occasions where variable gain or selectable gain may improve accuracy and simplify hardware and/or software.

Figure 18 shows a typical method for gain control. The CD4051, analog multiplexer, is placed in the feedback loop of a simple non-inverting op amp. The gain of this op amp is controlled by selecting one of the CD4051's analog switches.

This will switch a resistor in and out of the feedback loop. If these resistors, R_{2N}, are of different values, different gains are realized. These gains are given by:

$$A_V = 1 + \frac{R_{2N}}{R_1}$$

A microprocessor or some control logic would select a gain by latching the channel address into a MM74C173. It is important to ensure the output of the LF356B does not exceed the power supply, so before a new channel is selected the gain of the op amp should be reduced to a safe value. The 1k resistor on the output of the LF356 is to help protect the comparator inputs from accidental over or under voltages. Two back biased diodes placed from the input to V_{CC} and Ground (IN914 or Schottky) will offer further protection.

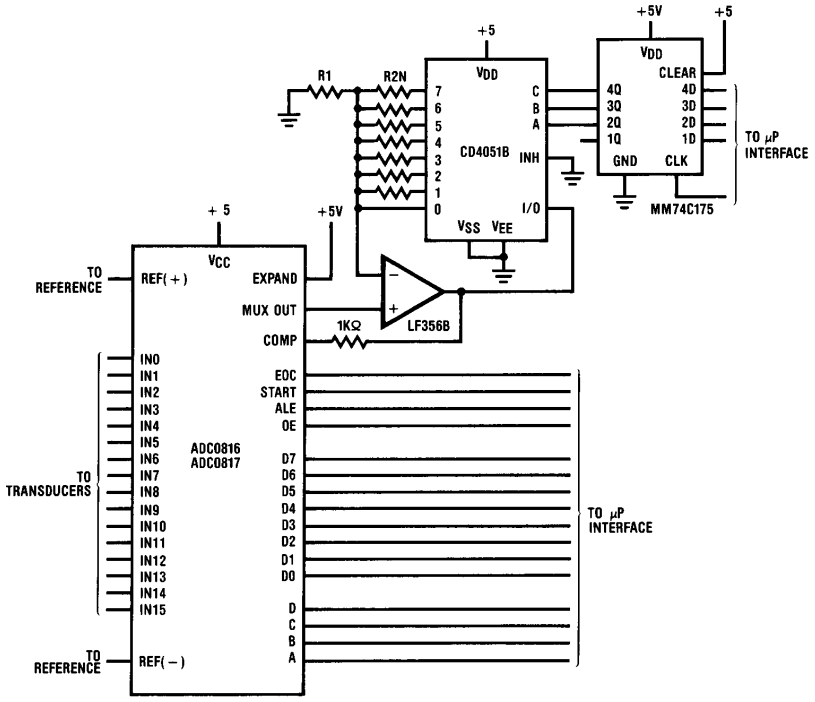

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FIGURE 18. Microprocessor Controlled Gain

B. Sample/Holds

The only major data acquisition element not included on the ADC0816 is a sample/hold circuit. If the input signals are fast moving then a S/H should be used to quickly acquire the signal and then hold it while the ADC0816/ADC0817 converts it. This circuit can be easily implemented by inserting it between the multiplexer output and the comparator input.

The simplest solution is to tie a capacitor on the multiplexer output and then tie this pin to the comparator input pin. The expansion control pin is used as a sample control. When this pin is high one switch is on and the capacitor voltage will follow the input. However, when the expansion control pin is pulled low, all switches are turned off and the capacitor holds its last value, almost. The input bias to the comparator is about 2 μA (worst case with Ck = 640 kHz). Thus the droop rate for a 1000 pF is approximately 2000 V/S or about 0.2 V/conversion. This is totally impractical. If a 0.01 μF capacitor is used instead then the droop rate is 20 mV, which may be satisfactory. Unfortunately, the acquisition time is on the order 100 μS, or about the length of a conversion.

The problem is that the comparator input leakage is too high for this sample and hold. To eliminate this, the input can be buffered by using an LM356B. *Figure 19*. The leakage, now due mostly to multiplexer leakages, is reduced to approximately 100 nA. The droop per conversion is typically less than 1.0 mV per conversion when using a 1000 pF capacitor and the acquisition time is approximately 20 μS.

A more accurate solution would be to isolate the capacitor from both the multiplexer comparator pins of the ADC0816/ADC0817. This is easily accomplished by using the LF398 monolithic sample/hold, as shown in *Figure 20*. The acquisition time for this part is typically 4 μS to 0.1%, and the droop rate is 20 μV/converson. This circuit has its own hold control thus the expansion control is free to be used normally.

The choice of the hold capacitor is critical to the performance of the sample/hold circuit. Some capacitors are composed of dielectrics that will have an initial droop after the hold is strobed. This is due to dielectric absorption. Polypropylene and polystyrene dielectrics have very little dielectric absorption and thus make excellent sample/hold capacitors. Such materials as mylar polyethylene have higher absorption properties and should not be used.

C. Filtering Analog Inputs

Under some conditions the analog input may have come from a noisy environment and to recapture the original signal some filtering may be required. Typically high frequency noise must be filtered. The ADC0816/ADC0817 can easily accommodate the addition of many standard low pass filters. Another useful filter is a 50 Hz or 60 Hz notch filter to eliminate the noise contributed to the circuit by A.C. power lines.

It is particularly easy to place a single passive filter between the multiplexer output and comparator input pins, but passive filters must be carefully designed to reduce input loading. The filter capacitor will tend to average the comparator sampling current as mentioned in the Input Considerations section. To eliminate this, the passive filter can be buffered by an op amp or an active filter could be used.

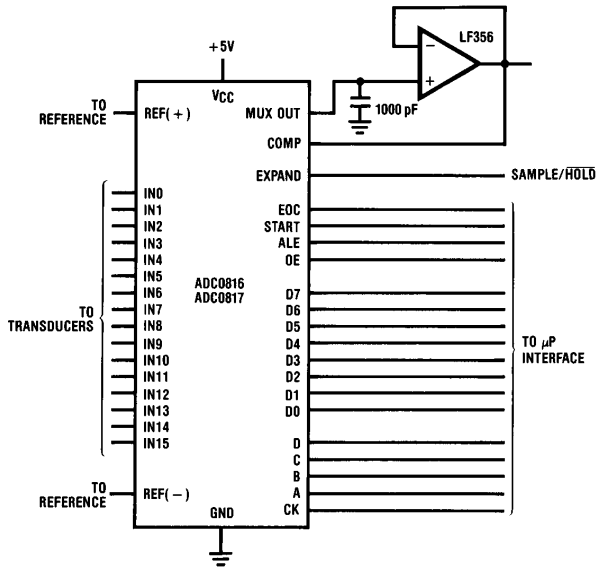

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FIGURE 19. Op Amp Sample Hold Circuit

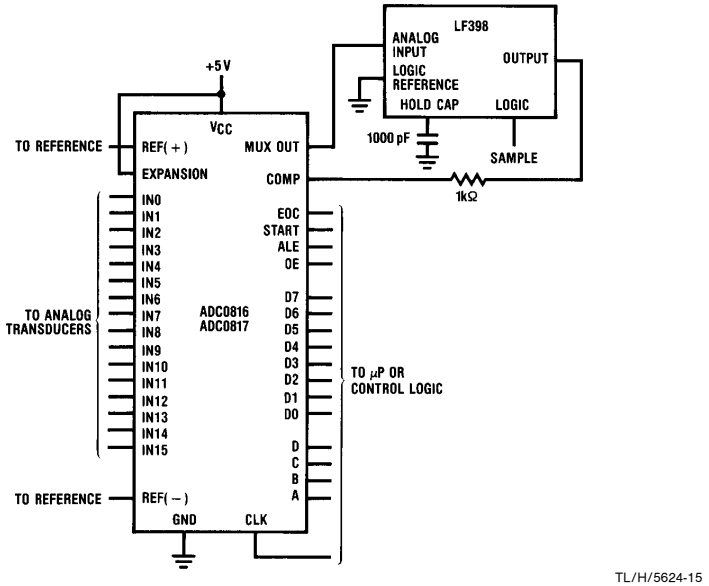

FIGURE 20. Sample/Hold Converter Using LF398

V. Microprocessor Interface

The interface requirements for the ADC0816/ADC0817 interconnection to various microprocessors are essentially the same as the ADC0808/ADC0809 requirements. The devices can be connected to the CPU so that it looks either like a memory location or I/O port. The data transfers can be initiated by either an interrupt to the CPU or the CPU can periodically interrogate the A/D. When trying to implement an absolute minimum components count system, the I/O port (as opposed to memory) addressing will usually require fewer components.

There are several design considerations that apply to most microprocessor systems when interfacing the ADC0816/ADC0817. Even though the actual timing of CPU read and write cycles vary, in general, a microprocessor will output the address and data (if write operation) onto its busses. A certain time later the Read or Write strobes will go active for a specified time. The interface logic must detect the state of the address and data busses and initiate the specified action. For the ADC0816/ADC0817 these actions are: 1) load channel address, 2) start conversion, 3) detect end of conversion and 4) read resultant data. These actions are performed by decoding the read/write strobes, address, and data information to form the and ALE and START pulses, then detect EOC, and finally read the data.

For the most part the decoding and strobe generation is straight forward. The START, ALE, and OE strobes will generally be of the same duration as the CPU read/write strobes and positive going (ALE can be negative going). One subtle choice is where to derive the A, B, C, and D channel select address. These lines can be connected to either the address bus or the data bus. The advantage of connecting them to the data bus is that in minimum systems, more I/O address lines are available for simple decoding. When the A, B, C, and D inputs are connected to the address bus each analog channel becomes a separate I/O port.

In most designs it is very tempting to tie START and ALE together, enabling one pulse to both write the channel address and then start the conversion. However, it is very important that the signal on the comparator input be stable before the conversion starts, otherwise the first and most important successive approximation could be in error. Usually the START and ALE pulses are the same length as the CPU read and write strobes which are normally between 0.2 to 1.μS long. Thus the conversion may start within 1 μS of the address select latching. (Remember the channel is selected on the rising edge of ALE and the conversion begins within 8 clock periods of the falling edge of START.) For converter clocks greater than 500 kHz, 1 μS may not be enough time to allow the analog input signal to propagate through the multiplexer and any additional signal conditioning circuitry such as buffers, S/H's, etc. There are, however, a couple of easy fixes that can correct this possible problem. First, the START/ALE pulse could be stretched to the proper length by using a one-shot (MM74C221 or similar) to generate a pulse as long as the total delay from multiplexer input to comparator input. Secondly, the problem can be circumvented by ''double pulsing'' the converter. This can be easily accomplished in software by writing to the START/ALE address twice. The first pulse latches the desired channel address and starts the conversion. The second pulse must again load the same channel address, which will not change the multiplexer's state, and will then restart the conversion. Of course, the second pulse must occur after the comparator input has settled.

Even though the hardware to interface the ADC0816/ADC0817 to various microprocessors will differ and the system software will vary, the basic routines to operate the ADC0816/ADC0817 are usually similar. There are many variations, but *Figures 21* & *22* illustrate flow charts that typify these routines. The ADC0816/ADC0817 is tied directly

to the address and data bus (as opposed to using a peripheral controller). Generally, the hardware to create START and ALE pulses. This does not necessarily have to be true, but write instructions are conceptually easier and little is gained by designing the logic such that read instructions intiate these pulses. The OE pulse must be created by an I/O or memory read as the converter's data must be read.

The major design consideration is whether EOC should be polled by the microprocessor or whether EOC should cause an interrupt. This decision is system dependent, however the following applications illustrate both methods.

A. Interfacing to INS8080

Interfacing the ADC0816/ADC0817 to an INS8080 system is extremely simple, because the INS8080/INS8224/INS8228 CPU group have separate I/O read ($\overline{I/OR}$) and I/O write ($\overline{I/OW}$) strobes which imply that the INS8080 has separate I/O addressing. In small systems this means that very little or no address decoding is necessary. *Figure 23* shows a very simple interface which uses two NOR gates to gate the I/O strobes with the most significant address bit A7. The INS8080 has 8 bits of port address which will yield a maximum of 4 I/O ports if inputs A, B, C, and D are connected to the address bus. A MM74C74 flip-flop is used as a divide-by-2 to generate a converter clock of 1 MHz. If the INS8080 system clock is $\leq$1 MHz this flip-flop is unnecessary.

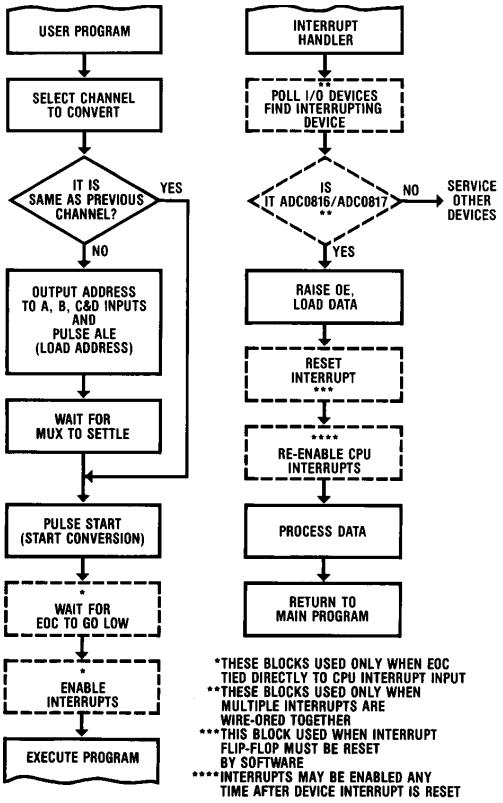

FIGURE 21. Flow Chart for Interrupt Control of ADC0816/ADC0817

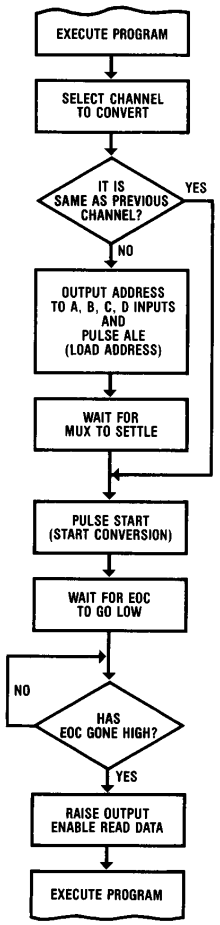

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FIGURE 22. Flow Chart to Control ADC0816/ADC0817 in a Polled I/O Mode

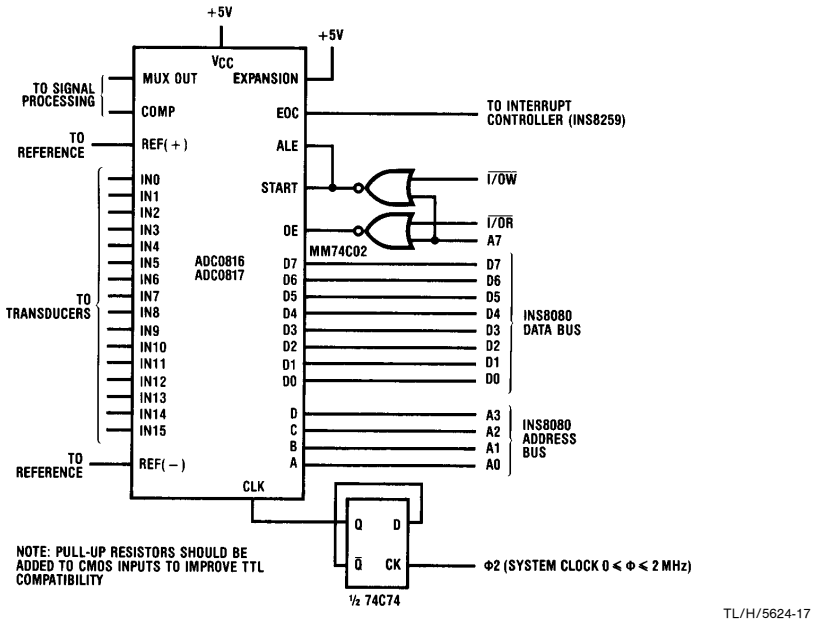

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FIGURE 23. Simple INS8080/8224/8228 to ADC0816/ADC0817 Interface

Typical software would first write the channel address to the converter and start it. As mentioned before, two start pulses should be sent to the ADC0816/ADC0817 to allow the comparator input to settle. After the second start pulse the CPU could execute other program segments until it is interrupted by EOC going high. Depending on the interrupt structure, program control would then be given to the interrupt handler which reads the converter's data.

The second interface circuit, *Figure 24* utilizes a DM74LS139 dual 2-4 decoder in which one-half of the chip is used to create read pulses and the other half write pulses. The START and OE inputs are inverted to provide the correct pulse polarity. This interface partially decodes A6 and A7 to provide more I/O capabilities than before. This circuit also implements a simple polled I/O structure. The EOC output is placed on the data bus by a TRI-STATE inverter when the inverter is enabled by an INS8080 read.

B. Interfacing to the Z80®

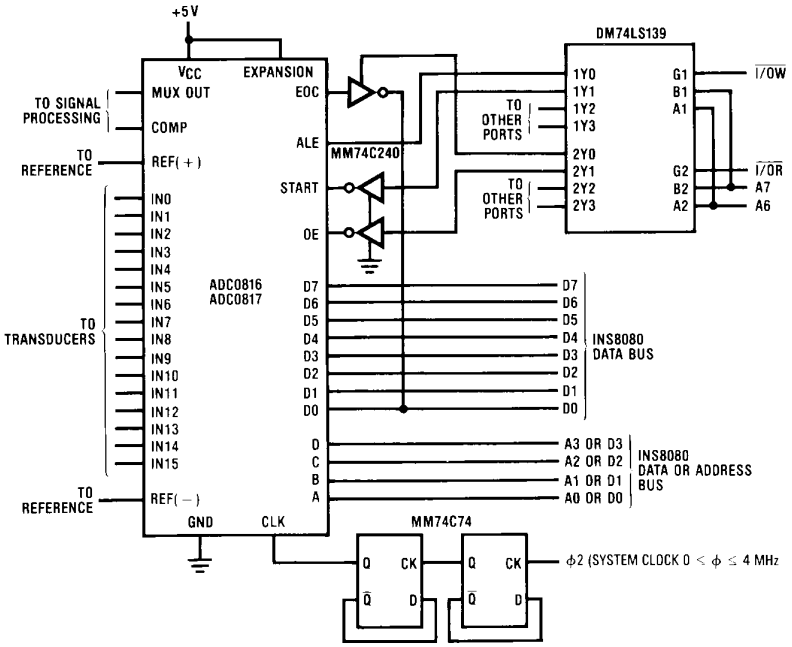
The Z80, even though architecturally similar to the INS8080, uses slightly different control lines to perform I/O reads and writes. In *Figure 25* a NOR gate approach similar to *Figure 22* is shown to interface the Z80 to the ADC0816/ADC0817. Instead of $\overline{I/OR}$ and $\overline{I/OW}$ strobes the Z80 has $\overline{RD}$ (read) and $\overline{WR}$ (write) strobes which are gated with $\overline{IOREQ}$ (I/O request). In the Z80 interface, to show a slight variation, START is connected to OE instead of ALE. This will cause a new conversion to be started whenever the data is read which may seem unusual, but can actually be useful if the converter is to be continually restarted upon completion of the previous conversion. Address bit A6 is used to derive a strobe which will place EOC on the data bus to be read by the CPU.

Figure 26 uses a 6 bit comparator to decode A4-A7 and $\overline{IOREQ}$. Two NOR gates are used to gate the ALE/START and OE pulses. This design functions the same as *Figure 23* except that the DM8131 provides much more decoding.

C. Interfacing to the NSC800

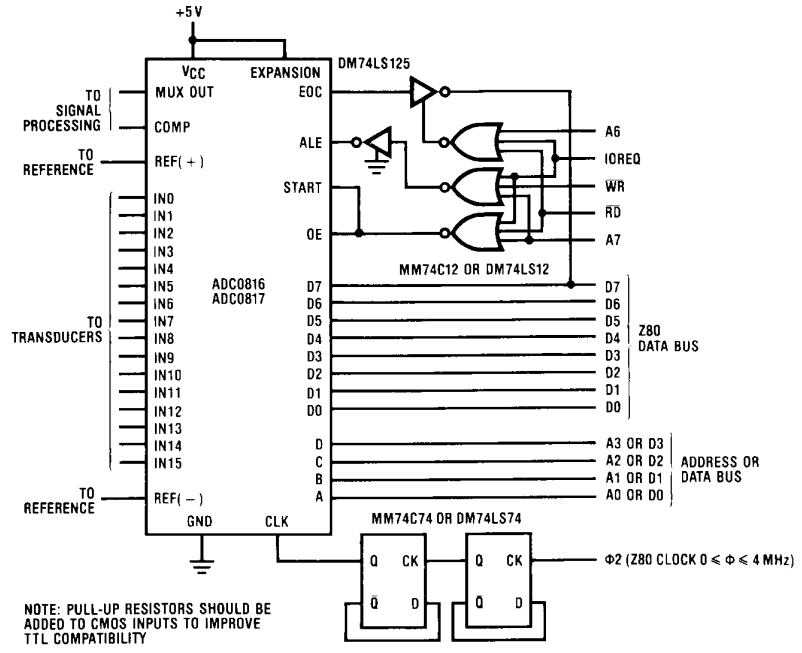
The NSC800 interface is actually very similar to the INS8080 I/O interface, even though their timing is very different. The NSC800 multiplexes the lower 8 address bits on the data bus at the beginning of each cycle. When accessing memory, A0-A7 must be latched out at the beginning of a read or write cycle, but for I/O accessing; the NSC800 duplicates the 8 bit I/O addresses on A8-A15 address lines and latches are not necessary since these lines aren't multiplexed. The I/O read and write strobes are derived from a $\overline{RD}$ (read) and $\overline{WR}$ (write) line and the IO/$\overline{M}$ signal.

Figure 27 shows a design using a dual 2-4 line decoder which decodes A15, and A14 and is enabled by the read/write strobes. TRI-STATE inverters are used to implement a scheme similar to *Figure 24*. This scheme has START and ALE accessed separately so that ''double pulsing'' isn't required.



NOTE: PULL-UP RESISTORS SHOULD BE ADDED TO CMOS INPUTS TO IMPROVE TTL COMPATIBILITY

FIGURE 24. Partial Address Decoding INS8080/8224/8228 to ADC0816/ADC0817



NOTE: PULL-UP RESISTORS SHOULD BE ADDED TO CMOS INPUTS TO IMPROVE TTL COMPATIBILITY

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FIGURE 25. Simple Z80 Interface to ADC0816/ADC0817

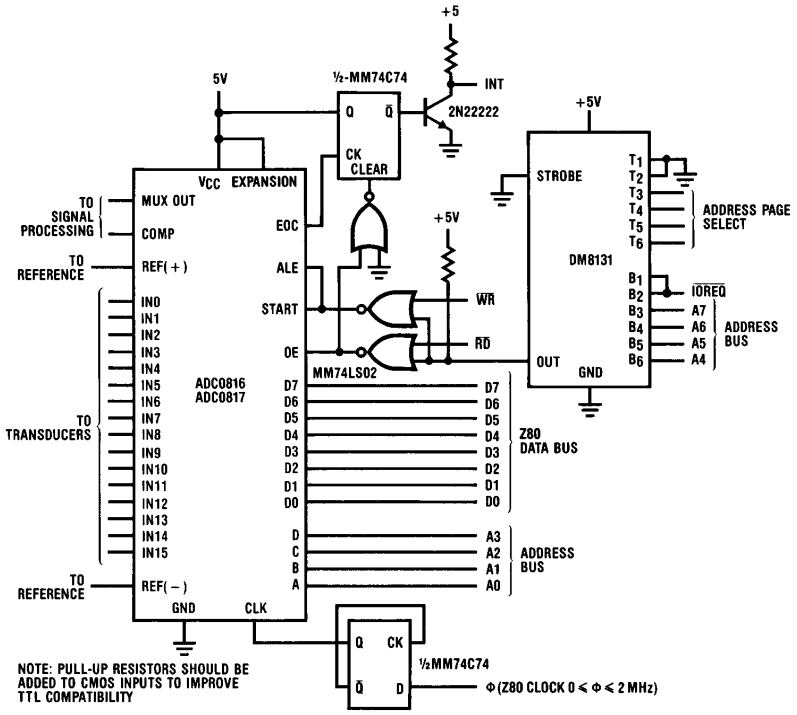

FIGURE 26. Decoded Z80 Interface

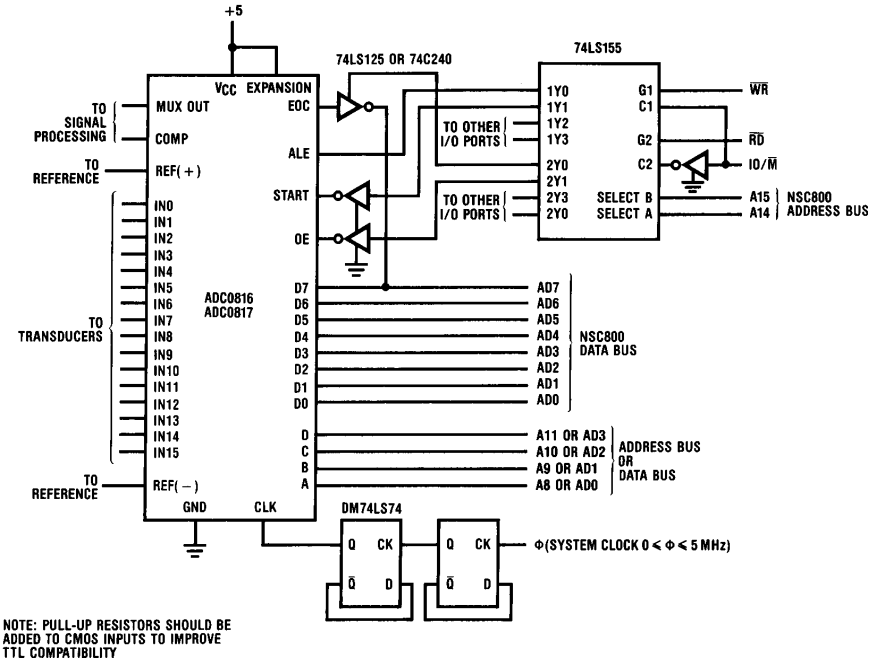

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FIGURE 27. Partially Decoded NSC800 to ADC0816/ADC0817 Interface

The next design, *Figure 28*, uses the same simple NOR gating scheme as *Figure 23*, except the NSC800 control signals are slightly different. A simple interrupt scheme for EOC is employed using an MM74C74. When EOC goes high the flip-flop is set and $\overline{INTR}$ goes low. When the NSC800 acknowledges the interrupt by lowering $\overline{INTA}$, the flip-flop will reset. If more than one interrupt can occur simultaneously either $\overline{INTA}$ should be gated with EOC, or some other signal instead of $\overline{INTA}$ must be used. This is required since it is possible for the NSC800 to detect another interrupt and clear the ADC0816/ADC0817 interrupt before it's detected.

D. Interfacing to the 6800

The 6800 has no separate I/O addressing capabilities, so the system I/O must be addressed as though it is memory. As mentioned before, memory mapping can require more address decoding in order to separate memory from I/O, but in small systems very minimal parts count is still attainable.

Figure 29 illustrates an interface which uses a DM8131 comparator to partially decode the A12, A13, A14, and A15 address lines with the ϕ_2 clock and Valid Memory Address (VMA), to provide an address decode pulse for the two NOR gates which in turn generate the START/ALE Pulse and the output enable signal. This design will locate the A/D in one 4k byte block.

This design tied EOC to $\overline{IREQ}$ interrupt through an inverter. This is only usable in single interrupt systems since the 6800 has no way of resetting this interrupt except by starting a new conversion. Since EOC is directly tied to the interrupt input, the controlling software must not re-enable interrupts until 8 converter clock periods after the START pulse when EOC is low.

The memory control signals are very different from the INS8080 type CPU's. One line indicates whether the operation is a read or write, R/$\overline{W}$ instead of separate read/write outputs on the INS8080/Z80/NSC800. This signal along with VMA indicates a valid read/write operation.

Figure 30 is slightly more complex, but provides more I/O port strobes. A NAND gate and inverter are used to decode the addresses, VMA and ϕ_2 clock. The I/O addresses are located at 11110XXXXXAABBBB (Binary); where X = don't care; A = 00 (Binary) for ALE write or IREQ reset/EOC read and A = 01 for START write or Data read; and B = channel select address if A, B, C and D are connected to the address bus and ALE is accessed. A dual 2-4 line decoder is used to generate these strobes and inverters are used to create the correct logic levels.

The 6800 supports only a wired-OR interrupt structure. In a multi-interrupt environment only one interrupt is received and the interrupt handler routine must determine which device has caused the interrupt and service that device. (Although the INS8080/Z80/NSC800 can implement a similar structure, hardware interrupt controllers can also be used which will automatically vector the μP to the correct service routine.) To do this EOC is brought out to the data bus so the CPU can check it.

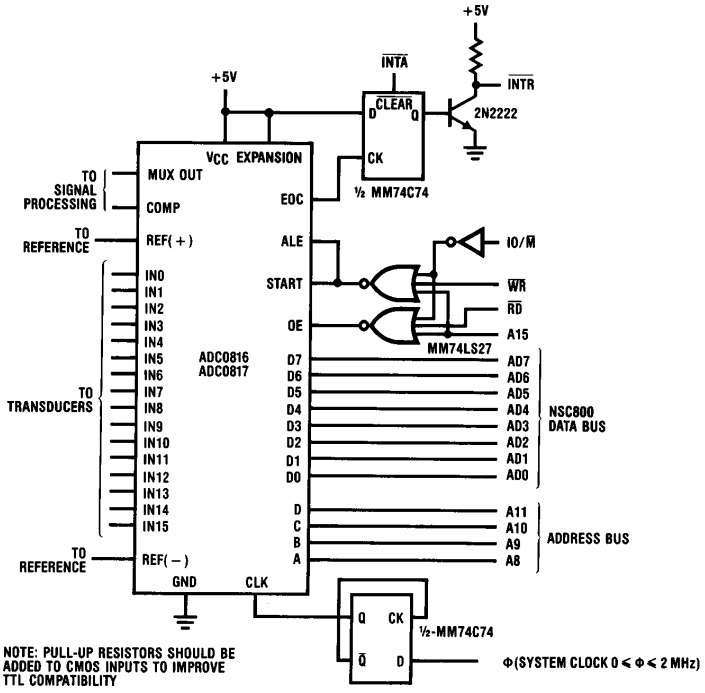

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FIGURE 28. Minimal NSC800 to ADC0816/ADC0817 Interface

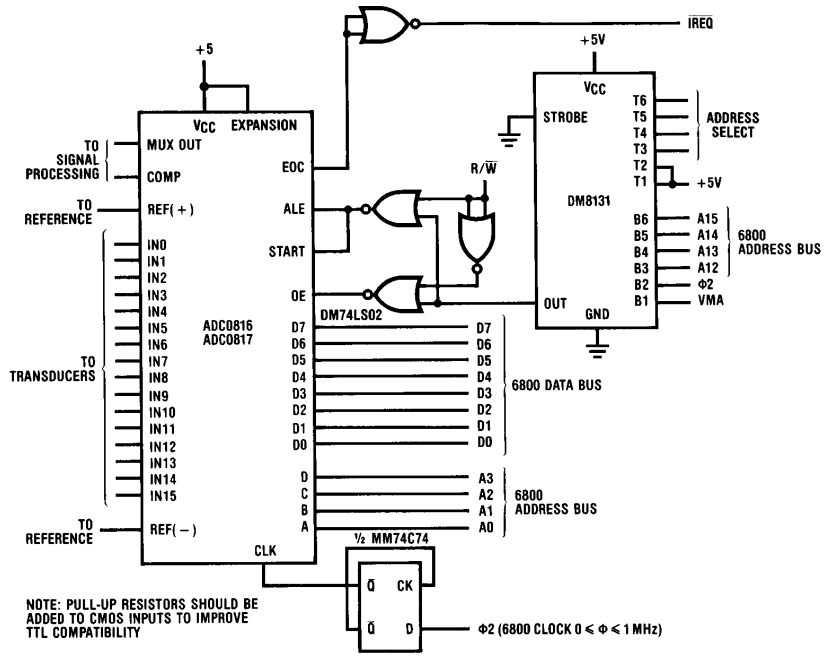

FIGURE 29. 6800 to ADC0816/ADC0817 Interface

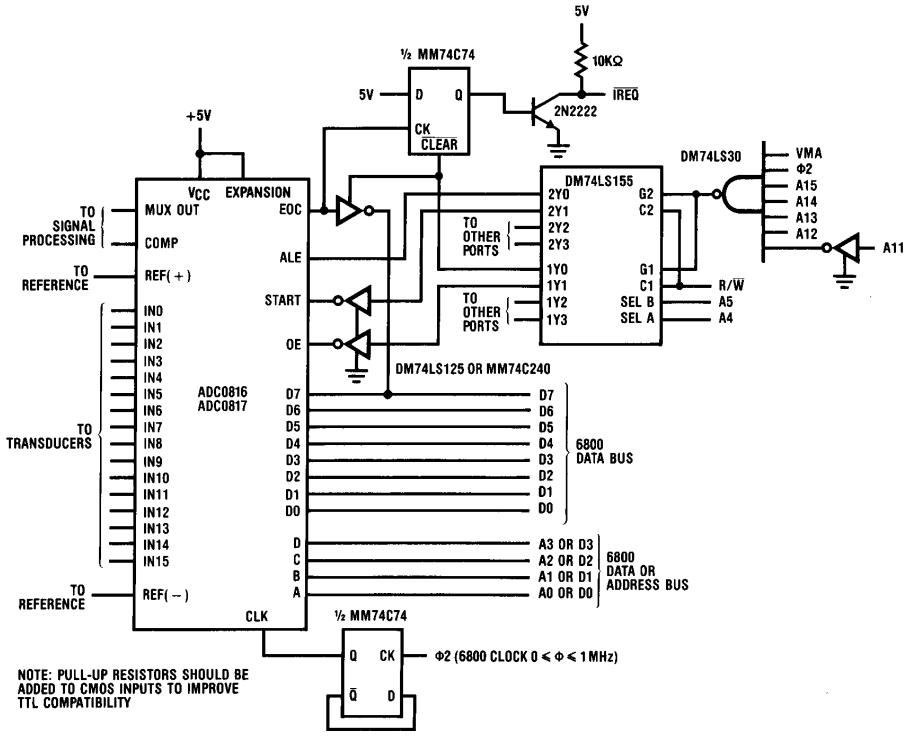

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FIGURE 30. Partially Decoded 6800 to ADC0816/ADC0817 Interface

F. Parallel Interface Circuits

In some cases μP support chips can be used to interface the ADC0816/ADC0817 to microprocessors. Most parallel I/O chips can be used, and provide enough flexibility to enable all functions to be under software control. Typical parallel I/O chips that could be used are INS8255, 6820, Z80-PIO and others. Typically these support IC's would be connected directly to the data and control pins and the software would manipulate the START and ALE pins via the interface chip. In some cases the chips provide handshaking and/or interrupt capabilities which can ease the converter interface. In some cases, the interface circuits will not provide a clock, and therefore must be provided externally.

While use of parallel I/O circuits simplify designs and increase versatility, they are more expensive than the 1 or 2 SSI or MSI circuits that they would replace, and thus not always the best choice.

VI. Conclusion

The ADC0816/ADC0817 are easy to use general purpose A/D converters with the additional benefit of a 16 channel analog multiplexer. The IC's can become a simple standard 8-bit data acquisition circuit or the basis of a more powerful data acquisition system. Both integrated circuits provide features to enable easy microprocessor interface, yet also allow hardwired control logic to be used. In those applications which require less accuracy, the less expensive ADC0817 can be used to reduce overall system cost.

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