Graphics Using the DP8350 Series of CRT Controllers

National Semiconductor
Application Note 212
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December 1978

The DP8350 CRT Controller series is a versatile building block for both low and high-end CRT terminal applications. This application note demonstrates how the DP8350 may be used in CRT graphics applications. Although this presentation is general, when specific examples are given the DP8350 ROM programmed version of the DP8350 series will be used (80 characters per row, 24 character rows, 5 x 7 character, 7 x 10 character field size.)

BACKGROUND INFORMATION

The basic function of the DP8350 controller is to control the elements of the "video loop" (*Figure 1*). A memory address generated by the CRT controller is presented to the CRT memory, which stores a record of what appears on the CRT display. The character generator converts this stored information into serial video data to the CRT monitor. The intensity of the CRT electron beam is modulated by this video data and its position is controlled by the horizontal and vertical sync pulses generated by the CRT controller.

The CRT screen video area is divided into character cells (*Figure 2*). Each cell has a unique CRT memory address. The DP8350 must present the correct character cell address to the CRT memory at the appropriate CRT beam location. Use of the line counter outputs of the DP8350 make possible the subdivision of each character cell address into the unique scan line of the present CRT beam location.

For the DP8350 and its unique internal ROM program format, each character cell is composed of 70 dots (7 dots wide and 10 dots high) *Figure 3*. When using the DP8350, each of these dots may be active video data. Typically however, in alphanumeric display systems, the character generator will provide cell to cell character spacing on the CRT screen by blanking some number of rows and columns of dots. That is why the DP8350's 7 x 10 dot field is used with a 5 x 7 character generator (2 horizontal and 3 vertical dot spaces).

In fact, it is the character generator that restricts the use of the full character cell dot field, not the DP8350! Using a character generator which allows video on every scan line and all dots of the cell width, makes graphic capability possible. This type of graphic display generation is called "character generator graphics."

All of the dots on the CRT display may also be independently controlled by a separate CRT memory address location; this is called "memory mapped graphics."

Both of these graphics display generation techniques will be discussed here, with demonstrations of how the DP8350 series may be used to reduce total component count.

CHARACTER GENERATOR GRAPHICS

In this graphics system (*Figure 4*) the character generator block contains a ROM that has been programmed with

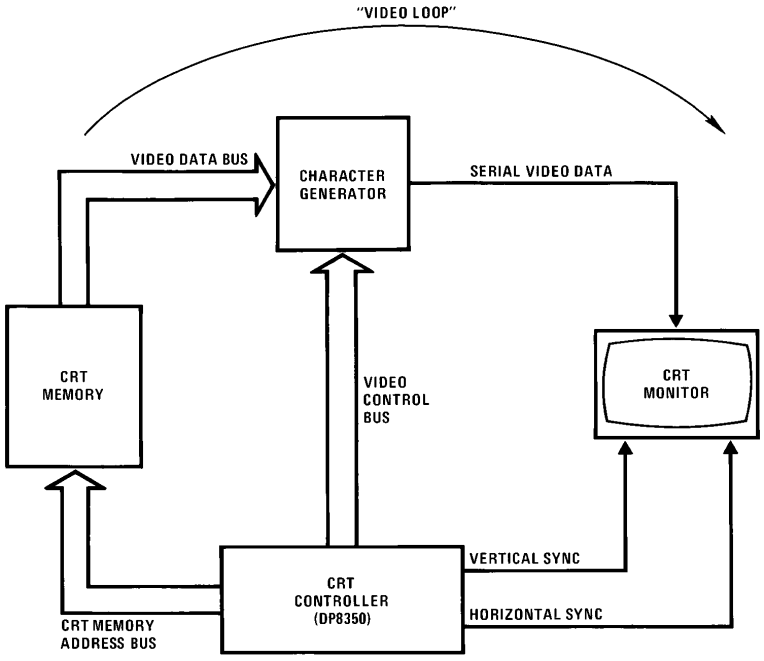

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FIGURE 1. Elements of the "Video Loop"

graphic symbols whose size is contained within the character cell size. This ROM may at the same time contain alphanumeric characters that do not use the full character cell size.

The block representation and operation of this system is the same as the alphanumeric's system previously described. The CRT memory presents the same character cell data to the character generator on every scan line of that character cell address. The character generator ROM is organized with addresses defining a particular symbol and address defining which scan line of a character row the CRT electron beam is currently on; thus defining the video data for that scan line of the symbol. The scan line address data comes directly from the DP8350. The parallel data that results is video data for that screen address cell width. This data is then serially shifted to the CRT monitor with a parallel to serial shift register.

This system allows every scan line of a character row to have active video information; thus the graphics symbol may be programmed to all sides of the character cell providing continuity from cell to cell both horizontally and vertically. At the same time, the alphanumeric's character may be programmed with cell to cell spacing.

Character generator graphics is the simplest most cost-effective approach to CRT graphics. It requires a minimum of software development and hardware support. The DP8350 CRT controller provides all the required timing and control pulses for the CRT memory, character generator, and CRT monitor.

Graphics capability with this system, however, is somewhat limited since individual dot control is not possible; only character cell symbol control is available. This system does apply well in such applications as bar graphs, circuit schematics, or flow charts and when these need to be combined with alphanumeric data.

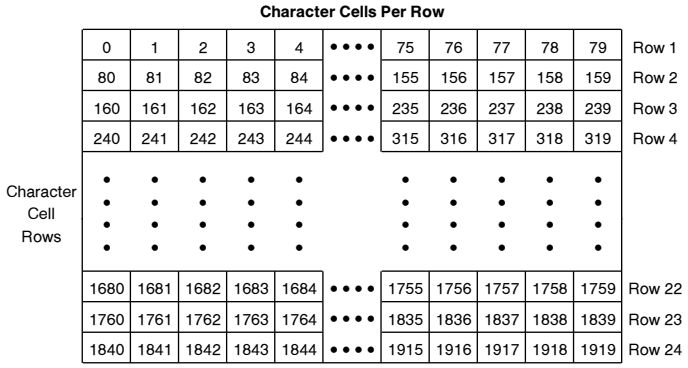

FIGURE 2. CRT Screen Cell Address Map Presented to CRT Memory by the DP8350 (Top of Page Register Contains Address 0) Character Cells Per Row = 80 Character Rows Per Frame = 24

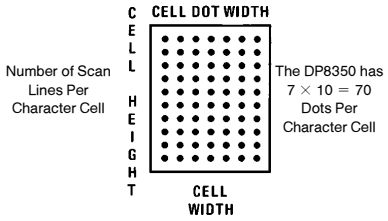

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FIGURE 3. The DP8350 Character Cell is 7 Dots Wide and 10 Dots High

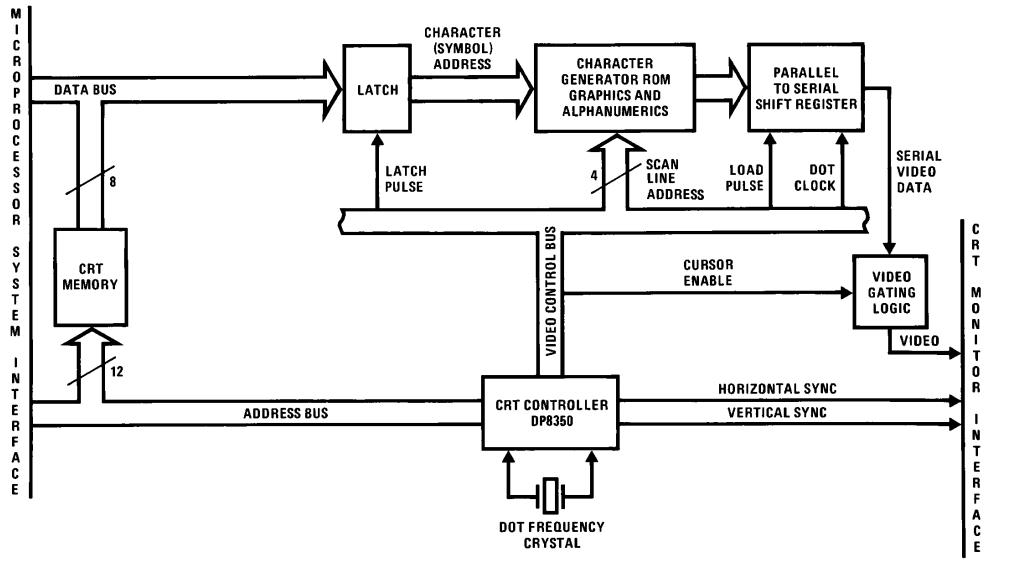

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FIGURE 4. Character Generator Graphics

CHARACTER GENERATOR GRAPHICS—WITH LINE BUFFERS

Modification of the character generator graphics block diagram is possible with the addition of a recirculating line buffer placed between the CRT memory and the character generator (*Figure 5*). In this case the character generator addresses for a character row are loaded serially into this shift register on the scan line before the first video scan line of a character row. These addresses are then recirculated for the number of scan lines per character row minus one (then the next character row of addresses is loaded). This system allows access to the CRT memory by the system controller on all but one scan line of a video character row. In contrast, the system previously described would have allowed access only during blanking intervals. In systems that require heavy access to the CRT memory to update screen information, this approach is very attractive.

In this case, as before, all the required control pulses for the "video loop" are provided by the DP8350 CRT controller.

MEMORY MAPPED GRAPHICS

If a very high resolution graphics display is required, every dot of the CRT display may be independently controlled. In this case, every dot of the CRT screen may be mapped to a specific CRT memory data bit—thus the name Memory Mapped Graphics. This type of system is obviously a more costly type of graphics, since to control every dot not only is there a need for more CRT memory, but the microprocessor overhead is such a system will be greater—both software and hardware. In any case, the DP8350 easily adapts to such a system as demonstrated in *Figure 6*.

In this approach, if you subdivide each character cell such that each scan line of the cell may be independently addressed, then from the CRT memory block instead of 8 bits of data defining a character cell code to the character generator, you get 8 bits of direct video data. Then the CRT memory block serves double duty—CRT memory storage and symbol or character generator. All that is left to do is convert this parallel video data to serial video data as before.

In the case of the DP8350 internal ROM format program, each cell is 7 dots wide; thus only 7 bits of video data are needed per character cell/scan line address. The DP8350 addresses the memory block as before with the character cell address, but in this case also with the scan line address. In this manner, the DP8350 series has a maximum address capability of 16 bits (64k).

VARIATIONS

If memory mapped graphics is desirable but standard alphanumerics is also required, combination of these techniques is possible. For example, if only a small portion of the CRT screen need be memory mapped and the remainder can be character generator alphanumerics and/or graphic symbols. In this case a higher order data bit from CRT memory defines whether the lower order data bits are graphics video data or ASCII and graphics symbol code. *Figure 7* is a block diagram of such a system.

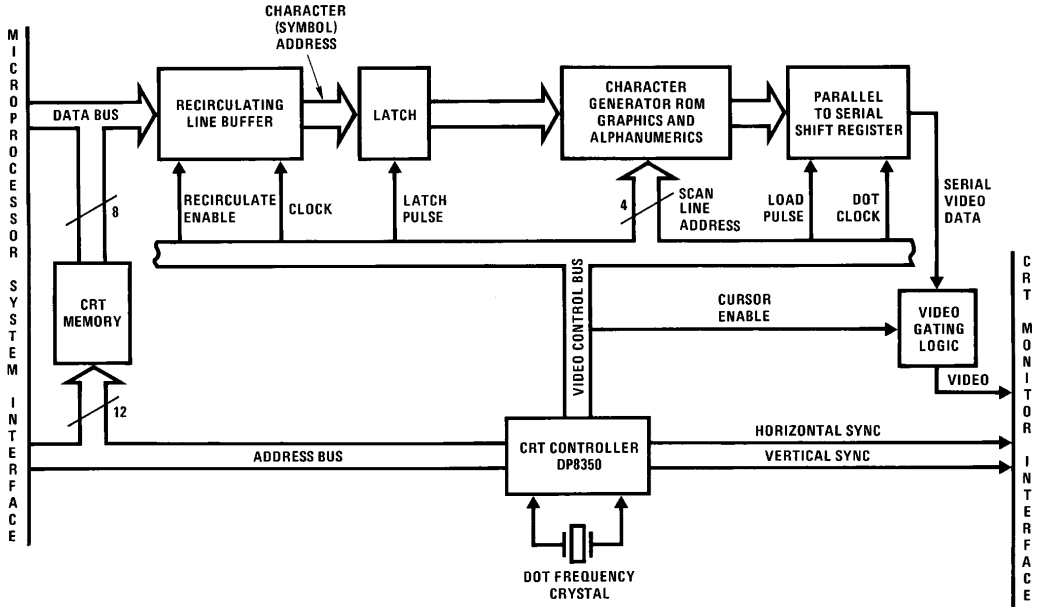

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FIGURE 5. Character Generator Graphics (with line buffer)

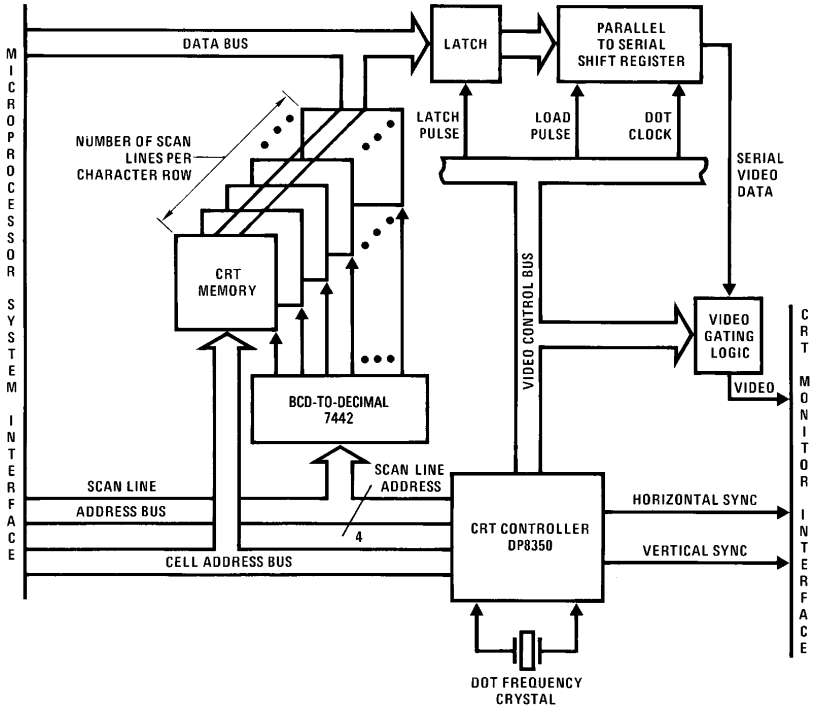

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FIGURE 6. Dot by Dot (Memory Mapped) Graphics

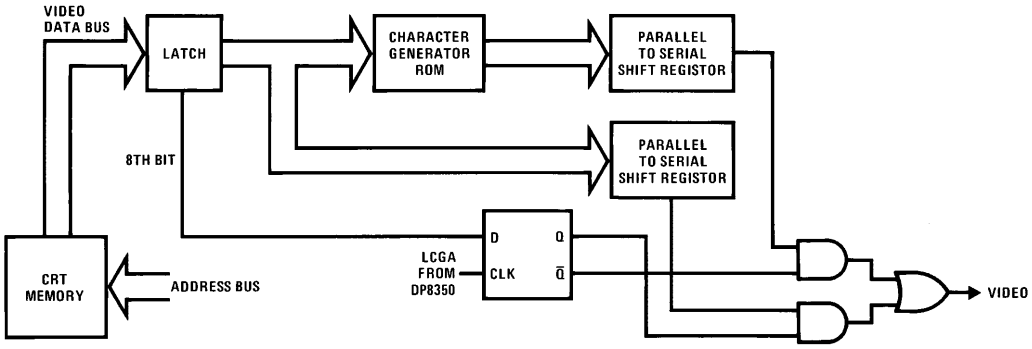

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FIGURE 7. Combined Character Generator and Memory Mapped Graphics

SUMMARY

This application note has demonstrated 2 basic graphics techniques that may be implemented using the DP8350 CRT controller. Variations to these techniques are possible such as changing character cell sizes and subdividing the character cell into dot blocks. In most cases, these variations are done to decrease hardware or software overhead. Since the DP8350 series of CRT controllers offer display format flexibility through internal ROM program variations—the device adapts equally well to these graphics variations as it does to the standard applications.

The fact that all the required control functions for the ''video loop'' are contained within the same chip—the DP8350—makes it very effective in these types of applications; as a result it will produce the minimum chip count and cost.

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