Overture™ Series High-Power Solutions BR100 - Bridged Amplifier BPA200 - Bridged/Paralleled Amplifier

National Semiconductor
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1. INTRODUCTION

National Semiconductor has a broad portfolio of monolithic power integrated circuits covering power levels from a few hundred milliwatts up to 60W of non-clipped continuous average power. These ICs cover most audio applications by themselves, however, for really high-power applications, other methods need to be employed because IC packages have limited power dissipation capabilities.

There are many different way of obtaining over 100W of output power. Most high-ended power amplifier manufacturers utilize discrete circuits which allows them to market their amplifiers as "specially designed,..." However, there is a price to be paid for discrete amplifier designs; they are complex, difficult to design, require many components, lack the comprehensive protection mechanisms of integrated circuits and are not as reliable.

Other methods of obtaining output power greater than 100W include the use of power ICs as drivers to external power discrete transistors. There are a number of these types of circuits, but they too possess all of the same flaws as discrete circuits, including a lack of comprehensive output stage protection.

2. OBJECTIVE

Therefore, the objective was to provide simple high-power solutions that were conservatively designed, highly reliable and has low part count. This document provides two specific, but not unique, application circuits that provide output power of 100W and above. These circuits are the bridged and bridged/parallel configurations.

These two circuits are simple to understand, simple to build and require very few external components compared to discrete power amplifier designs. Simplicity of design and few components make this solution much more reliable than discrete amplifiers with external power transistors. In addition, these circuits inherently possess the full protection of each individual IC that is very difficult and time consuming to design discretely. Finally, these circuits are well known and have been in the industry for years.

3. CONCLUSION

The BR100 (100W Bridged Circuit) and the BPA200 (200W Bridged/Paralleled Circuit) are high-power solutions that can be used in many applications, but they are primarily targeted for Home Theater Amplifier applications such as powered subwoofers, self-powered speakers, and surround sound amplifiers.

While bridged amplifier configurations are able to provide high power levels, they also consume four times more power than a conventional single-ended solution. However, it is feasible to conservatively design a 100W bridged amplifier solution, as well as shown here. The bridged solution is designed to drive an 8Ω nominal load for self-powered speaker or powered subwoofer applications.

The parallel amplifier which will not be discussed here, is another configuration that can be used to obtain higher output power levels by combining two IC outputs and doubling output current drive capability. The parallel amplifier using Overture ICs is ineffective in obtaining higher output power levels with 8Ω loads because the ICs are voltage supply limited. However, the parallel topology provides a great way of achieving higher power levels while keeping within IC power dissipation limits by driving low impedance loads, which is the case for many self-powered speaker and powered subwoofer designs. The main advantage of the parallel configuration is its ability to divide total power dissipation between ICs, since each amplifier is providing half of the load current.

If the bridged and parallel configurations are combined, the outcome is a very high-power amplifier solution that far exceeds the capabilities of one IC alone, while maintaining reasonable power dissipation levels within each IC. The bridged portion doubles the output voltage swing and quadruples the total power dissipation while the parallel portion halves the current between each IC set and divides the total power dis-

sipation between each of the four ICs. The result is higher system output power with each IC not exceeding its individual power dissipation capabilities. Higher output power levels are attained, while the ICs run at a normal temperature, keeping long-term reliability high. The schematic of the Bridged/Parallel Amplifier is shown in *Figure 7*.

The data in the following sections will exemplify that the bridged and bridged/paralleled solutions using multiple power ICs can meet high fidelity specifications while providing output power from 100W up to 400W. The low noise and excellent linearity traits of the monolithic IC are transferred to the high-power solution, making the circuit even more attractive. In addition, the protection mechanisms within the IC, which are not easily designed discretely, are inherently designed into the circuit, making the solution priceless.

While the data show what specs can be achieved by the configurations, as always, good design practices need to be followed to achieve the stated results. In addition to good electrical and layout practices, the thermal design is equally critical with Overture ICs. The following section will expand on the thermal design aspects of Overture ICs. While the bridged and bridged/paralleled configurations are only two of many that can be made to obtain higher output power levels, the concept of "design by power dissipation" is equally applicable to other types of booster circuits.

The BR100 and BPA200 schematics and test results exemplify what can be achieved with proper component selection, thermal design, and layout techniques. The BR100 and BPA200 demoboards are available from your regional National Semiconductor Business Center.

4. THERMAL BACKGROUND

The voltage and current ratings of a power semiconductor are typically the first specs considered in designing high power amplifiers. The same is true for an integrated monolithic power amplifier. However, power dissipation ratings are equally important to the long-term reliability of the power amplifier design. When using a monolithic IC in its intended application and within its specified capabilities, the thermal design is relatively straightforward. When an IC is used beyond its capabilities, as in booster circuits, power dissipation issues become more critical and not as straightforward. Therefore, the designer must understand the IC's power dissipation capabilities before using the IC in a booster configuration.

Typical Characteristic Data

The power dissipation capabilities of a power IC are either specified in the datasheet or can be derived from its guaranteed output power specification. While the power dissipation rating for the LM3886T is 125W, this number can be misleading. Its power dissipation specification is derived from the IC's junction-to-case thermal resistance, $\varnothing_{JC}$ = 1˚C/W, the maximum junction temperature, T_J = 150˚C, and the ambient air, T_A = 25˚C. As stated in the datasheet, the device must be derated based on these parameters while operating at elevated temperatures. The heatsinking requirements for the application are based on these parameters so that the IC will not go into Thermal Shutdown (TSD). The real problem for Overture ICs, however, comes from the sensitivity of the output stage's unique SPiKe™ Protection which dynamically monitors the output transistor's temperature. While the thermal shutdown circuitry is enabled at T_J = 150˚C, SPiKe circuitry is enabled at T_J = 250˚C for instantaneous power spikes in the output stage transistor. As the overall temperature of the IC increases, SPiKe circuitry becomes even more sensitive causing it to turn on before the 125W limit is reached. TSD circuitry will continue to function globally for the IC in conjunction with SPiKe circuitry. However, protection circuitry should not be activated under normal operating conditions. The question then becomes, what is the power dissipation limit for the IC such that SPiKe circuitry is not enabled? Knowing the power dissipation limit and keeping the case temperature of the IC as cool as possible will expand the output power capability without activating SPiKe Protection.

The other way to determine IC power dissipation capabilities is to analyze the output power specification in the datasheet. In the case of the LM3886T, there are two output power specification guarantees: 60W (min) into a 4Ω load using ±28V supplies and 50W (typ) into an 8Ω load from ±35V supplies. Using these two conditions and the theoretical maximum power dissipation equation shown below, results in the following maximum power dissipations:

Single-ended Amplifier Pdmax Equation

$$Pdmax = V_{CC}tot^2/2\pi^2R_L$$

Non-Isolated LM3886T

1. V_{CC} = ±28V, R_L = 4Ω

   $Pdmax = V_{CC}tot^2/2\pi^2R_L = (\pm 28V)^2/2\pi^2(4\Omega)$ = 39.7W not including quiescent power dissipation.

   Pdmax = 39.7W

2. V_{CC} = ±35V, R_L = 8Ω

   $Pdmax = V_{CC}tot^2/2\pi^2R_L = (\pm 35V)^2/2\pi^2(8\Omega)$ = 31.0W not including quiescent power dissipation.

   Pdmax = 31.0W

These results show that the IC can handle a maximum of ≈40W of continuous power dissipation without SPiKe Protection being turned on under continuous sinusoidal input with proper heatsinking. The same theory applies to other Overture ICs as well, like the LM3876T, which is capable of dissipating 31W with proper heatsinking. It should be noted that the results shown above are for the Non-Isolated Power Package, where the back of the package is tied to the silicon substrate, or $-V_{EE}$. The Isolated Power Package has overmolded plastic on the back keeping the package electrically isolated from the silicon substrate. This extra amount of plastic increases the package thermal resistance from 1˚C/W for the non-isolated version to ≈2˚C/W for the isolated version. The result of increased thermal resistance is poorer power dissipation, so the numbers stated above are somewhat lower for the isolated package.

Comparing the above maximum power dissipation in single-ended mode to the bridged-mode under the same electrical conditions shows that the IC's electrical conditions would need to be derated to keep within its power dissipation capabilities. Using the bridged-output Pdmax equation shown below gives us the following results:

Bridged-output Amplifier Pdmax Equation

$$Pdmax = 4V_{CC}tot^2/2\pi^2R_L = 2V_{CC}tot^2/\pi^2R_L$$

The bridged-output Pdmax equation represents the bridged amplifier solution. If a dual amplifier IC is used like the LM1876T, then the total Pdmax would need to be dissipated in the single IC package. However, if two individual ICs are used, like two LM3886Ts, then the total power dissipation is divided between each IC.

Two Non-Isolated LM3886Ts

1. V_{CC} = ±28V, R_L = 4Ω
   Pdmax = $4V_{CC}tot^2/2\pi^2R_L$ = $(\pm 28V)^2/2\pi^2(4\Omega)$ = 158.8W
   Pdmax = 158.8W
   Pdmax/IC = 79.4W

Therefore, using a bridged configuration, V_{CC} would have to be equal to ±20V to keep the IC's power dissipation within 40W when driving a 4Ω load! This equates to about 110W of output power in bridged-mode driving a 4Ω load. When driving an 8Ω load, and using the same bridged Pdmax equation and a maximum of 40W of power dissipation, the supply voltages would have to be ±28V. This equates to about 120W of output power!

There are two major points to note here:

1. The maximum power dissipation analysis was taken into account using regulated power supplies. The IC for the whole analysis is being tested at the worst case power dissipation point for a constant full-load power supply voltage. When using an unregulated power supply, the no-load voltage will be somewhat higher (15%–35%) causing the overall maximum power dissipation to be higher than expected.
2. In the real "audio" application, the average music power dissipation is much less than the maximum power dissipation created by a sinusoidal input. Therefore, the IC will run cooler than expected due to the lower power dissipation.

However, when you put these two points together, they cancel out, but only for music stimulus. Most product qualifications go through worst case power dissipation scenarios which implies that sinusoids will be used with unregulated power supplies. Therefore, when doing the thermal portion of the design, the higher supply voltages will increase the IC power dissipation and must be taken into account.

So, the no-load supply voltage may be just a bit higher than the supply voltages stated above for the 4Ω and 8Ω power dissipation cases. However, to be more conservative, it would be smart to derate these supply voltages just a bit, especially knowing that load impedances are not constant over frequency.

Thermal Conclusion

Because of National's portfolio of products and the capabilities of the bridged/paralleled circuit, the bridged solution is applicable for a power output window between 80W and 120W. Trying to exceed this power level without a rigorous thermal design will be difficult to achieve. More caution needs to be applied along with better thermal management for bridged circuit designs. The proposed bridged/paralleled solution is a more robust design than the bridged circuit, allowing higher output power levels to be obtained. By paralleling the two paralleled sets of ICs, the amount of output power attainable is essentially limitless.

In addition to better heatsinking, the application of a small fan can substantially increase the IC's continuous power dissipation capabilities for either solution. While the air flow of the fan used to take the data is not known, its air flow seemed to be consistent with a typical computer fan. The IC maximum power dissipation data for an individual LM3886 is summarized below in *Table 1*. The data shown below should only be used as a guideline of possible IC power dissipation capability. Your electrical design parameters and thermal management may be different, changing the achievable results. As always, lab testing is recommended to verify any solution.

TABLE 1. Power Dissipation Results

Power IC	Pdmax (No Fan)	Pdmax (With Fan)
LM3886T	40W	60W
LM3886TF	30W	45W

Thermal Testing Conditions

The data summarized in *Table 1* was obtained by using the bridged/paralleled configuration and the following conditions: The system was warmed up for an hour using a power dissipation of 30W per device with a 4Ω load. Four different temperature points were measured after stabilizing, then the supply voltages were incremented while insuring that SPiKe Protection was not enabled during each test by monitoring each amplifier output. The supply voltages continued to be incremented until SPiKe protection or thermal shutdown was enabled, providing the IC's power dissipation limits under those operating conditions.

The input stimulus was a 20 Hz sinewave with an amplitude corresponding to the worst case power dissipation for the given load and supply voltage. The ICs were evenly spread out along the heatsink with dimensions of: 3.25" high x 13.25" long x 1.3125" deep. The main body of the heatsink was 0.25" thick with (10) 1.0625" deep fins. Unfortunately, the fins ran horizontally, which hindered heat radiation without a fan, but helped with air flow and heat dissipation when a fan was used.

This same testing procedure can be used for any number of booster circuits, including variations of the bridged/paralleled circuit. Another variation would be to add more ICs in parallel to further reduce power dissipation, allowing low impedance loads to be driven to obtain even higher output power levels.

5. BR100 - 100W BRIDGE CIRCUIT

Audio Testing

The following graphs represent the performance level attainable from the bridged circuit when well laid out and properly heatsinked. The testing focused on maximum output power capabilities, and amplifier linearity. The low THD+N plots shown on the following page exemplify the high degree of linearity of the bridged circuit which directly translates into a cleaner sounding more transparent amplifier. Other bridged circuit topologies that use the output of one amplifier as the input to the second inverting amplifier, as used by our competitors, inherently possess higher THD and noise that will degrade the solution's sound quality.

Linearity Tests

The linearity of the amplifier is represented by the low THD+N values shown in *Figure 1* and *Figure 2*. *Figure 1* represents the THD+N vs Frequency for 1W, 56W, and 100W power levels. The 20 kHz THD+N is less than 0.02% for 1W and about 0.008% for 56W and above. For normal listening levels, the THD+N is about 0.004% for most of the audio band. *Figure 2* represents the THD+N vs Output Power Level for 20 Hz, 1 kHz, and 20 kHz. The THD+N between 20 Hz and 1 kHz is less than 0.004% from 1W to the clipping point. The 20 kHz THD+N is less than 0.02% from 1W to the

clipping point. The continuous clipping point power is around 105W while the power at 10% THD is about 140W. These THD graphs were obtained using relative THD units, which indicates that the noise level for the amplifier is quite low. Typically, the noise level becomes a significant THD+N contributor at low power levels and shows up as a linearly decreasing function of increasing input signal amplitude. The low power level THD+N for this amplifier is more than acceptable for home entertainment applications.

Figure 3 represents the bridged amplifier schematic. The design is extremely simple, consisting of a non-inverting power op amp configuration and an inverting power op amp configuration. The input to the amplifier solution goes to each individual configuration. While closed-loop gain matching is not critical, it is recommended to have fairly close values. The main functional point to note about this solution is that for a positive going input signal, amplifier U1 will have a positive changing output signal while U2 will have a negative changing output signal. The final voltage across the load is two times the peak amplitude of each individual amplifier output. Since output power is based on the square of the output voltage, the output power is theoretically quadrupled. This document will not go further into the functionality of the circuit as it is widely known in industry.

BR100 THD+N vs Freq RI=8Ω V_{CC}=±25.5V BW<80 kHz Po=1W, 56W, 100W

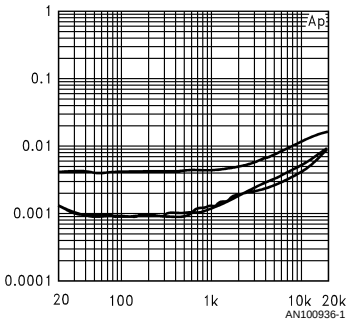

FIGURE 1. THD+N vs Frequency

BR100 THD+N(%) vs Po @ f=20 Hz, 1 kHz, 20 kHz, RI=8Ω V_{CC}=±25.5V BW<80 kHz

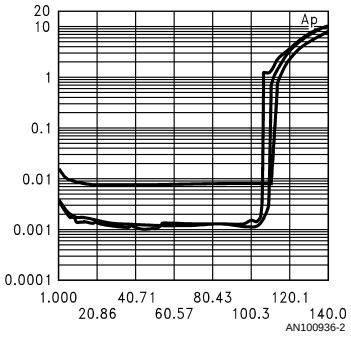

FIGURE 2. THD+N vs Output Power

Schematics:

— Bridged Amplifier Schematic

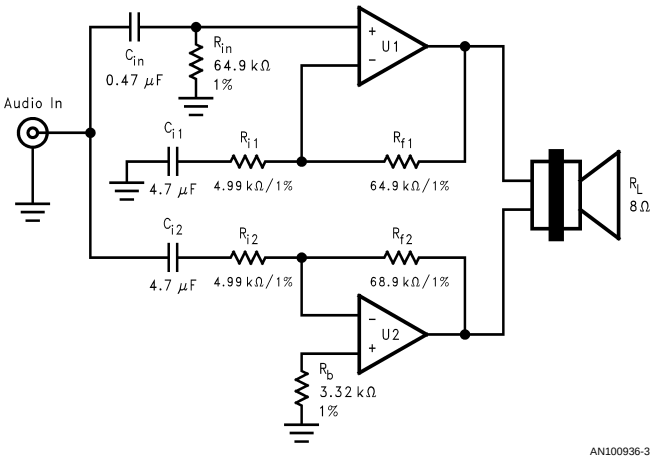

FIGURE 3. Bridged Amplifier Schematic

Electrical Design Notes

The following electrical design notes will aid in making the bridged amplifier design go more smoothly while also helping to achieve the highest level of performance.

— The input impedance of the inverting amplifier is essentially resistor, R_i. The value of this resistance affects the gain setting of the amplifier as well as the low frequency rolloff in conjunction with C_i. There is a tradeoff between having a low frequency rolloff, a high input impedance and a small capacitor size and value. It is critical to have a flat band response down to 20 Hz while it is equally important to have a high enough input impedance so that heavy loading does not occur from the preamp stage. Using large valued low-cost capacitors implies the use of leaky electrolytics which affect the output offset voltage. Electrolytic capacitors are also less linear than other premium caps and should not be used in the signal path when not necessary. This tradeoff issue is the toughest portion of the design. The amplifier gain setting is just as one would expect for an inverting op amp. Of course, the input impedance issue can be quickly resolved by using a voltage follower as an input buffer, but it was omitted from this design to minimize cost and simplify the design. The values provided in the bridged schematic are at a good tradeoff point. There is sufficient input impedance for practically all audio op amps, the closed-loop gain setting is 14 for each amplifier, (gain of 28 overall) while the capacitor value of 4.7 µF sets the low frequency −3 dB rolloff at about 7 Hz.

— The non-inverting input resistance, Rb, is used to create a voltage drop at the non-inverting terminal to offset the voltage at the inverting input terminal due to the input bias current flowing from the output to the inverting input. Generally, the value of this resistor equals the value of the feedback resistor so that the output offset voltage will be minimized close to zero. However, if this value is too large, noise can easily be picked up which will be amplified and seriously affect the THD+N performance. If the resistor is eliminated and the terminal is grounded, the THD+N performance will be much better, but it will not necessarily be optimized. By connecting the non-inverting input directly to a ground reference, any noise on that ground will be directly injected into the amplifier, amplified and thus will also affect the THD+N performance. The best solution is to use a value of resistance not too large to pick up stray noise and not too small as to be affected by ground noise fluctuations. The value used in the previous plots was a 3.32 kΩ resistor. It should be noted that this is not necessarily the optimized value and can change with varying circuit layouts.

— Low leakage signal path capacitors should be used where possible to reduce output offset voltages. This is not too big of an issue since each gain stage has only unity gain at DC. This is another reason why 1% resistor tolerances are not necessarily required. To obtain the highest quality amplifier, polypropylene capacitors should be employed in the signal path and for supply bypassing.

— As always, the better the supply bypassing, the better the noise rejection and hence higher performance.

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6. BPA200 - 200W BRIDGED/PARALLELED CIRCUIT

Audio Testing

The following graphs represent the performance level attainable from the bridge/parallel circuit when well laid out and properly heatsinked. The testing focused on maximum output power capabilities, amplifier linearity and noise level.

Linearity Tests

The linearity of the amplifier is represented by the low THD+N values shown in *Figure 4* and *Figure 5*. *Figure 1* represents the THD+N vs Frequency for 1W, 56W, and 200W power levels. *Figure 5* represents the THD+N vs Output Power Level for 20 Hz, 1 kHz, and 20 kHz. The THD+N between 20 Hz and 1 kHz is less than 0.004% from 1W to the clipping point. The 20 kHz THD+N is less than 0.02% from 1W to the clipping point. The continuous clipping point power is around 210W while the power at 10% THD is 300W. These THD graphs were obtained using relative THD units, which indicates that the noise level for the amplifier is quite low. Typically, the noise level becomes a significant THD+N contributor at low power levels and shows up as a linearly decreasing function of increasing input signal amplitude. In *Figure 5*, the THD+N decreases from 0.004% to 0.001% from 1W to the clipping point for frequencies between 20 Hz and 1 kHz. The THD+N decreases from 0.02% to 0.009% from 1W to 50W and rises thereafter up to about 0.015%.

BPA-200 THD+N vs Frequency Po = 1W, 56W, 200W RI=8Ω BW<80 kHz

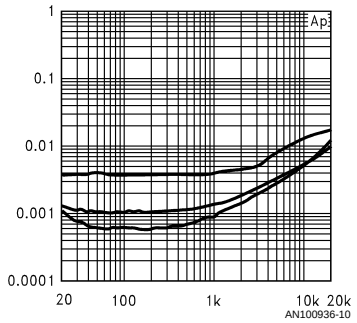


FIGURE 4. THD+N vs Frequency

BPA-200 THD+N(%) vs Po @ f=20 Hz, 1 kHz, 20 kHz RI=8Ω BW<80 kHz

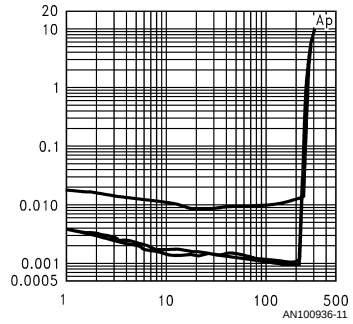


FIGURE 5. THD+N vs Output Power

Output Power Tests

Although the amplifier was designed based on thermal dissipation capabilities using continuous sinusoidal inputs, the output power levels attainable are significantly greater with pulsed waveforms that more accurately reflect music material. The continuous clipping point power and burst power levels are shown in *Table 2* below.

TABLE 2. BPA-200 Maximum Output Power Levels

Load Impedance	Continuous Clipping Point Power	Burst Clipping Point Power
8Ω	225W	295W
4Ω	335W	450W

The burst power levels were obtained using a 20 Hz sinewave with two cycles on and twenty cycles off. The output power capability of the BPA-200 is further substantiated by the power bandwidth measurement. The amplifier is capable of producing 200W continuously into an 8Ω load up to f = 90.5 kHz with little change in THD+N. The graph in *Figure 6* shows the power bandwidth measurement. Also notice that the low frequency power in the graph is not rolled off as would normally occur with a DC blocking capacitor. The servo circuits allow the low frequency power to remain constant down to DC without high output offset voltage.

BPA-200 Power Bandwidth @ Po = 200W RI=8Ω BW>500 kHz

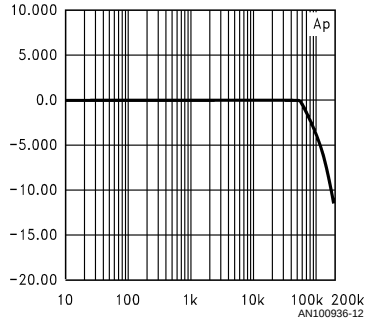


FIGURE 6. Power Bandwidth

Noise Floor Tests

The following plots exemplify the low-noise aspects of the BPA-200. *Figure 7* was obtained using an 8k FFT relative to 1 dBV with a measurement bandwidth of 22 kHz. An FFT analyzer is extremely handy in determining the noise culprit when debugging a new circuit and its layout, as well as evaluating the coupling effects of the 60 Hz component and its harmonics. As shown in *Figure 8*, the noise level is quite low and the influence of the power supply is relatively small. The highest 60 Hz components reach −105 dBV, while the noise floor sits around −120 dBV.

BPA-200 Spot Noise Floor(dBV) RI=8Ω BW<22 kHz

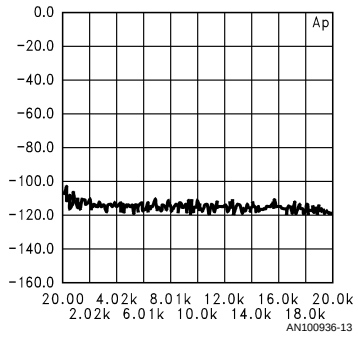


FIGURE 7. Linear-Scale Noise Floor

BPA-200 Spot Noise Floor(dBV) RI=8Ω BW<22 kHz

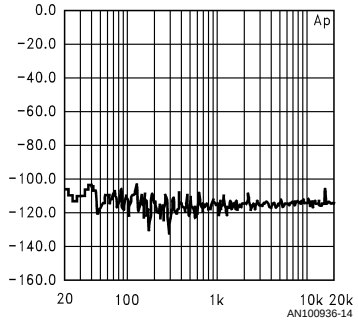


FIGURE 8. Log-Scale 60 Hz Noise Floor

Even with the limited number of graphs shown, the quality of this amplifier from a measurement perspective is quite good. However, with all audio equipment, nothing is really better than doing a test drive with your ears. We recommend that you check this design concept out.

7. Schematics:

— Bridged/Paralleled Amplifier Schematic

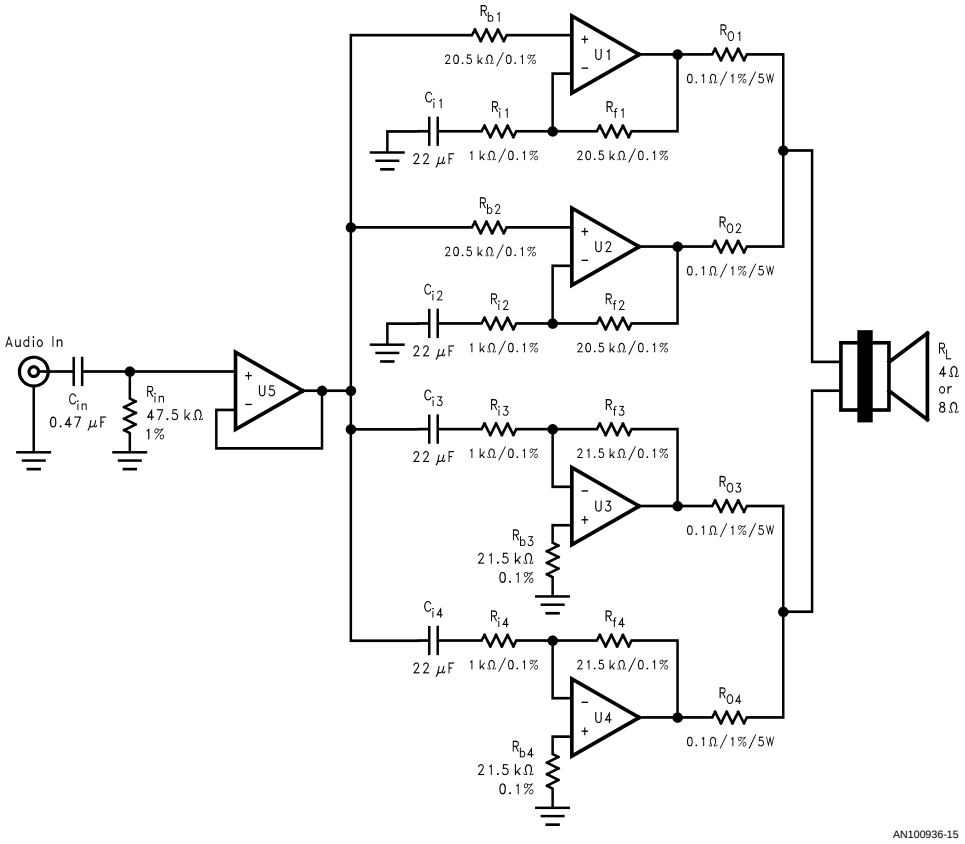
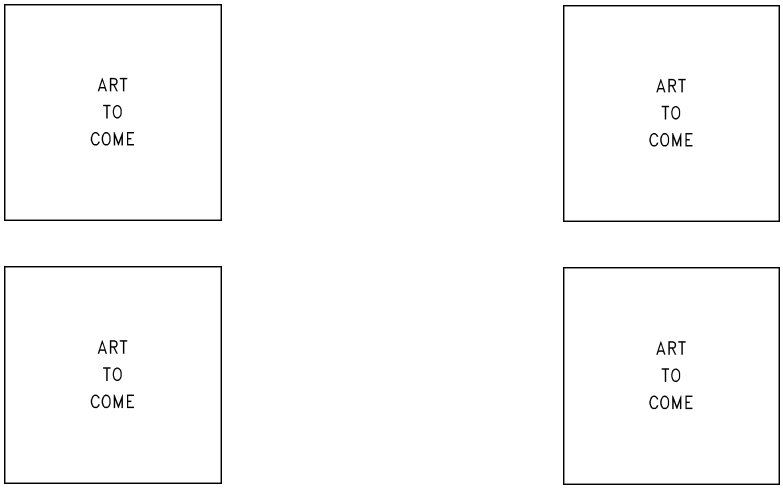
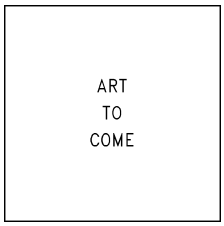


FIGURE 9. Bridge/Parallel Amplifier Schematic

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