

LVDS Quad Dynamic I_{CC} vs Frequency

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Dana Kagimoto
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LVDS OPERATION

LVDS (Low Voltage Differential Signaling) is a high speed general purpose interface that can be used in a wide range of application areas. Due to its small signal swing, differential signaling and current mode driver outputs, noise is minimized and very low power consumption across frequency is obtained.

The driver outputs consist of a current source which drives the differential pair. The receiver has high impedance so that the majority of the current flows across the 100 Ω termination resistor generating ~ 300 mV across the receiver inputs which have a threshold of less than 100 mV.

The transmission line (a cable or a controlled impedance printed circuit board) must be terminated and matched to its characteristic differential impedance to complete the current loop and terminate high speed signals. The accurate termination resistor, that is about 100 Ω and matches the media, must be placed across the differential signal lines as close to the receiver inputs as possible. If the medium is not properly terminated, signals that reflect from the end of the cable or trace may interfere with succeeding signals. EMI emissions are also reduced with proper termination.

LVDS COMPARED TO OTHER TECHNOLOGIES

Since LVDS technology is not dependent on a specific power supply, like some PECL and ECL technologies at 5V, maintaining the same signal levels and performance with lower power supply voltages of 5V, 3.3V and even less than 2.5V is easy to accomplish.

LVDS has a simple termination scheme that is easy to implement in most applications; whereas, PECL and ECL can require more complex termination than the one resistor LVDS solution. PECL drivers commonly require 220 Ω pull down resistors for each driver output along with 100 Ω resistor across the receiver input.

As mentioned before, EMI effects are reduced as signaling swings are much smaller than traditional CMOS, TTL or PECL.

FOCUS ON DYNAMIC I_{CC} VS FREQUENCY

This note will look at the presently offered LVDS quad receivers - the 5V DS90C032 and the 3.3V DS90LV032A - and the LVDS quad drivers - the 5V DS90C031 and the 3.3V DS90LV031A.

Receiver dynamic I_{CC} was measured with all four inputs simultaneously switching and TTL outputs with load capacitance of 8 pF simulating the PCB board trace and gate inputs. Driver dynamic I_{CC} was also measured with all four inputs simultaneously switching and LVDS outputs loaded with a 100 Ω load and board capacitance of ~ 25 pF.

Both the receivers and drivers were driven by a Tektronix HFS 9009 Stimulus System. The receiver input signal level was 1.1V to 1.3V (for a V_{ID} of 200 mV) and the driver signal level was 0V to 3V.

A comparison of the Dynamic I_{CC} of the two LVDS Quad Receivers is shown in *Figure 1*. The dynamic I_{CC} includes both the quiescent and load current of 4 channels. At low frequency, the dynamic I_{CC} of the two devices is stable at ~ 10 mA. It then rises to ~ 40 mA at 100 MHz and ~ 75 mA at 200 MHz. It can also be noted that the 5V device initially draws less current (~ 5 mA) than the 3.3V device (~ 10 mA) up to 30 MHz, then draws more current than the 3.3V device at the higher frequencies (~ 75 mA to ~ 60 mA). Both devices can run at high speeds (close to 300 Mhz) at reasonable power levels.

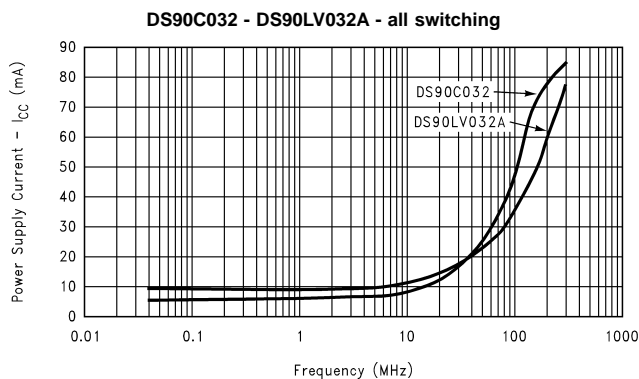


FIGURE 1. Dynamic I_{CC} vs Frequency of LVDS Quad Receivers

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In *Figure 2*, the 5V DS90C032 is shown with all four receivers switching compared to only one receiver switching with the other three inputs open. Once again, we see that at low frequencies, the dynamic I_{CC} is stable at ~ 7 mA, then rises

to ~ 75 mA with all four receivers switching and ~ 25 mA with a single receiver switching at 200 MHz. The substantial increase in power at high frequency is mainly a function of the output and load capacitance.

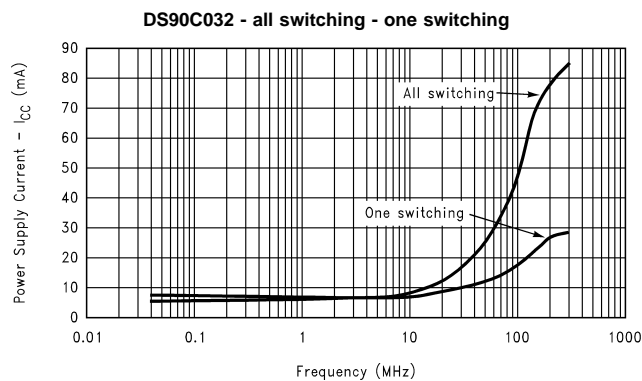


FIGURE 2. Dynamic I_{CC} vs Frequency of DS90C032

As you can see in *Figure 3*, the LVDS receiver dynamic I_{CC} is substantially lower than other industry data transmission standards of PECL and RS-422. Across all frequencies, the LVDS I_{CC} is one-third that of PECL and almost half that of RS-422.

Receiver Dynamic I_{CC} vs Frequency - all switching - TTL outputs unloaded

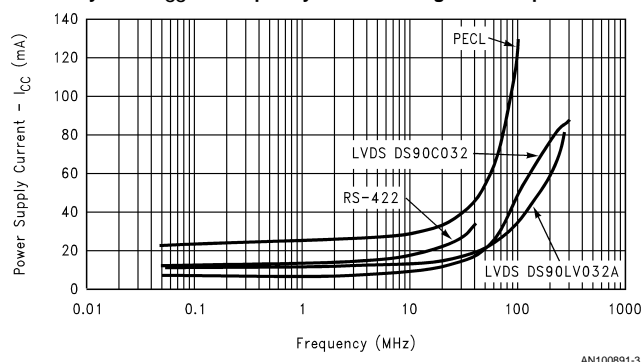


FIGURE 3. Dynamic I_{CC} vs Frequency of LVDS, PECL, and RS-422

A comparison of the Dynamic I_{CC} of the two LVDS Quad Drivers is shown in *Figure 4*. At low frequency, the dynamic I_{CC} of the two devices is stable at less than 20 mA. It then rises to ~ 22 mA at 100 MHz and ~ 28 mA at 200 MHz. It can also be noted that the 5V device initially draws less current

(~ 15 mA) than the 3.3V device (~ 21 mA) up to 140 MHz, then draws more current than the 3.3V device at the higher frequencies (~ 34 mA to ~ 27 mA). Both devices can run at high speeds (close to 300 MHz).

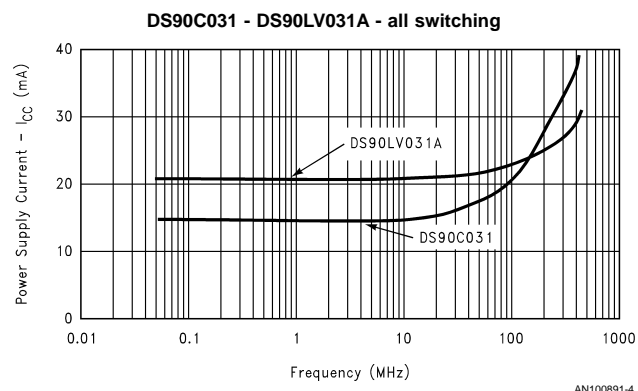


FIGURE 4. Dynamic I_{CC} vs Frequency of LVDS Quad Drivers

In *Figure 5*, the 5V DS90C031 is shown with all four drivers switching compared to only one driver switching with the other three inputs grounded through a 50Ω resistor. Once

again, we see that at low frequencies, the dynamic I_{CC} is stable at ~ 14 mA, then rises to ~ 28 mA and ~ 18 mA at 200 MHz.

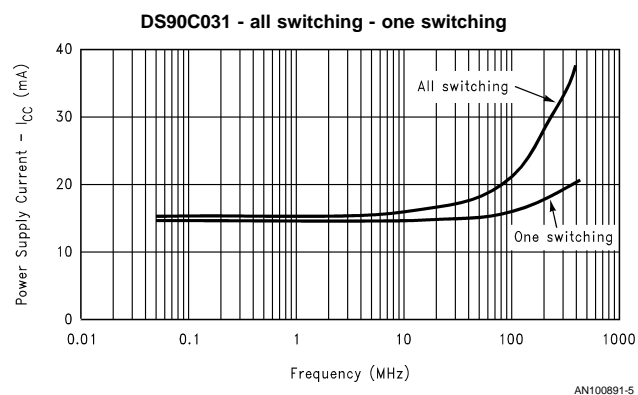
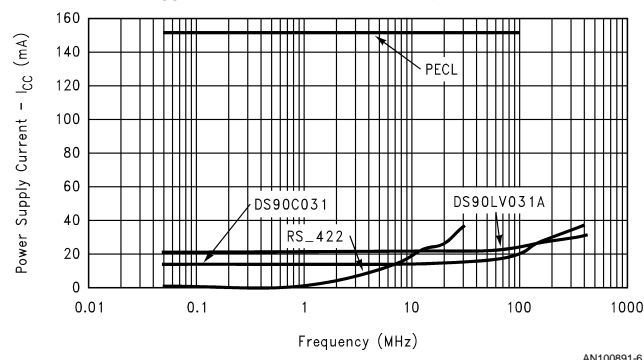


FIGURE 5. Dynamic I_{CC} vs Frequency of DS90C031

As you can see in *Figure 6*, the LVDS driver dynamic I_{CC} is substantially lower than other industry data transmission standards of PECL and RS-422. Across all frequencies, the LVDS I_{CC} is one-eighth that of PECL and comparable to RS-422. The low voltage swing feature of LVDS allows for this low power consumption along with high data rates.

LVDS signal levels (V_{OD} of ± 400 mV and V_{OH}/V_{OL} of 1.4V/1.0V) are 50% smaller than PECL (V_{OD} of ± 800 mV and V_{OH}/V_{OL} of 3.0V/2.2V) and 80% smaller than RS-422 (V_{OD} of 3V and V_{OH}/V_{OL} of 3.4V/0.4V). The lower voltage of LVDS allows for lower load current.

Driver Dynamic I_{CC} vs Frequency - all switching - LVDS outputs loadedFIGURE 6. Dynamic I_{CC} vs Frequency of LVDS, PECL and RS-422

LVDS technology can save power in several ways. The power dissipated by the load (the 100 Ω terminating resistor) is a mere 1.2 mW. In comparison, an RS-422 driver typically delivers 3V across a 100 Ω termination for 90 mW of power consumption. Similarly, LVDS devices require about one-tenth the power supply current of PECL and ECL devices.

In addition to lower power dissipation and static I_{CC} current, LVDS can lower system power through its CMOS current mode driver design. This design greatly reduces the frequency component of the I_{CC} . The I_{CC} vs frequency plot shows that for LVDS, it is virtually flat between 10 MHz to 100 MHz for the quad devices. Compare this to TTL/CMOS transceivers whose dynamic power consumption increases exponentially with frequency in the area of interest between 10 MHz to 100 MHz.

SUMMARY

LVDS is a high speed general purpose interface that can be used in a number of application areas. It is easy to implement AND has a simple single resistor termination scheme. This application note focused on Dynamic I_{CC} vs Frequency

for our presently offered LVDS quad receivers and drivers. It showed that the receiver dynamic I_{CC} is stable (~ 10 mA) at low frequencies (up to 10 MHz) and one-third that of PECL and almost half that of RS-422 across all frequencies. The driver dynamic I_{CC} is stable (~ 20 mA) at low frequencies (up to 50 MHz) and one-eighth that of PECL across all frequencies. RS-422 has a speed limitation and increasing dynamic I_{CC} at the upper frequency end. This difference in lower power consumption and higher speeds by LVDS over other industry data transmission standards is achieved by its differential low voltage signals and unique design.

REFERENCES

For additional information on LVDS applications and operation, please refer to the following guide that can be ordered through the Technical Response Group in Arlington, TX at 1-800-272-9959 or through the National website at: www.national.com

LVDS Owner's Manual - Design Guide

Publication #550062-001

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National Semiconductor Corporation
Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com

www.national.com

National Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
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Français Tel: +49 (0) 1 80-532 93 58
Italiano Tel: +49 (0) 1 80-534 16 80

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Fax: 65-2504466
Email: sea.support@nsc.com

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