Multi-Drop Channel-Link Operation

National Semiconductor
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CHANNEL-LINK OPERATION

The Channel-Link chipset is configured to provide high speed data transmission over a reduced size interconnect. With the 7 to 1 mux/demux architecture cable and connector reductions of up to 80% are possible. LVDS also provides a low noise system due to the use of current mode LVDS line drivers, a small signal swing of ~300 mV typical, and differential signaling. LVDS is also very noise tolerant, as the receivers support a tight 100 mV threshold and a wide ±1V common mode operating range. Standard LVDS devices are intended for single termination (100Ω) applications. The transmitter may be connected to a single receiver load (point-to-point) or may be connected to multiple receivers (multi-drop) when certain system design guidelines are adhered to. This is possible since the chipset provides transparent synchronous data transmission and requires no control (other than a power down pin). The transmitter only requires clock and data, and each receiver operates independent of the others. The scope of this application note is to discuss the specific recommendations for multi-drop applications.

CONFIGURATION

The transmission line connecting the transmitter outputs to the receiver inputs and the termination resistor is critical. It must be designed to minimize any transmission line effects (reflections) from mid-stream receivers to the down stream receivers. This can be done by employing a daisy chain bus structure. A daisy chain is formed by running from the transmitter to the first receiver, then the next, and so on. Branches off the main line are minimized, and termination is *only* at the extreme end of the line. A daisy chain is shown in *Figure 1*. Receiver input impedance is in the order of 100's of kΩ, therefore DC loading is not a problem even with a dozen or more receivers connected along the line. The AC loading and any imbalance introduced will be more of the limiting factor in determining how many receivers may be added to the bus. Testing done at National Semiconductor's Interface lab has successfully driven 5 receiver loads across 18 inches of flat ribbon cable in a daisy chain. Greater distances are possible by using higher quality cable such as twisted pair. Other configurations such as "Y" or "T"s as shown in *Figure 2* should be avoided.

The Y and T configurations present two transmission line problems. At point A, a reflection will occur due to the impedance change. The two legs each have an impedance of Z_O, but they are seen in parallel at the point, therefore at point A, there is a change of impedance from Z_O to $Z_O/2$, which will create a −33% reflection. A second problem also exists in regards to termination. Each leg should be terminated, ideally in Z_O Ω. Thus the transmitter will see a 50Ω DC load instead of the intended 100Ω load and this will cut in half the signal swing due to the current mode drivers (fixed amount of current). For these AC (reflection) and DC (50Ω) reasons the Y and T configurations should be avoided.

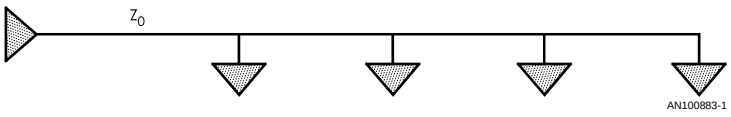

FIGURE 1. Daisy Chain Bus Configuration Supports Multi-drop Applications

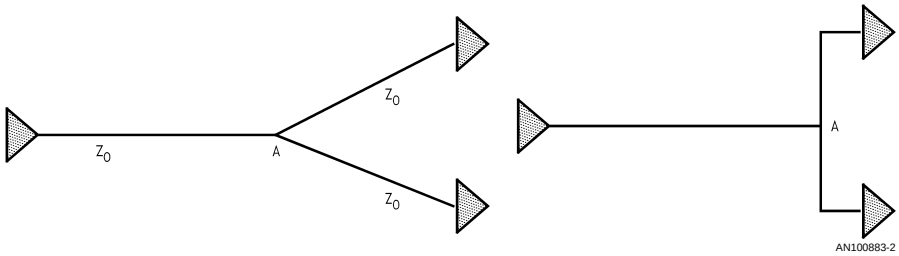

FIGURE 2. Avoid Y and T Configurations for Multi-drop Applications

STUBS & TERMINATION

Stubs are defined as the branch off the main line to the receiver inputs. These should be kept as short as possible to ensure that they appear as a lumped load to the transmission line and that a reflection does not occur at the high impedance inputs of the receiver. Stubs occur at the input of every receiver, including the last receiver. If PCB real estate is available the final receiver's layout may include the termination resistor(s). If PCB real estate is tight at the final receiver, then a fly-by termination may be employed. This is shown in *Figure 3*.

Stubs should be no longer than 1 inch in length, and the shorter the better. The use of surface mount chip resistors for the termination is recommended due to their small form factor, and low parasitics. 0805 packages are commonly employed.

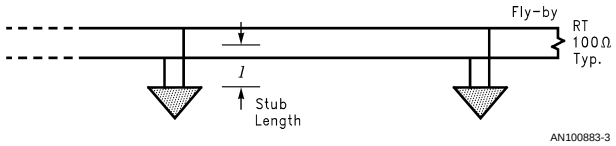

FIGURE 3. Fly-by Termination Provides Room for the Termination

LVDS PCB TECHNIQUES:

LVDS features fast edge rates, therefore the interconnect between transmitters and receivers will act as a transmission line. The PCB traces that form this interconnect must be designed with care. The following general guidelines should be adhered to:

- Hand route or review very closely auto-routed traces.
- Locate the Transmitters and Receivers close to the connectors to minimize PCB trace length for off PCB applications.
- Traces should be laid out for differential impedance control (space between traces needs to be controlled). See *Figure 4* and AN-905 for equations.
- Minimize the distance between traces of a pair to maximize common mode rejection.
- Place adjacent LVDS trace pairs at least twice as far away (as the distance between the conductors of the pair) (see *Figure 4*).
- Place TTL/CMOS (large dV signals) far away from LVDS, at least three times (>3S) away or on a different signal layer. (See *Figure 4*.)
- Match electrical length of all LVDS lines.
- Keep stubs as short as possible.
- Avoid crossing slots in the ground plane.
- Avoid 90˚ bends (use two 45s).
- Minimize the number of via on LVDS traces.
- Maintain equal loading on both traces of the pair to preserve balance.
- Match impedance of PCB trace to connector to media (cable) to termination to minimize reflections (emissions) for cabled applications (typically 100Ω differential mode impedance).
- Select a termination resistor to match the differential mode characteristic impedance of the interconnect, 2% tolerance is recommended.
- Locate the termination within 1/2 (<1) inch of the receiver inputs if not using a fly-by termination method.
- Use surface mount components to minimize parasitic L & C for bypass caps and termination resistors.
- Use a 4 layer PCB (minimum).
- Bypass each LVDS package at the device pin (Bulk bypass nearby also) with parallel capacitors (0.1 µF//0.01 µF//0.001 µF) on each of the supply pins (V_{CC}, $LVDSV_{CC}$, and $PLLV_{CC}$).

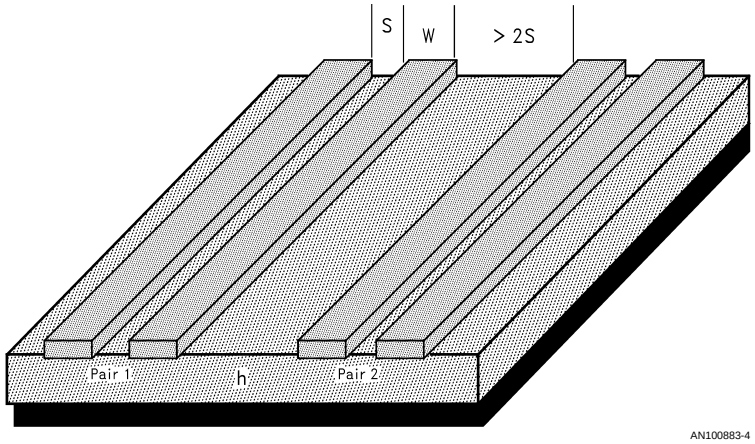

FIGURE 4. Differential Trace Layout (See AN-905)

SUMMARY

Channel-Link provides a versatile high speed data transmission system. It allows for many possibilities of configurations and deployments solving unique problems to special application needs. This application note focused on a distribution application where a Channel-Link Transmitter is connected to several Receivers. Bus configuration along with PCB recommendations were presented. Following these recommendations and guidelines will help ensure that the signal fidelity on the interconnect is maintained and supports error-free transmission.

REFERENCE

For additional information on Channel-Link applications and operation, please see the following application notes located on the National website at:

www.national.com

Topic	AP-Note ##
Channel-Link Overview	AN-1041
Sampling Margin and Skew Budgets	AN-1059
Parallel Application of Channel-Links	AN-1084

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