LM3641 Application Information Guide

National Semiconductor
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INTRODUCTION

The LM3641 Lithium Protection Integrated Circuit resides inside a 3.6V Lithium-Ion battery pack consisting of a single cell or multiple parallel cells. The IC controls the ON/OFF state of a pair of low threshold N-channel power MOSFETs placed in series with the battery cell(s). The purpose of this MOSFET pair is to protect the cell(s) from inadvertent electrical over-stress. The IC compares the cell voltage against internally programmed minimum and maximum limits.

The IC also monitors the bi-directional current flow in the battery pack by measuring the voltage across a robust 4 mΩ current sensing resistor internal to the protection IC package. The IC turns OFF the MOSFET pair whenever any fault limit is exceeded. The limits for overcharge and overdischarge voltage, as well as independent limits for each direction of overcurrent are factory adjusted employing EEPROM.

A Control pin allows external ON/OFF control of the MOSFET pair and resets the IC after the MOSFET pair is turned off and the pack is safe to operate again.

In this application note, there will be a description of the Low Cell Charge Enable (LCCE) feature and the Active Rectification (AR) feature.

LOW CELL CHARGE ENABLE FEATURE

Low Cell Charge Enable (LCCE) is a passive method of enabling the cell to be charged when the cell voltage is too low to keep the active IC circuitry operational. The circuit in *Figure 1* illustrates the effective signal path to the GATE pin of the IC resulting from a connection of a charger to the pack. The base of the PNP is pulled low with bias current from the charger through R1 and the NPN. The collector of the PNP pulls high on the GATE pin. When the cell voltage is high enough to power up the rest of the IC, the logic will short the base-emitter of the PNP with switch, S1. This occurs at about 1.4V. The logic is able to determine at this time if a charger is applied to the pack and turn on the normal switches that activate GATE = V_{DD} drive with switch S2.

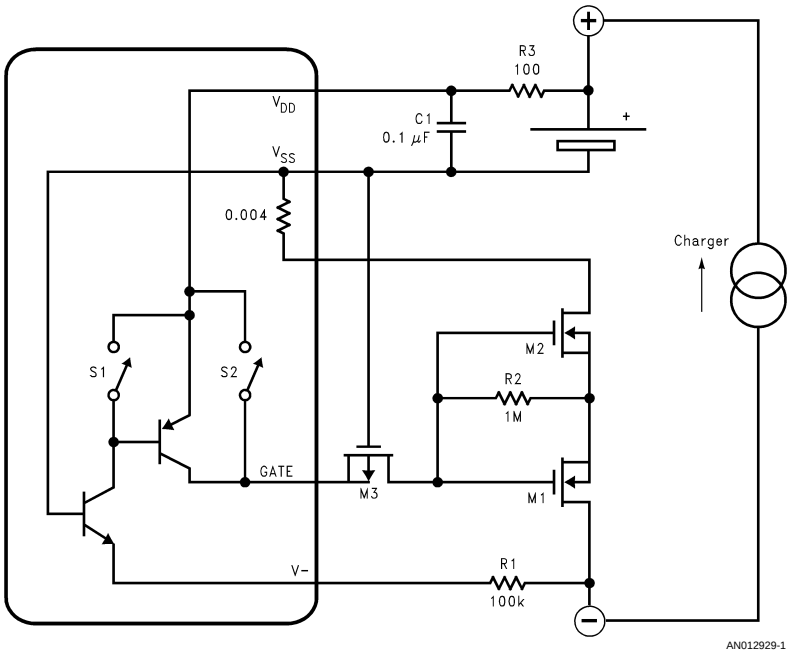

FIGURE 1. Low Cell Charge Enable Circuit

The various PCB voltages related to LCCE operation are shown in *Figure 2*. This plot illustrates the relative value of terminal voltages versus cell voltages that ranges from 0V to greater than V_{MAX}. The GATE pin of the IC tracks the cell voltage as it increases from 0V, except for a narrow flat region. This flat region occurs between the point that the M3 cascode can conduct and the logic of the IC powers up. The reason for the flat region will be explained. First, notice the gate voltage of the power MOSFETs M1 and M2. These FETs do not turn on until the initial conduction of M3 and also exhibit the flat region of operation. The power FETs' gate voltage equals the cell voltage beyond this region and below

V_{MAX}. Next, the IC's V− pin voltage is seen as being slightly below 0V (V_{SS}) whenever V_{CELL} is less than approximately 1.4V. This because the power FETs have not turned on, or fully turned on, the V− pin is pulled below 0V. The V− pin voltage is determined by the V_{BE} of the NPN for the bias current allowed by R1. The V− terminal of the pack follows the same track as the V− pin of the IC except during the flat region. This because during the flat region, the pack's V− terminal is set by the V_{GS} of the power FET's necessary to conduct the charger's compliance current. The pack's components operate in a feedback loop in the flat region. The PNP drive to the GATE pin can not pull any higher without also pulling the IC's V− pin higher, which would deprive base current to the PNP.

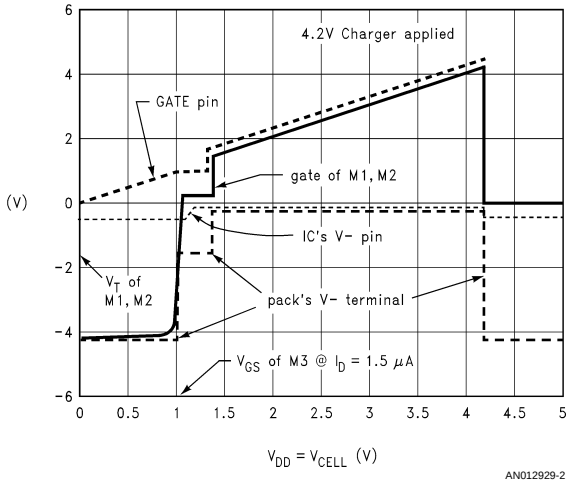

FIGURE 2. FET Drive vs CELL Voltage (Charging)

The cell voltage that allows the power FETs to initially conduct is determined by the threshold voltage of M3. When V_{CELL} = M3's $V_{GS(ON)}$ for $I_D \approx V_{T(M1)}/1\ m\Omega$, then the M1 and M2 are able to start conducting. This is also the start of the flat region. In the flat region loop that maintains the PNP in the active region keeps the power FETs on. Finally at ≈ 1.4V, the IC's logic will now pull the GATE pin high in open loop mode.

If at any time the charger is removed and the cell voltage is below V_{MIN}, then the GATE pin will turn off and the power FETs will not conduct.

ACTIVE RECTIFICATION FEATURE

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