Noise Floor Measurement of PLL Frequency Synthesizers

National Semiconductor
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INTRODUCTION

Phase noise is a critical performance parameter of frequency synthesizers for wireless applications. RF system designers of phase modulated cellular systems, such as PHS, GSM and IS-54, need low noise local oscillator (L.O.) or frequency synthesizer blocks. In phase modulated system the integrated phase noise of the synthesizer contributes to the RMS phase error of the transceiver. The frequency switching time and the suppression of reference spurs are also critical for these modern digital standards. A narrower loop filter bandwidth would decrease the integrated phase noise for the locked condition, but would increase the PLL lock time. A standard measurement technique for quantifying the phase locked loop noise generated by the synthesizer is described in this note.

PHASE NOISE SPECTRUM

Single sideband phase noise is a critical performance parameter of any frequency control system. Sideband noise can be converted into the frequency band of interest and reduce system sensitivity. A typical plot of a PLL noise characteristic is shown in *Figure 1*. When using a spectrum analyzer it can be safely assumed that both sides of the spectrum are identical. The integrated phase noise is not an "apples to apples" comparison for most systems, since this is highly dependent on the divider ratio, loop filter bandwidth, and damping or phase margin of the PLL. The spectrum peaking and loop bandwidth are functions of the loop bandwidth, while the noise "inside the loop" is generally proportional to the divider ratio. Noise outside the 3 dB loop bandwidth falls off rapidly, and does not contribute to the integrated noise significantly.

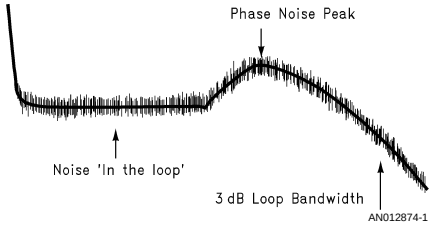


FIGURE 1. Single Sided Phase Noise Spectrum

The phase/frequency comparator's function is to adjust the voltage presented to the VCO until the feedback signal's frequency (and phase) match that of the reference signal. When this "phase-locked" condition exists, the VCO's frequency will be N times that of the comparison frequency. Where N is the programmable VCO divide ratio. It is assumed that any noise present at the input of the phase detector is multiplied up by a factor of N, and appears inside the loop of the PLL. This is generally synthesizer divider noise and phase detector noise. Obviously, this is an oversimplification of the noise properties of a PLL, but does serve as a way of normalizing phase noise measurements.

PHASE NOISE FLOOR MEASUREMENT

The basic phase-lock-loop configuration we will be considering is shown in *Figure 3*. The PLL consists of a high-stability crystal reference oscillator, a frequency synthesizer such as the National Semiconductor LMX2332TM, a voltage controlled oscillator (VCO), and a passive loop filter. The crystal reference used is the 10 MHz signal from the back of a spectrum analyzer at about +7 dBm or 1.42 V_{PP}. The VCO used for this test was an ALPS URAE8x934 VCO with a tuning constant of 27 MHz/V phase locked at 900 MHz. By using a relatively wide loop filter bandwidth, (15 kHz for N = 4500) we are able to vary the reference frequency from 30 kHz to 400 kHz without changing the component values and maintain loop stability. The phase noise measurements were made at 150 Hz offset, to ensure that the data was on the flat portion of the curve "inside the loop". At least 20 video averages were taken over a 1 kHz span for each measurement. In order to come up with the phase noise floor figure of merit the spectrum analyzer measurement must be normalized in terms of dBc/Hz, by subtracting 10 log of the resolution bandwidth used in the measurement. The noise is then referenced to the input of the phase detector by subtracting 20 log N. Without taking into account any errors from the spectrum analyzer we have:

$$\text{Phase Noise Floor} = \left(\text{Phase Noise from S. A.}\right) - 10 \log \left(\frac{\text{S.A. Res BW}}{}\right) - 20 \log N$$

SUMMARY

A graph showing the phase noise floor of the LMX2332A vs. phase detector frequency is shown in *Figure 2*. This shows the phase noise floor is not solely dependent on the divider ratio N. The phase noise floor for a 900 MHz VCO frequency and a channel spacing of 30 kHz, is less than −169 dBc/Hz.

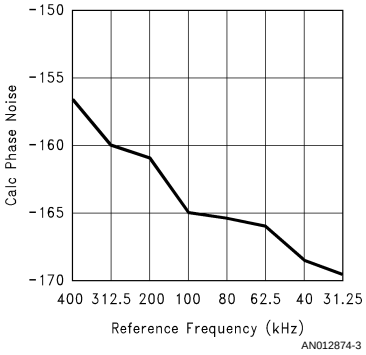


FIGURE 2. LMX2332 Phase Noise Floor

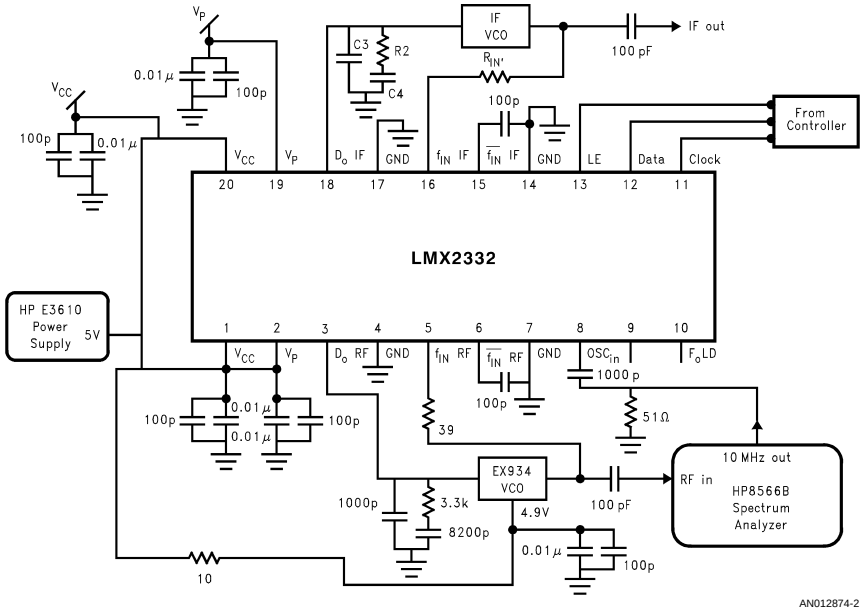
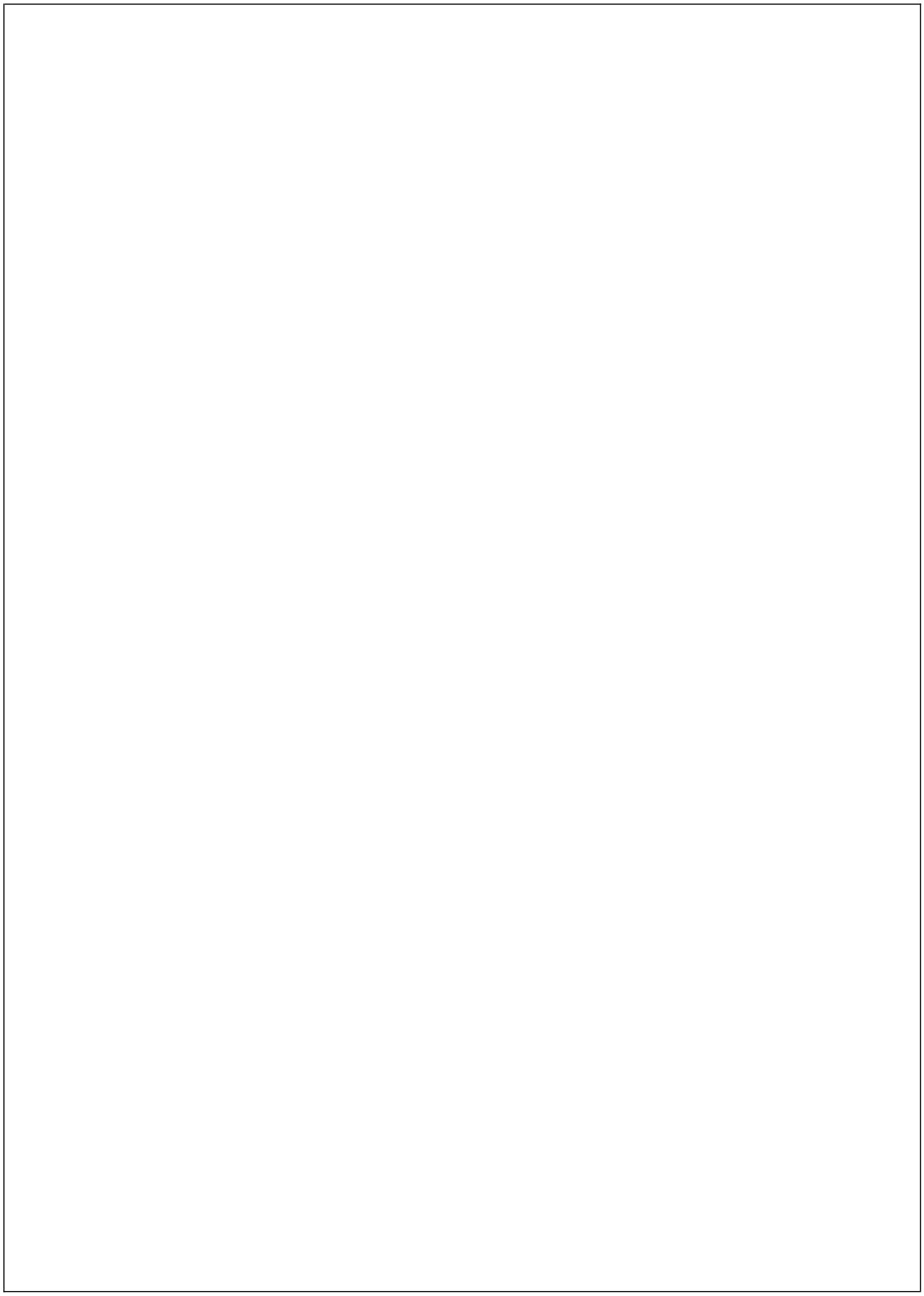


FIGURE 3. Measurement Setup



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