DP8408A/9A Fastest DRAM Access Mode

National Semiconductor
Application Brief 9
Tim Garverick
Rusty Meier
January 1986

If one desires the fastest possible operation of the DP8408A/9A multi-mode dynamic RAM controller/driver in accessing DRAMs, mode 4, externally controlled access mode should be considered.

In using mode 4 there are three input signals which must be considered:

1) $\overline{\text{RASIN}}$—generates $\overline{\text{RAS}}$
2) R/$\overline{\text{C}}$—switches between rows and columns on the address outputs
3) $\overline{\text{CASIN}}$—generates $\overline{\text{CAS}}$

In producing these signals a delay will be needed between $\overline{\text{RASIN}}$ and R/$\overline{\text{C}}$ and between R/$\overline{\text{C}}$ and $\overline{\text{CASIN}}$. (**Note:** In mode 4 external generation of $\overline{\text{CASIN}}$ can produce $\overline{\text{CAS}}$ faster than automatic generation of $\overline{\text{CAS}}$.)

Two important parameters have been added to the DP8408A/9A data sheets that help one compute the minimum acceptable delays between the above-mentioned signals. These parameters are:

1) t_{DIF1} = MAXIMUM ($t_{RPDL} - t_{RHA}$) = 13 ns
   where t_{RPDL} = $\overline{\text{RASIN}}$ to $\overline{\text{RAS}}$ delay
   t_{RHA} = row address held from column select
2) t_{DIF2} = MAXIMUM ($t_{RCC} - t_{CPDL}$) = 13 ns
   where t_{RCC} = column select to column address valid
   t_{CPDL} = $\overline{\text{CASIN}}$ to $\overline{\text{CAS}}$ delay

These parameters are specified as being less than what would be calculated using the min/max values given for t_{RCC}, t_{CPDL}, t_{RPDL} and t_{RHA} in the DP8408A/9A specification sheets, because on-chip delays track over temperature and supply variations.

The equation for the delay between $\overline{\text{RASIN}}$ and R/$\overline{\text{C}}$ that guarantees the specified DRAM t_{RAH} is:

min delay required = $t_{DIF1} + t_{RAH}$
= 13 ns + t_{RAH}
where t_{RAH} = DRAM minimum row address hold time from $\overline{\text{RAS}}$

The equation for the delay between R/$\overline{\text{C}}$ and $\overline{\text{CASIN}}$ that guarantees the specified DRAM t_{ASC} is:

min delay required = $t_{DIF2} + t_{ASC}$
= 13 ns + t_{ASC}
where t_{ASC} = DRAM minimum column address set-up time to $\overline{\text{CAS}}$

To produce the above-mentioned delays between signals, a ±2 ns resolution delay line can be used as follows:

(assuming t_{RAH} = 20 ns, t_{ASC} = 0 ns)
$\overline{\text{RASIN}}$ to R/$\overline{\text{C}}$ delay = 13 ns + 20 ns
= 33 ns
R/$\overline{\text{C}}$ to $\overline{\text{CASIN}}$ delay = 13 ns + 0 ns
= 13 ns

Thus, R/$\overline{\text{C}}$ must follow $\overline{\text{RASIN}}$ by a minimum of 33 ns and $\overline{\text{CASIN}}$ must follow R/$\overline{\text{C}}$ by a minimum of 13 ns. With a delay line of ± 2 ns resolution, the $\overline{\text{RASIN}}$ to R/$\overline{\text{C}}$ and R/$\overline{\text{C}}$ to $\overline{\text{CASIN}}$ delays can be typicals of 35 ns and 15 ns, respectively. (See *Figures 1* and *2*.)

This scheme will provide a maximum $\overline{\text{RASIN}}$ to $\overline{\text{CAS}}$ delay of:

35 ns + 15 ns + 2 ns (resolution uncertainty)
+ MAXIMUM (t_{CPDL}) = 52 ns + MAXIMUM (t_{CPDL})

For the DP8408/9-2, MAXIMUM (t_{CPDL}) = 58 ns.

For the DP8408A/9A (no dash), MAXIMUM (t_{CPDL}) = 68 ns (not 58 ns as indicated in data sheets up to November 1982).

The fastest mode 4 accesses (with the assumed delay line and DRAM parameters) are therefore, 110 ns and 120 ns, respectively, for the -2 and non-dash parts.

The maximum $\overline{\text{RASIN}}$ to $\overline{\text{CAS}}$ delay (t_{RICL}) in mode 5 (auto mode) for the DP8408/9-2 (which guarantees a min t_{RAH} of 20 ns) is 130 ns. The maximum t_{RICL} in mode 5 for the DP8408A/9A (no dash) is 160 ns.

Thus, it is shown that if the features offered by the DP8408A/9A automatic modes can be sacrificed, mode 4 (externally controlled access) may be used to obtain the fastest memory access.

RRD-B30M105/Printed in U. S. A.

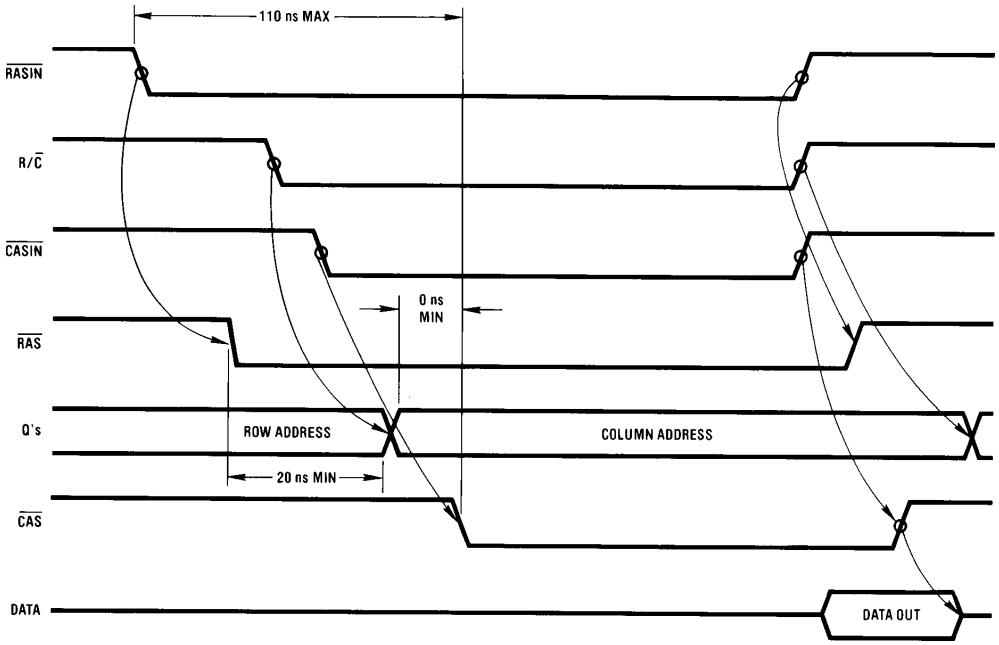
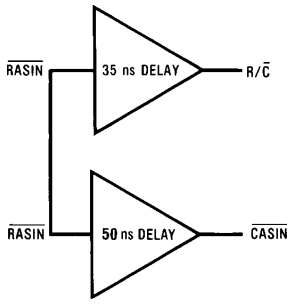


FIGURE 1. Mode 4 Timing Relationships

TL/F/8403–1



TL/F/8403–2

FIGURE 2. Mode 4 Externally Generated Signals

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408