A Method for Efficient Task Switching Using the NS32381 FPU

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INTRODUCTION

Many microprocessor based embedded control systems are built as real-time multitasking systems where different functions of the system are controlled by different tasks. The multiple tasks in such a system have the appearance of all executing simultaneously, when in reality only one task is running on the processor at one time. (Readers not familiar with the concepts of *tasks* and *multitasking* can find explanations in most general textbooks about operating systems.)

A *task switch* is when one task stops executing and another begins executing. A task switch usually involves saving the values of the processor's registers onto the stack. In systems where both a Central Processor Unit (CPU) and a Floating Point Unit (FPU) are used, the registers of both processors must be saved. However, if the FPU has not been used during the execution of a task, saving its registers onto the stack is unnecessary and is an undesirable waste of time. This application brief is for the software designer of an embedded software system. It explains how to detect when the FPU has not been used in a task so the task switch time can be shortened by not saving the FPU registers.

METHOD

The Floating Status Register (FRS) *(Figure 1)* of the NS32381 has a Trap Type field (bits 0–2) that records any exceptional conditions detected by a floating point instruction. The Trap Type field is loaded with zero whenever any floating point instruction except LFSR (Load Floating Status Register) or SFSR (Store Floating Status Register) completes without encountering an exception condition.

Seven Trap Type codes are used to signal the different conditions (including the code "000" that is used to indicate "no exception"). One code "111" is not used.

Loading the FSR at the beginning of every task with a value that sets the Trap Type field to the unused code "111" lets the FSR be used later to determine whether the NS32381 has been used in the task. If the Trap Type code at the end of the task is still "111", it means that no floating point instruction has been executed since the FSR was loaded.

The execution figures below refer to a system that uses the NS32381 FPU with the National Semiconductor NS32GX32 CPU. This method also works with the NS32CG16 processor.

Saving the floating point registers onto the stack using routine 1 *(Figure 2)* described below takes 296 clock cycles. In cases where it is possible that the NS3281 has not been referenced in the current task, routine 2 *(Figure 3)* can be executed prior to saving the registers. This routine takes 43 cycles. In cases when the Floating Point Unit has not been referenced, 253 clock cycles (85.5%) are saved. If the FPU has been referenced, 43 cycles are added to the 296 cycles of the normal routine (extra 14.5%)

These numbers indicate that whenever the probability of not using the FPU is greater than 14.5% this method is efficient.

Routine #1

```
save_freg:   sfsr   tos
             movl   l0, tos
             movl   l1, tos
             movl   l2, tos
             movl   l3, tos
             movl   l4, tos
             movl   l5, tos
             movl   l6, tos
             movl   l7, tos
```

FIGURE 2

Routine #2

```
             sfsr   tos
             andb   h'7, r0
             cmpb   h'7, r0
             beq    end
save_freg:   sfsr   tos
             movl   l0, tos
             movl   l1, tos
             movl   l2, tos
             movl   l3, tos
             movl   l4, tos
             movl   l5, tos
             movl   l6, tos
             movl   l7, tos
             •
             •
             •
end:
```

FIGURE 3

NS32381 FPU Status Register (FSR)

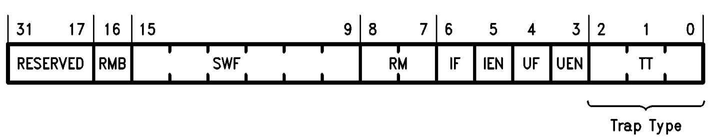

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FIGURE 1

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