The DP8490 and DP5380 Comparison Guide

National Semiconductor
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OVERVIEW

National Semiconductor has released two products to support the Small Computer System Interface (SCSI). These two products offer significant features over existing asynchronous SCSI devices such as:

- Lower power (25 mW vs 700 mW)
- Lower cost
- Higher speed (up to 4 Mbytes/sec)
- More functionality
- Compatibility (with existing NCR5380)

FEATURES OF NATIONAL's DP8490 & DP5380

Low Power

The DP8490 Enhanced Asynchronous SCSI Interface (EASI) and the DP5380 Asynchronous SCSI Interface (ASI) are CMOS devices. The current drawn by the NCR5380 is 140 mA while both the EASI and the ASI draw 4 mA max—*and* the EASI/ASI are specified with SCSI pins terminated with SCSI spec values!

Low Cost

National's marketing strategy will ensure the EASI and ASI are the most competitively priced parts on the market.

High Speed

The high speed CMOS process used for the EASI and ASI means that DMA rates of up to 4 Mbytes per second are achievable. Currently there are no low cost high speed 8-bit DMA controllers that will provide the necessary speed. A common solution is to provide the simple DMA functionality as part of ASIC circuitry normally found in each application. National has published an application note on how to build a 4 Mbytes/sec asynchronous SCSI interface using the EASI/ASI devices to assist designers.

The user should be aware that with this increase in speed comes the need and care on the user's part in board design and layout. The EASI and ASI have reduced: read access times from 140 ns to 50 ns, write data hold times from 30 ns to 10 ns, and all other parameters correspondingly. This means the designer should ensure he has correctly generated chip strobes. In particular pay attention to the generation of DACK, and the period of hand-over of the bus between the DMA and CPU.

Improved Functionality

The EASI provides new and enhanced functions to ease the firmware overhead. The major features are:

new interrupts
new interrupt status and mask structure
extended arbitration
loopback and other testing facilities
microprocessor data bus parity
improved SCSI and DMA timing

New Interrupts

The EASI adds interrupts for: arbitration complete, any phase mismatch, true end of DMA and microprocessor parity error. The arbitration complete interrupt allows the firmware to program the EASI to arbitrate for the bus and interrupt when done. True End of DMA interrupt overcomes the fault in the DP5380 when using it to *send* data on SCSI.

New Interrupt Structure

The DP5380 cannot be fully interrupt driven (e.g., no arbitration complete interrupt)—the DP8490 can be! In the DP5380 the firmware must read 2 registers and then process the results to determine the cause of an interrupt. Not all interrupt conditions have a status bit in the DP5380. The DP8490 provides an interrupt status register which gathers all status into one register, with a dedicated status bit for each interrupt. An interrupt mask register provides individual masking control of each interrupt. Finally, the design of the interrupt logic ensures interrupts will not be lost (they can be on the DP5380).

Extended Arbitration

The DP5380 device must be polled by the μP during arbitration. Since this process does not start until the bus is free, the μP may be polling for many milliseconds. The DP8490 provides an interrupt on arbitration complete to allow the μP to handle other tasks such as cacheing data, overlapped seeks etc. The DP8490 also implements the 2.2 μs SCSI arbitration delay before interrupting the μP.

Loopback Testing

The DP8490 provides a loopback test mode. Each SCSI pin driver is disabled and looped back internally. The firmware may exercise the EASI to verify correct part operation. SCSI signal driving and monitoring, interrupts and DMA can all be tested. The EASI also provides programmable parity polarity (EVEN/ODD) for both μP and SCSI buses. These bits may be used to verify parity circuitry on all boards in a SCSI system.

Microprocessor Parity

The PCC-packaged DP8490 provides an extra pin for μP data bus parity. This enables checked data to be maintained throughout a system—even including controller buffer memory.

Improved Timing

The DP5380 has some timing anomalies just like the NCR5380 on the SCSI and μP interfaces. The DP8490 fixes these.

COMPATIBILITY

The DP5380 is *completely* compatible with existing NCR5380 type devices—but offers higher speed and lower power.

The DP8490 is also completely compatible with existing NCR5380 type devices except for one register bit. An unused ''test-mode'' bit in the NCR5380 is replaced by an ''Enhanced Mode'' bit in the DP8490. Until this bit is set the DP8490 functions as a DP5380. Once set the enhanced features of the DP8490 are accessible. Since the DP8490 powers up in DP5380 mode *all DP5380 sockets should be able to use a DP8490!*

For more information see Section 8 of the DP8490 datasheet.

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