Receiver Interrupts/Flags for the DP8344 Biphase Communications Processor

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The DP8344 has a flag that corresponds to each of its interrupts except NMI. This allows the BCP to operate efficiently in either an interrupt driven or polled environment and gives the user the flexibility to combine the two. However, one must be aware that even though the names are the same, their controls may be different. The event that controls when the interrupt and its corresponding flag is asserted or cleared may not be the same. However, this is only the case for the three receiver interrupts; the other 8344 interrupts are set and cleared in exactly the same manner as their associated flag. To easily discuss these subtle differences, it should be made clear that the transceiver reset does clear all the receiver flags and interrupts and that this will not be mentioned when discussing the individual receiver interrupts below.

To begin with, the receiver active (RA) interrupt and flag are both asserted by the same event; the receiver detecting two or three line quiescents, depending on the state of Receive Line Quiescent (RLQ), followed by a code violation and a sync bit. However, the RA interrupt is cleared by reading the {RTR} or {ECR} register while the RA flag is cleared by an error or the end of the transmission. The receiver identifies the end of the transmission by detecting a mini code violation in all protocols except 5250, and in 5250 by waiting for the Line Active (LA) flag to time out after fill bits are received. The data available (DA) interrupt and flag are both asserted when a byte is present on the output of the FIFO. However, the DA interrupt also becomes active when an error is detected by the receiver. They are both cleared by reading the {RTR} register until the FIFO is empty, but the DA flag will also be cleared when an error is detected. The situation is similar with the receive FIFO full interrupt and flag. They are both asserted when three words are present in the FIFO, but the RFF interrupt also becomes active when an error is detected. Both the RFF flag and interrupt are cleared exactly the same way by reading the RTR register.

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