Use of the NS32332 with the NS32082 and the NS32201

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Care should be taken when the NS32332 is designed in a system with the NS32201 and the NS32082. Two configurations need to be considered, one with MMU and one without.

In a configuration without an MMU, TCU and CPU both run a four clock cycle bus (*Figure 1*). The RDY signal is the only incompatible signal between the CPU and TCU and therefore the RDY output of the TCU should not be directly connected to the RDY input of the NS32332. The NS32332 samples its RDY input in the middle of T3 while the NS32201 asserts its RDY output shortly after the middle of T2 and removes it shortly after the middle of T3, thus the NS32332 RDY input hold time (tRDYh) is not met. To meet tRDYh, the RDY output of the NS32201 should be clocked by the rising edge of the CTTL using a D-type flip-flop (74AS74) and then taken to the NS32332. It should be noted that the NS32332 outputs the data in a write cycle in T3 unless DT/SDONE pin is sampled low on the rising edge of the reset in which case the data is output during T2. The DT/SDONE pin is implemented as of revision B of the NS32332.

In a configuration with MMU the NS32332 runs a four clock cycle bus while the NS32082 runs a five cycle bus. Two options can be exercised.

The first option is extending the NS32332 bus cycle to five clocks by adding a blind wait state that bypasses the NS32201 (*Figure 2*). This configuration generally requires the minimum hardware modification for a 320xx based design to run the NS32332. Here the NS32201 output signals can be used to interface the NS32332 and the NS32082 to the memory or I/O. Additional wait states can be inserted by clocking the RDY output of the TCU.

The second option is to have the NS32332 run a four clock cycle bus (*Figure 3*). In this configuration the NS32201 output signals cannot be used to interface the NS32332 to memory or I/O; they can only be used to interface the NS32082 to the memory. In this configuration a revision N of the NS32082 should be used.

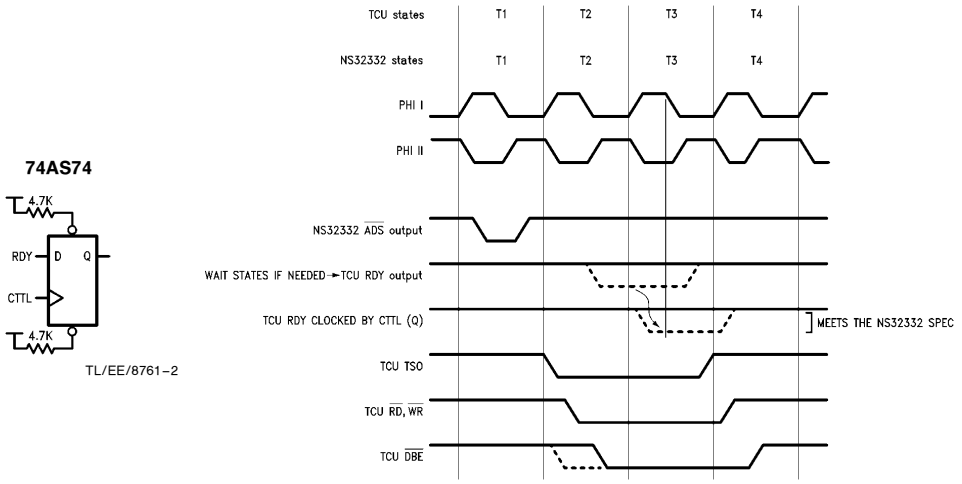

FIGURE 1. NS32332, TCU Timing Diagram, No Wait State, No MMU

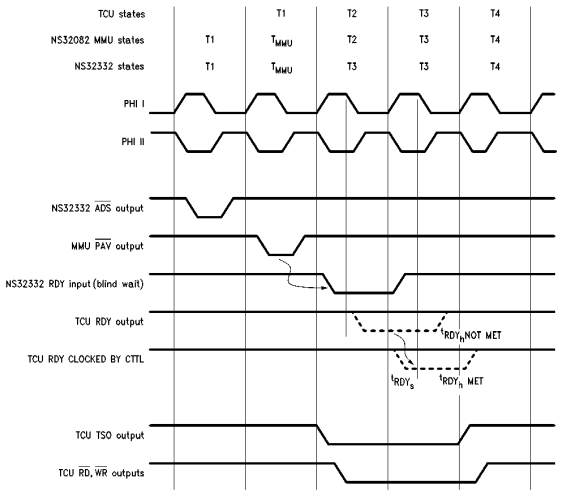

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FIGURE 2. NS32332, MMU, TCU Timing Diagram when NS32332 is Run with 1 Wait State Similar to Timing Diagram of NS32332 Adapter to DB32000

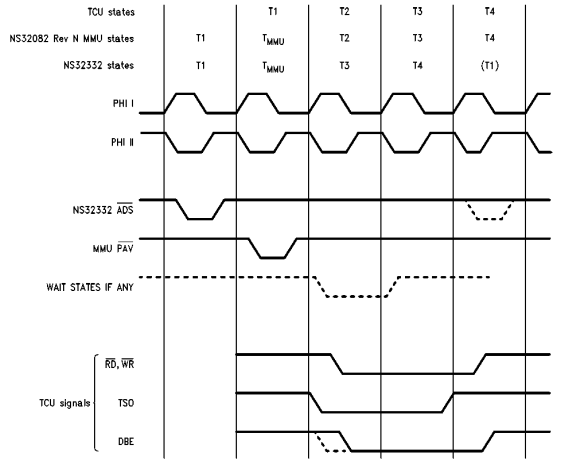

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FIGURE 3. NS32332, MMU, TCU Timing Diagram with No Wait State

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National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408