DP8408A/09A/17/18/19/28/29 Application Hints

National Semiconductor
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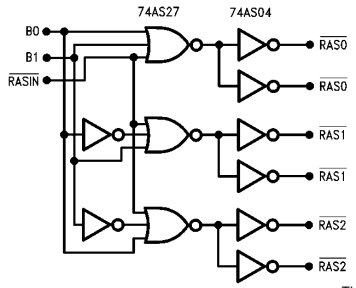
The DP8408A, DP8409A dynamic RAM controllers have been well received by dynamic memory users because they perform functions formerly requiring multiple integrated circuit chips. These controllers are designed to be suitable for a variety of DRAM control methods. As a result of the many combinations of ways in which inputs to these chips may be varied, it was inevitable that certain conditions exist that would cause the DP8408A, DP8409A to respond in an undesirable way. Feedback from customers using these chips has resulted in thorough investigations of such conditions. The following are constraints on the use of the DRAM controllers which are not addressed in their data sheets. The majority of customers will find that most of the items on this list are not pertinent to their particular application, and those that are impose minimal restrictions.

1) The on-chip refresh counter resets when the RFI/O pin goes low for a refresh request in mode 5 if this pin is excessively loaded with capacitance. The data sheet suggests that this pin not be loaded with greater than 50 pF. Since RFI/O, in most cases, needs only to drive a low capacitance in a refresh control circuit, this limit is not unreasonable.
2) When the DP8408A, DP8409A is in a refresh mode, the RFI/O pin indicates that the on-chip refresh counter has reached its end-of-count. This end-of-count is selectable as 127, 255 or 511 (511 is available only on the DP8409A) to accommodate 16k, 64k or 256k DRAMS, respectively. Although the end-of-count may be chosen to be any of these, the counter always counts to 511 (255 for the DP8408A) before rolling over to zero.
3) When going from mode 0, 1 or 2 (refresh) to mode 5 of the DP8408A, if $\overline{\text{CASIN}}$ and R/$\overline{\text{C}}$ are both low, a glitch occurs on the $\overline{\text{CAS}}$ output. Since neither of these inputs is used in these modes, one or both should be held high.
4) Most DRAMs specify 0 ns row address set-up time to $\overline{\text{RAS}}$. In order to guarantee this, the row address to the DP8408A, DP8409A must be valid 10 ns before $\overline{\text{RASIN}}$ transitions low to initiate an access. In terms of the data sheet parameters, maximum ($t_{APD} - t_{RPDL}$) = 10 ns.
5) When changing modes from refresh to access, again sufficient time must be allowed for the row address to be valid before $\overline{\text{RAS}}$ occurs. In this case, the address outputs of the DP8408A, DP8409A are changing from the refresh counter to the row address inputs. In order for the row address to be set up a minimum of 0 ns before $\overline{\text{RAS}}$ goes low, $\overline{\text{RASIN}}$ should not go low until 30 ns after the change from refresh to access mode.
6) Both the low and high pulse widths of $\overline{\text{RAS}}$ have minimum requirements during refresh. When in mode 0, the $\overline{\text{RASIN}}$ to $\overline{\text{RAS}}$ low delay is longer than the $\overline{\text{RASIN}}$ to $\overline{\text{RAS}}$ high delay. In terms of the data sheet parameters, maximum ($t_{RFPDL} - t_{RFPDH}$) = 25 ns. Thus, the minimum low pulse width of $\overline{\text{RAS}}$ in mode 0 equals the $\overline{\text{RASIN}}$ low pulse width minus 25 ns. The minimum high pulse width of $\overline{\text{RAS}}$ in mode 0 equals the $\overline{\text{RASIN}}$ high pulse width.
7) The fastest memory access may be accomplished using mode 4 and external delay lines (see App. Brief #9).
8) In the data sheet, it is specified that $\overline{\text{CS}}$ should go low 30 ns (t_{CSLR}) before $\overline{\text{RASIN}}$ goes low to initiate an access in mode 5. This is to prevent the possibility of a glitch on the $\overline{\text{RAS}}$ outputs, resulting from the DP8409A interpreting the $\overline{\text{RASIN}}$ as a hidden refresh. For the same reason, $\overline{\text{CS}}$ should be held low for a minimum of 15 ns after $\overline{\text{RASIN}}$ returns high, ending the access in mode 5.
9) If the DP8409A is being used in mode 5 and $\overline{\text{CS}}$ = 1, and if $\overline{\text{RASIN}}$ goes low within 15 ns before RFCK (R/$\overline{\text{C}}$) goes low, up to a 15 ns glitch may occur on the refresh request pin, RFI/O. However, since $\overline{\text{CS}}$ is high, a hidden refresh will occur as it normally would with RFCK high. If the glitch on RFI/O were detected and interpreted as a forced refresh request, no forced refresh would be allowed by the DP8409A since a hidden refresh was allowed. This would not cause any problem, however, since the hidden refresh has taken care of the refresh requirement for that period of RFCK. Also, this forced refresh request could not be detected if the system does not check RFI/O for a low state while $\overline{\text{RASIN}}$ is low (i.e., an access is taking place).
10) At CPU clock frequencies of 10 MHz and above it is suggested that the hidden refresh capability of the DRAM controller (DP8409/17/19/29) be disabled. The main reason for this suggestion is to satisfy the parameter "t_{RKRL}" (RFCK high to $\overline{\text{RASIN}}$ low for hidden refresh) which is given as a minimum of 50 ns in the DP8417/19/29 data sheets. Disabling hidden refresh also eliminates the need of meeting the parameter of "t_{CSRL1}" ($\overline{\text{CS}}$ low to access $\overline{\text{RASIN}}$ low using Mode 5 with hidden refresh capability) which is given as a minimum of 34 ns in the DP8417/19/29 data sheets. In order to eliminate hidden refresh the "$\overline{\text{CS}}$" pin of the DRAM controller should be permanently grounded on the DRAM controller, and the "$\overline{\text{CS}}$" that previously went to the DRAM controller should be "ORed" with "$\overline{\text{RASIN}}$" (the "OR" gate's output becoming the new "$\overline{\text{RASIN}}$" input to the DRAM controller).
11) If the user desires to improve the DRAM controller "$\overline{\text{RASIN}}$ to $\overline{\text{RAS}}$ out" time ("tRPDL") external logic may be used to create multiple "$\overline{\text{RAS}}$s". The circuit shown below requires only several 74XX oxide isolated type IC's (74AS27 and 74AS04) to accomplish this aim. To use this circuit $\overline{\text{RASIN}}$ should transition low during refreshes.



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