Instruction Execution Times of FPU NS32081 Considered for Stand-Alone Configurations

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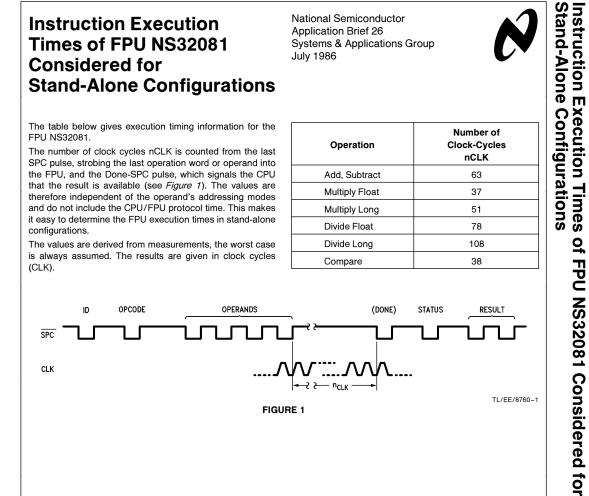


The table below gives execution timing information for the FPU NS32081.

The number of clock cycles nCLK is counted from the last SPC pulse, strobing the last operation word or operand into the FPU, and the Done-SPC pulse, which signals the CPU that the result is available (see Figure 1). The values are therefore independent of the operand's addressing modes and do not include the CPU/FPU protocol time. This makes it easy to determine the FPU execution times in stand-alone configurations.

The values are derived from measurements, the worst case is always assumed. The results are given in clock cycles (CLK).

| Operation | Number of Clock-Cycles nCLK | |
|----------------|-----------------------------------|--|
| Add, Subtract | 63 | |
| Multiply Float | 37 | |
| Multiply Long | 51 | |
| Divide Float | 78 | |
| Divide Long | 108 | |
| Compare | 38 | |



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