

74F779

8-Bit Bidirectional Binary Counter with 3-STATE Outputs

General Description

The 'F779 is a fully synchronous 8-stage up/down counter with multiplexed 3-STATE I/O ports for bus-oriented applications. All control functions (hold, count up, count down, synchronous load) are controlled by two mode pins (S_0, S_1). The device also features carry lookahead for easy cascading. All state changes are initiated by the rising edge of the clock.

- Built-in lookahead carry capability
- Count frequency 100 MHz typ
- Supply current 80 mA typ
- Guaranteed 4000V minimum ESD protection
- Available in SOIC (300 mil only)

Features

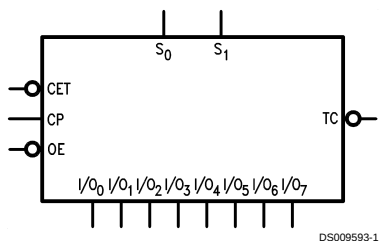
- Multiplexed 3-STATE I/O ports

Ordering Code:

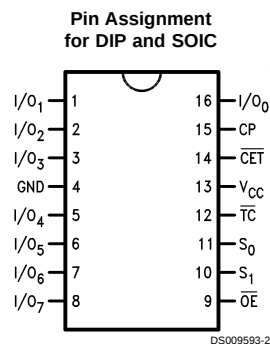
Commercial	Package Number	Package Description
74F779PC	N16E	16-Lead (0.300" Wide) Molded Dual-In-Line
74F779SC (Note 1)	M16B	16-Lead (0.300" Wide) Molded Small Outline, JEDEC

Note 1: Devices also available in 13" reel. Use suffix = SCX.

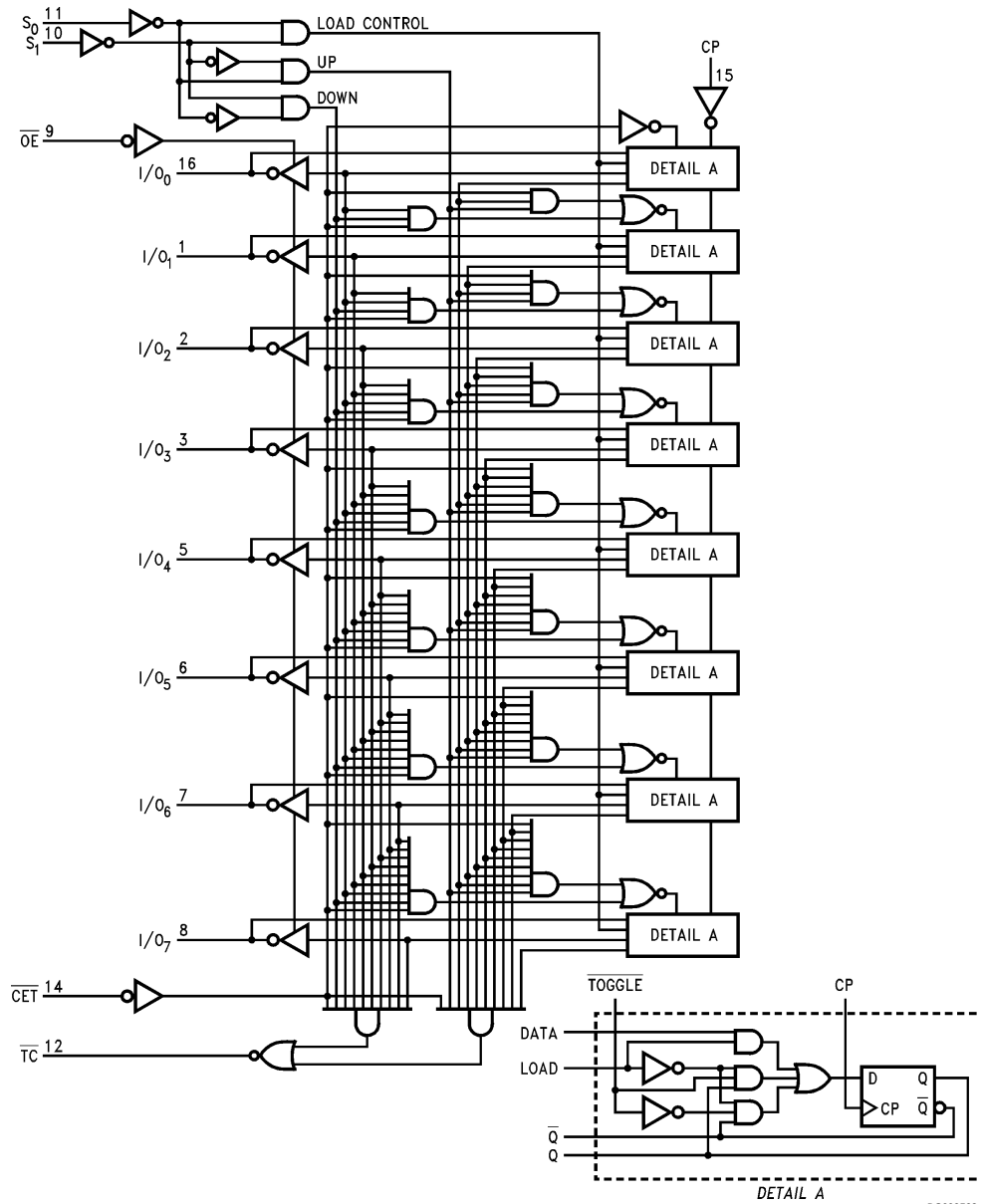
Logic Symbol



Connection Diagram



Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Unit Loading/Fan Out

Pin Names	Description	74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
$I/O_0-I/O_7$	Data Inputs	0.25/0.33	5 μA /-0.2 mA
	Data Outputs	75/15 (12.5)	-3 mA/24 mA (20 mA)
S_0, S_1	Select Inputs	0.25/0.33	5 μA /-0.2 mA
$\overline{OE}$	Output Enable Input (Active LOW)	0.25/0.33	5 μA /-0.2 mA
$\overline{CET}$	Count Enable Trickle Input (Active LOW)	0.25/0.33	5 μA /-0.2 mA
CP	Clock Pulse Input (Active Rising Edge)	0.25/0.33	5 μA /-0.2 mA
$\overline{TC}$	Terminal Count Output (Active LOW)	25/12.5	-1 mA/20 mA

Function Table

S_1	S_0	$\overline{CET}$	$\overline{OE}$	CP	Function
X	X	X	H	X	I/O_0 to I/O_7 in High Z
X	X	X	L	X	Flip-Flop Outputs Appear on I/O Lines
L	L	X	H	↗	Parallel Load All Flip-Flops
(Not LL)	H	X	↗		Hold ($\overline{TC}$ Held HIGH)
H	H	X	X	↗	Hold
H	L	L	X	↗	Count Up
L	H	L	X	↗	Count Down

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

↗ = LOW-to-HIGH Clock Transition

(Not LL) means S_0 and S_1 should never both be LOW level at the same time.

Absolute Maximum Ratings (Note 2)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
Plastic	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 3)	-0.5V to +7.0V
Input Current ((Note 3)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	-0.5V to V _{CC}
3-STATE Output	-0.5V to +5.5V
Current Applied to Output	

in LOW State (Max) twice the rated I_{OL} (mA)
ESD Last Passing Voltage (Min) 4000V

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Commercial	
Supply Voltage	
Commercial	+4.5V to +5.5V

Note 2: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 3: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	74F			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage		0.8		V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage		-1.2		V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH	74F 10% V _{CC}	2.4		V	Min	I _{OH} = -3 mA
	Voltage	74F 5% V _{CC}	2.7				
V _{OL}	Output LOW	74F 10% V _{CC}		0.5	V	Min	I _{OL} = 20 mA
	Voltage	74F 5% V _{CC}		0.5			I _{OL} = 20 mA
I _{IH}	Input HIGH Current	74F		5.0	μA	Max	V _{IN} = 2.7V (Non-I/O Pins)
I _{BVI}	Input HIGH Current Breakdown Test	74F		7.0	μA	Max	V _{IN} = 7.0V (Non-I/O Pins)
I _{BVIT}	Input HIGH Current Breakdown (I/O)	74F		0.5	mA	Max	V _{IN} = 5.5V (I/O _n)
I _{CEX}	Output HIGH Leakage Current	74F		50	μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	74F	4.75		V	0.0	I _{ID} = 1.9 μA All other pins grounded
I _{OD}	Output Leakage Circuit Current	74F		3.75	μA	0.0	V _{IOD} = 150 mV All other pins grounded
I _{ZZ}	Bus Drainage Test			500	μA	0.0	V _{OUT} = 5.25V
I _{IL}	Input LOW Current		-0.2		mA	Max	V _{IN} = 0.5V (Non I/O Pins)
I _{IH} + I _{OZH}	Output Leakage Current		70		μA	Max	V _{OUT} = 2.7V (I/O _n)
I _{IL} + I _{OZL}	Output Leakage Current		-200		μA	Max	V _{OUT} = 0.5V (I/O _n)
I _{OS}	Output Short-Circuit Current		-60	-150	mA	Max	V _{OUT} = 0V
I _{CCH}	Power Supply Current			90	mA	Max	V _O = HIGH
I _{CCL}	Power Supply Current			105	mA	Max	V _O = LOW
I _{CCZ}	Power Supply Current			110	mA	Max	V _O = HIGH Z

AC Electrical Characteristics

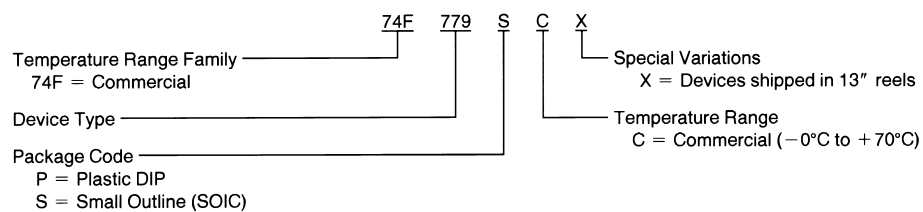
Symbol	Parameter	74F			74F		Units
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$		
		Min	Typ	Max	Min	Max	
f_{max}	Maximum Clock Frequency	100	105		90		
t_{PLH}	Propagation Delay	3.0	5.0	8.0	3.0	8.5	ns
t_{PHL}	CP to I/O_n	5.0	7.5	11.0	5.0	11.0	
t_{PLH}	Propagation Delay	5.0	7.5	9.0	5.0	10.0	ns
t_{PHL}	CP to $\overline{\text{TC}}$	5.0	9.3	10.5	5.0	11.5	
t_{PLH}	Propagation Delay	2.5	3.8	5.5	2.5	6.0	ns
t_{PHL}	$\overline{\text{CET}}$ to $\overline{\text{TC}}$	4.5	6.1	8.0	4.5	8.5	
t_{PLH}	Propagation Delay	3.5	6.5	12.0	3.5	13.0	ns
t_{PHL}	SN to $\overline{\text{TC}}$	3.5	7.5	12.0	3.5	13.0	
t_{PZH}	Output Enable Time	3.0	5.0	7.0	3.0	8.0	ns
t_{PZL}	$\overline{\text{OE}}$ to I/O_n	5.0	8.0	10.0	5.0	10.5	
t_{PHZ}	Output Disable Time	1.0	4.0	6.5	1.0	7.0	ns
t_{PLZ}	$\overline{\text{OE}}$ to I/O_n	1.0	3.7	6.5	1.0	7.0	

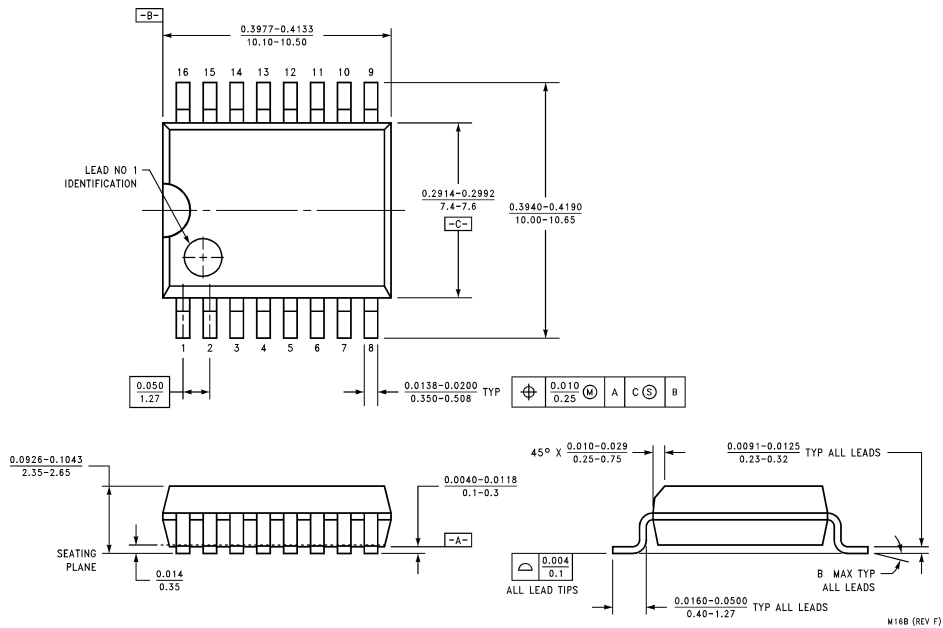
AC Operating Requirements

Symbol	Parameter	74F		74F		Units
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Com}$		
		Min	Max	Min	Max	
$t_s(\text{H})$	Setup Time	5.0		5.0		ns
$t_s(\text{L})$	I/O _n to CP	5.0		5.0		
$t_h(\text{H})$	Hold Time	0.0		0.0		ns
$t_h(\text{L})$	I/O _n to CP	0.0		0.0		
$t_s(\text{H})$	Setup Time	9.5		10.0		ns
$t_s(\text{L})$	Sn to CP	9.5		10.0		
$t_h(\text{H})$	Hold Time	0.0		0.0		ns
$t_h(\text{L})$	Sn to CP	0.0		0.0		
$t_s(\text{H})$	Setup Time	7.0		7.0		ns
$t_s(\text{L})$	$\overline{\text{CET}}$ to CP	7.0		7.0		
$t_h(\text{H})$	Hold Time	0.0		0.0		ns
$t_h(\text{L})$	$\overline{\text{CET}}$ to CP	0.0		0.0		
$t_w(\text{H})$	Clock Pulse Width	4.0		4.0		ns
$t_w(\text{L})$	High or Low	4.0		4.0		

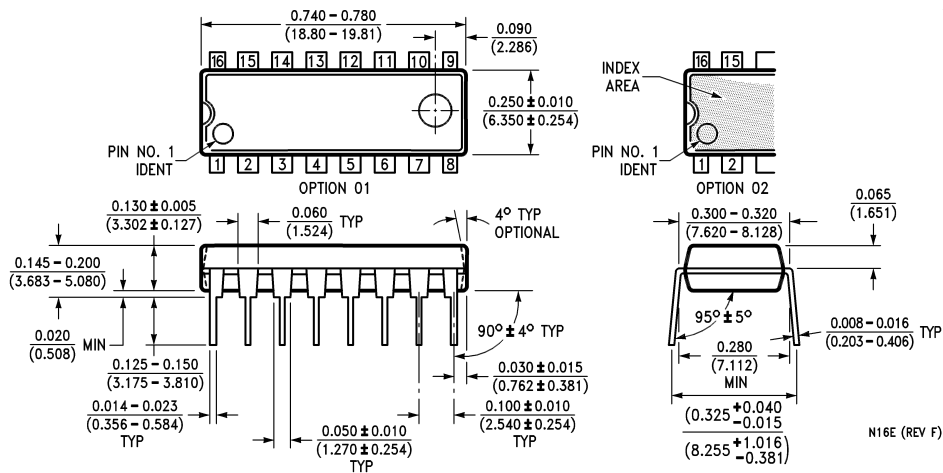
Ordering Information

The device number is used to form part of a simplified purchasing code where a package type and temperature range are defined as follows:



Physical Dimensions inches (millimeters) unless otherwise noted

**16-Lead (0.300" Wide) Small Outline Package, JEDEC
Package Number M16B**



**16-Lead (0.300" Wide) Molded Dual-In-Line Package (P)
Package Number N16E**

