MC80364K64

Low Power 3.3V/2.5V

64Kx64 PBSRAM

Preliminary Information

- **High performance, low power pipeline burst SRAM**
  - Ultra low power single chip 512Kbyte Cache for green PC and battery powered PC
- **High performance**
  - 83-133MHz Speed grades
  - 3-1-1-1 Burst Read
  - 1-1-1-1 Burst Write
  - 3-1-1-1-1-1-1-1... pipeline operation
- **Low power**
  - Low active power
  - Ultra low power ZZ standby mode
  - Single 3.3V supply (V_{DD})
  - Isolated 3.3V or 2.5V I/O supply (V_{DDQ})
- **Compatibility**
  - Individual Byte Write and Global Write masking
  - Interleave and burst address support
  - Three chip enables for easy expansion
  - Industry standard 128-Pin PBSRAM pinout
  - Industry standard PBSRAM specification
- **Applications**
  - Pentium® and PowerPC™ pipelined L2 Cache
  - Ideal for high speed, low power communications buffers
  - Power sensitive portable and DSP applications

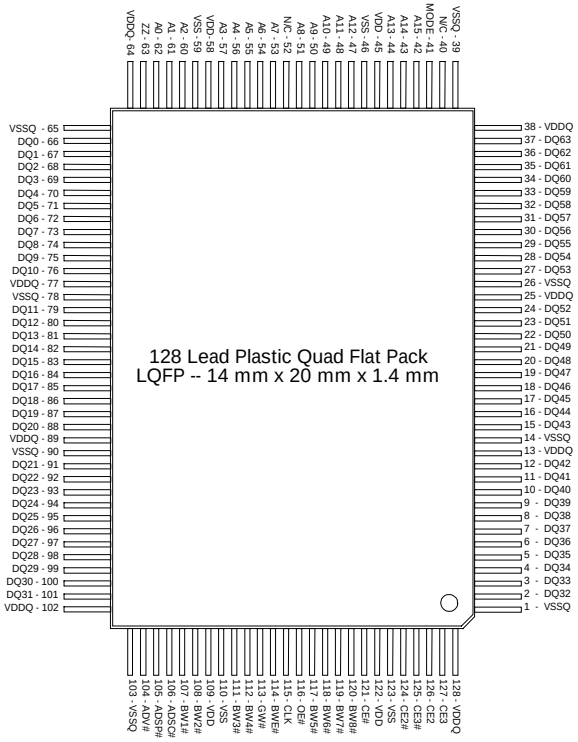


Figure 1. Pin Function

Overview

The MoSys MC80364K64 is a high performance, low power pipeline-burst-SRAM (PBSRAM)). Fabricated using an advanced low power, high performance CMOS process, the MoSys MC80364K64 is pin and function compatible with industry standard 64Kx64 PBSRAM specification.

The MoSys MC80364K64 supports PBSRAM operating modes at maximum burst frequency including indefinite pipeline read or write (3-1-1-1-1-1-1...)

Available in 64Kx64 capacity, the MoSys MC80364K64 is packaged in a standard 128 lead LQFP.

Sleep Mode

MoSys x64 Pipeline Burst Cache supports sleep mode (ZZ).

Low Power

The MC80364K64 affords systems dramatic power savings due to the benefits of it's proprietary MoSys technology. Peak operating power of typical PBSRAM is 7x that of MC80364K64. Making it ideal for portable applications, as well as applications requiring a large amount of RAM.

Part Number Designation

Example*: MC80364K64L-10*
Device Designation: *MC8*, Series: *03*
Organization: *64K64*
Package Type: L=LQFP
Speed: *–10* = 100 MHz

Table 1. Pin Description

Pin Number	Symbol	Type	Description
62, 61, 60, 57, 56, 55, 54, 53, 51, 50, 49, 48, 47, 44, 43, 42	A[15:0]	Input	Processor Addresses
107, 108, 111, 112, 117, 118, 119, 120	BW[8:1]#	Input	Processor host bus byte enables.
113	GW#	Input	Global Write from cache controller
114	BWE#	Input	Byte Write Enable from controller
115	CLK	Input	Processor host bus clock
121	CE#	Input	ADSP# mask and ADSC# chip enable
124	CE2#	Input	Depth expansion chip enable
125	CE3#	Input	Depth expansion chip enable
126	CE2	Input	Depth expansion chip enable
127	CE3	Input	Depth expansion chip enable
116	OE#	Input	Asynchronous output enable
104	ADV#	Input	Burst address counter advance
105	ADSP#	Input	ADS# of processor
106	ADSC#	Input	ADS# of controller
63	ZZ		Sleep-mode: ZZ
66, 67,68, 69, 70, 71, 72, 73, 74, 75, 76, 79, 80, 81, 82, 83, 84, 85, 86 ,87, 88, 91,92, 93, 94, 95, 96, 97, 98, 99, 100, 101, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 15, 16, 17, 18, 19, 20, 21, 22 ,23, 24, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37	DQ[63:0]	I/O	Data I/O pins
41	MODE	Input	Burst Mode Select
40, 52	N/C	-	Not connected internally
122, 109,58, 45	VDD	3.3 Volts	Power
123, 110, 59, 46	VSS	Ground	Ground
13, 25, 38, 64, 77, 89, 102 128	VDDQ	I/O Supply	I/O Buffer Supply
1, 14, 26, 39, 65, 78, 90, 103,	VSSQ	I/O Ground	I/O Buffer Ground

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
V_{DD}	Core Supply Voltage		3.6	V
V_{DDQ}	I/O Supply Voltage		3.6	V
V_{ih}	Input High Voltage		V_{DDQ} +0.5	V
V_{il}	Input Low Voltage	V_{SSQ}-0.5		V
Ts	Storage Temperature	-65	150	?C

Notes: Max Vih is not to exceed maximum VDDQ

Table 3. Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Max	Units
V_{DD}	Supply Voltage	3.3V +10%/-5%	3.135	3.6	V
V_{DDQ}	I/O Supply Voltage	2.5V +44%/-5%	2.375	3.6	V
V_{ih}	Input High Voltage		1.7	V_{DDQ} + .3	V
V_{il}	Input Low Voltage		-0.3	0.8	V
V_{oh1}	Output High Voltage	I_{oh} = -5 mA V_{DDQ} = 3.3V	2.4		V
V_{oh2}	Output High Voltage	I_{oh} = -5 mA V_{DDQ} = 2.5V	2.0		V
V_{ol}	Output Low Voltage	I_{ol} = 5 mA		0.4	V

Table 4. Absolute Maximum AC Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{ih}	Input High Voltage	1.7	V_{DDQ}+1.0	V
V_{il}	Input Low Voltage	V_{SSQ} - 1.0	0.8	V
tOVR	Overshoot/Undershoot Voltage Duration		0.2*tCY	ns
tSET	Overshoot/Undershoot Settling Time		0.8*tCY	ns

Table 5. Maximum DC Current Requirements

Symbol	Condition	2.5V Supply	3.3V Supply	Units
I_{DD}	Operating current, device selected; all inputs $\leq$ Vil or $\geq$ Vih; cycle time $\geq$ tKC min, VCC = max, 0 pF load	10	50	mA
I_{DD1}	Idle current, device selected; ADSP#, ADSC#, GW#, BW#s, ADV# and all other inputs $\geq$ 2.8 volts; cycle time $\geq$ tKC min, VCC = max, 0 pF load	2	15	mA
I_{DD2}	Clock stopped, all inputs $\geq$ 2.8 v, VCC = max	1	1	mA
I_{DDZZ}	Sleep mode, clock stopped, all inputs $\geq$ 2.8 v, VCC = max	1	1	mA

Figure 2. AC Timing Definitions

Table 6. AC Timing Characteristics at Recommended Operating Conditions

		-7R5 (133 MHz)		-8R5 (117 MHz)		-10 (100 MHz)		-12 (83 MHz)		
Sym	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
tAAH	ADV# hold	0.5		0.5		0.5		0.5		ns
tAAS	ADV# setup	2		2		2		2		ns
tADSH	ADSx# hold	0.5		0.5		0.5		0.5		ns
tADSS	ADSx# setup	2		2		2		2		ns
tAH	Address hold	0.5		0.5		0.5		0.5		ns
tAS	Address setup	2		2		2		2		ns
tCEH	Chip Enable hold	0.5		0.5		0.5		0.5		ns
tCES	Chip Enable setup	2		2		2		2		ns
tDH	Write Data hold	0.5		0.5		0.5		0.5		ns
tDS	Write Data setup	2		2		2		2		ns
tKC	Clock cycle	7.5		8.5		10		12		ns
tKH	Clock high	2		2.5		3.2		4		ns
tKL	Clock low	2		2.5		3.2		4		ns
tKQ	Clock to output valid		4.5		5		5.5		6	ns
tKQHZ	Clock to output high-Z	1.5	7.5	1.5	8.6	1.5	10	1.5	12	ns
tKQLZ	Clock to output low-Z	0		0		0		0		ns
tKQX	Clock to output invalid	1.5		1.5		1.5		1.5		ns
tOELZ	OE# to output low-Z	0		0		0		0		ns
tOEHZ	OE# to output high-Z		4.5		4.8		5.5		6	ns
tOEQ	OE# to output valid		4.5		4.8		5.5		6	ns
tOEQX	OE# to output invalid	0		0		0		0		ns
tWS	GW#, BWx# setup	2		2		2		2		ns
tWH	GW#, BWx# hold	0.5		0.5		0.5		0.5		ns
tZZs	ZZ standby		100		100		100		100	ns
tZZREC	ZZ recovery	100		100		100		100		

NOTE: V_{DDQ} = 2.5V (+44%/-5%), V_{DD} = 3.3V (+10%/-5%)

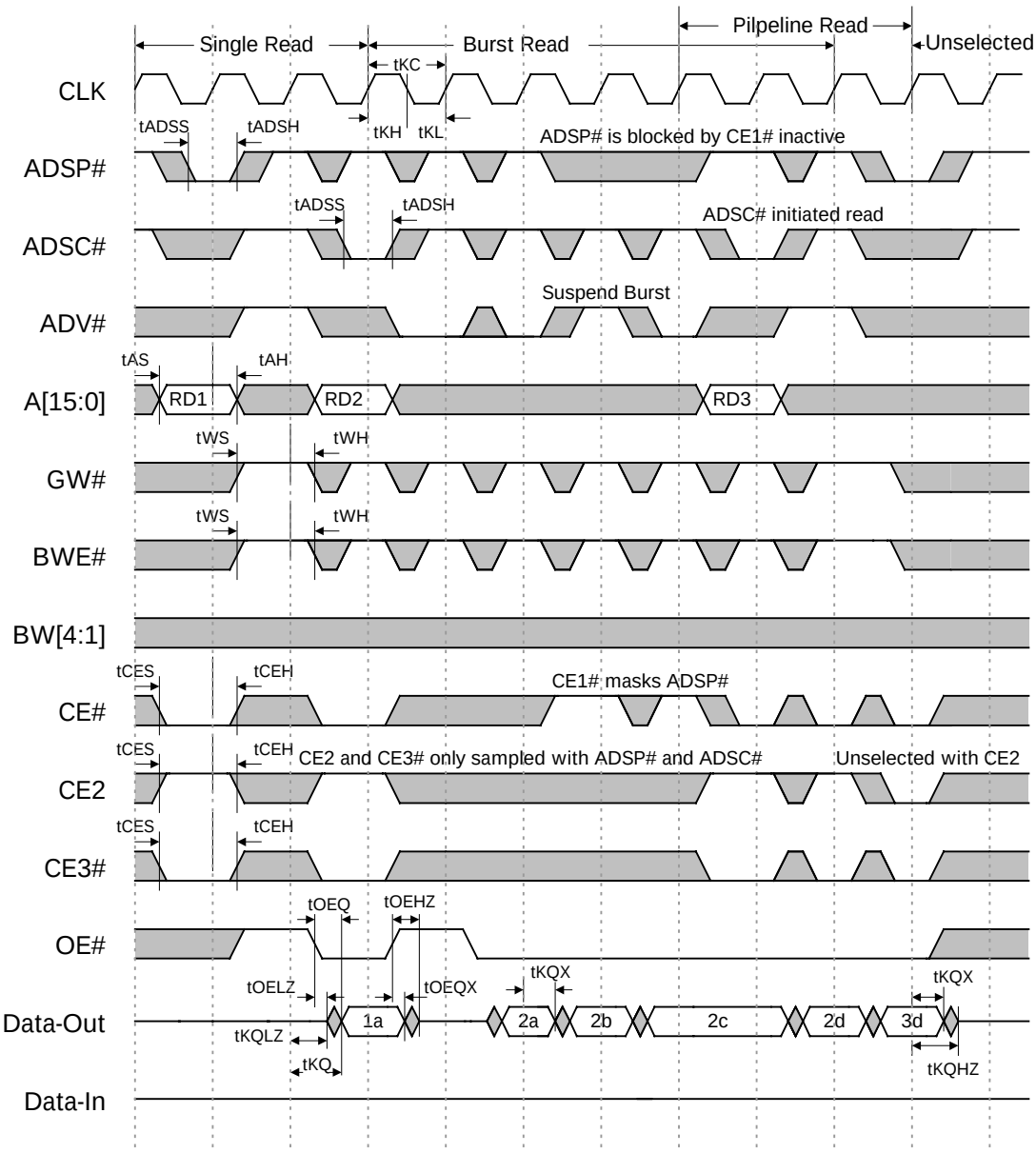


Figure 3 Read Cycle Timing

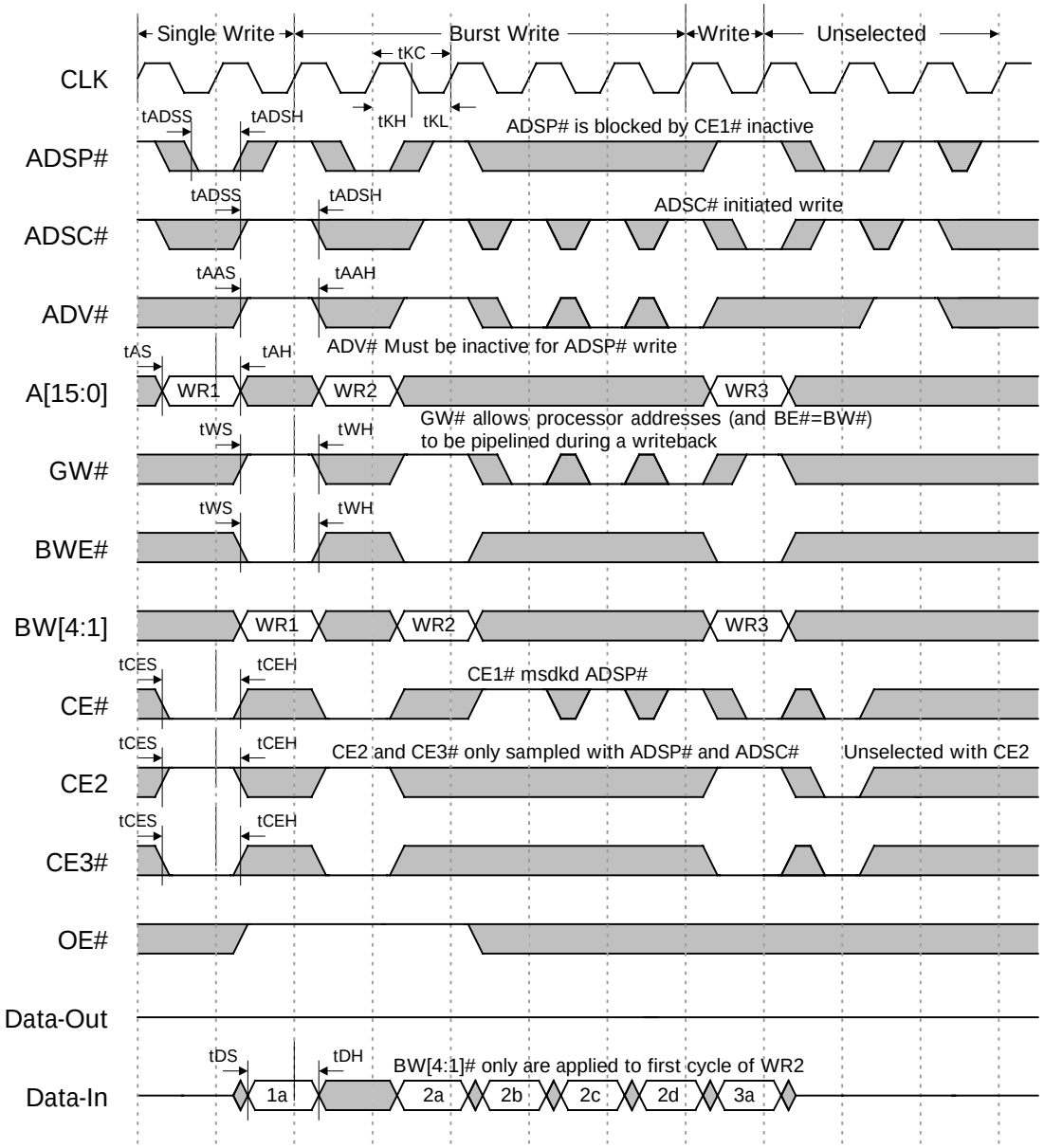


Figure 4 Write Cycle Timing

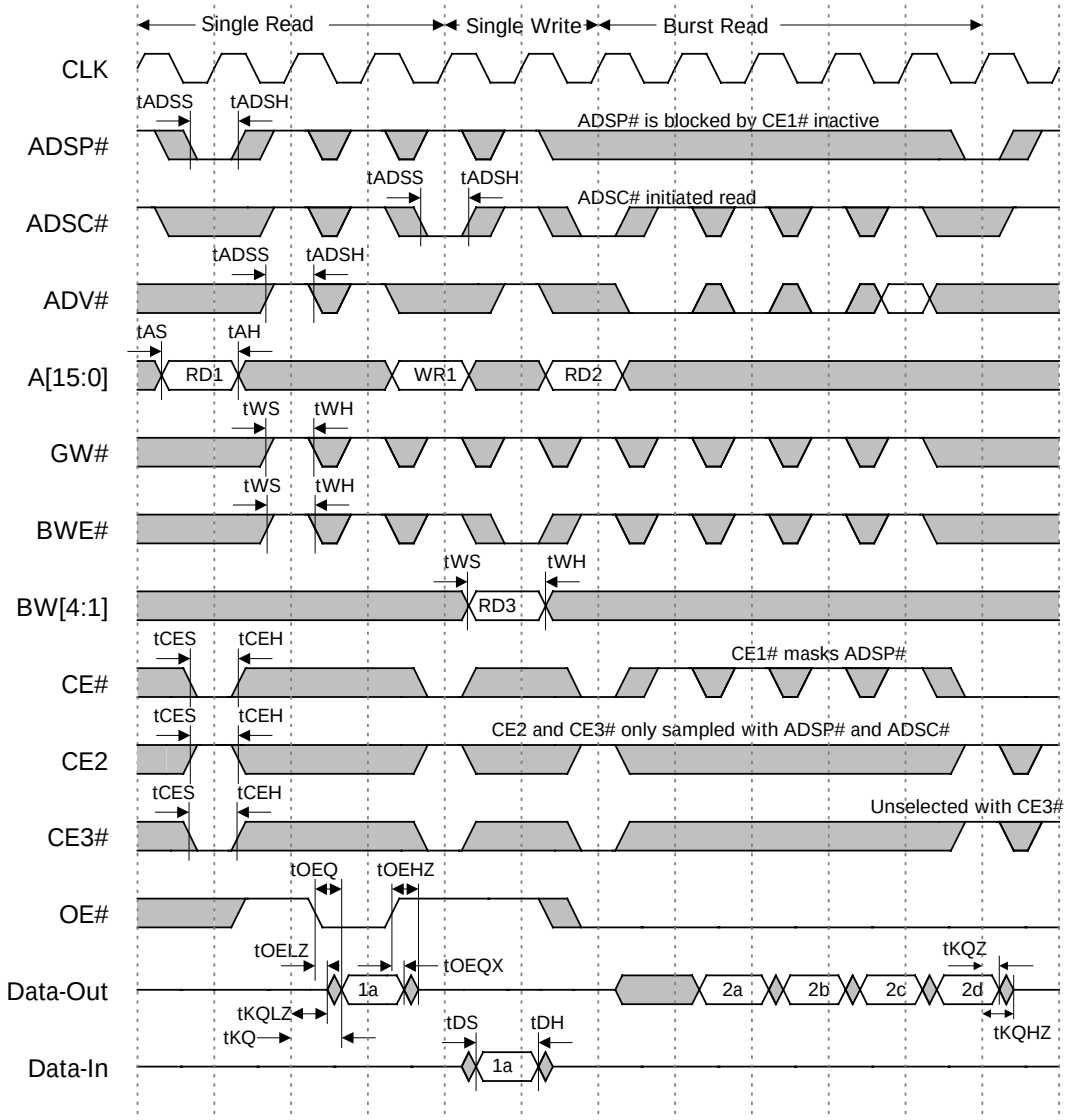


Figure 5 Read/Write Cycle Timing

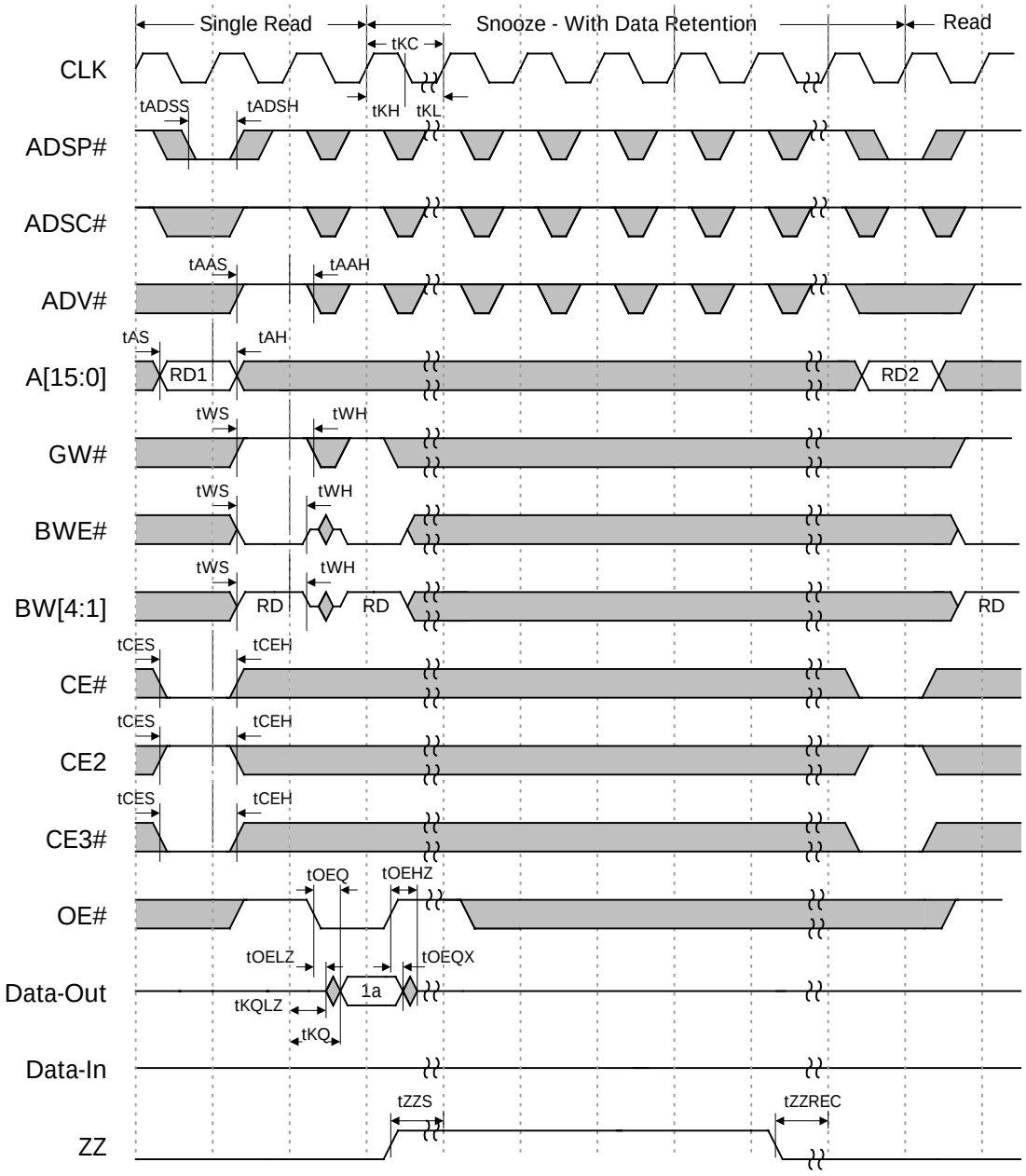
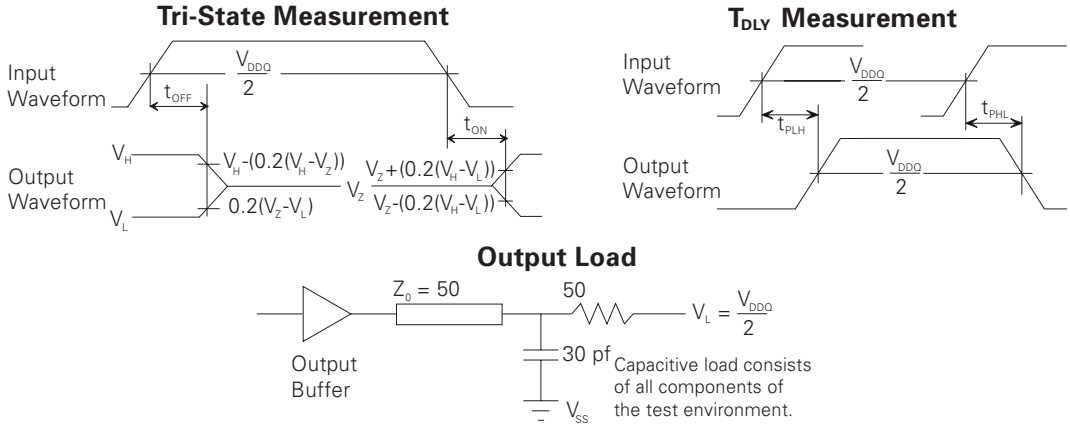


Figure 6 ZZ and RD Timing

Test and Measurement



Test Structure and Measurement Points

Notes

1 Valid Delay Measurement is made from the VDDQ / 2 on the input waveform to the VDDQ / 2 on the output waveform. Input waveform should have a slew rate of 1V/ns.

Tri-state t_{off} measurement is made from the VDDQ/2 on the input waveform to the output waveform moving 20% from its initial to final value VDDQ/2.

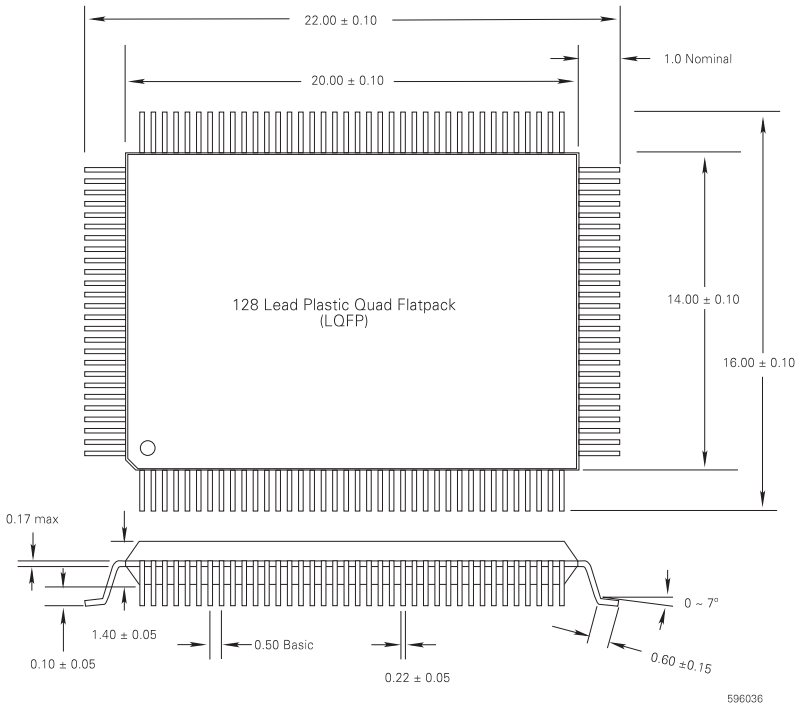


Figure 7. LQFP Mechanical Characteristics